

# ESD Ratings of SiC FETs and Cascode JFETs

## AND90325/D

### Introduction

This Application Note discusses the ESD capabilities of onsemi transistor offerings.

### ESD Rating of SiC FETs

onsemi's FET product line is built on the core technology of a High-Voltage, Normally-On SiC JFET coupled with a Low Voltage, Normally-Off Silicon MOSFET in a cascode configuration. Given the cascode configuration of the SiC JFET and Si MOSFET, the MOSFET is connected to the Gate and Source pins of a package, and it the limiting device when it comes to ESD capability. The JFETs are p-n junctions and can handle far more ESD than the MOSFET. Our MOSFETs use integrated diodes as ESD protection, and the size and capacitance of the MOSFET become the determining factor in ESD capability.



onsemi cascode FETs utilize a low voltage MOSFET to turn the Normally-On JFET to a Normally-Off device with the Gate drive behavior of a Silicon MOSFET.

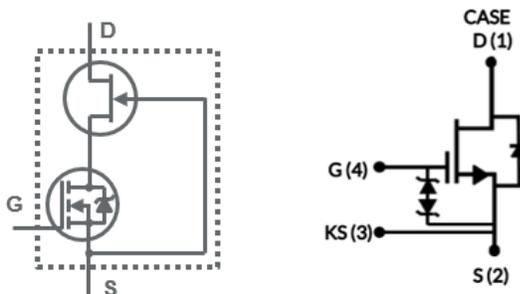


Figure 1. (Left) Basic Cascode Diagram Showing the MOSFET Drain Connected to the JFET Source. (Right) Cascode Diagram Showing Back-to-Back Diodes on the Gate to Source Pads of the MOSFET.

Across the onsemi SiC FET product lines we use a family of MOSFETs that are scaled to the size and RDSon of the JFET. The smallest JFETs will require the smallest MOSFETs, and these become the limiting ESD ratings for our parts. This also means by ESD testing the MOSFETs alone, we determine the ESD ratings of all products that use that MOSFET.

For the Charged Device Model samples of every MOSFET were tested up to ±2000 V and passed. This puts the parts into CDM class C3 (>1000 V). For Human Body

Model testing, samples of every MOSFET were tested up to ±8000 V on each of the 3 pin combinations. All MOSFETs passed to 8000 V for the Drain to Source pin pair. Gate to Source and Gate to Drain testing varied from device size. The smallest MOSFETs passed at Gate-to-Source at 3900 V and Gate-to-Drain at 3700 V. This sets the minimum HBM class H2 (>2000 V to <4000 V) for all onsemi devices.

### ESD Rating of SiC FETs

Similar to the MOSFETs, the onsemi family of SiC JFETs are scaled with size and the smallest devices are the most sensitive to ESD. Unlike the MOSFETs, the JFET is fundamentally insensitive to ESD because the device is made up of p-n junctions. Utilizing the smallest JFET in the lineup, Charged Device Model testing was done to ±1000 V, and Human Body Model testing for all pin pairs was done to ±8000 V. Putting all JFETs in the C3 and H3A classes, respectively.

Table 1. ESD Results for MOSFETs

P/N	CDM		HBM			
	Class	Results	Class	G to S	G to D	D to S
AW1044	C3	±2 kV	3B	8 kV	8 kV	8 kV
AW1046	C3	±2 kV	2	3.9 kV	3.7 kV	8 kV
AW1048	C3	±2 kV	3A	4.9 kV	4.6 kV	8 kV
AW1060	C3	±2 kV	3B	8 kV	8 kV	8 kV
AW1065	C3	±2 kV	3A	4.8 kV	4.9 kV	8 kV

The Larger SiC FETs with larger MOSFETs will outperform the H2 classification. The two largest devices, are rated to class 3B (>8000 V).

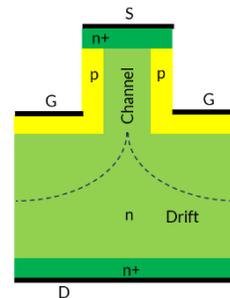


Figure 2. Unit Cell of JFET Structure Highlighting (a) the Lack of Gate Oxide, and (b) the 2 p-n Junctions (Gate-to-Drain, and Gate-to-Source).

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