3-phase Inverter Power Module 1200 V SPM 31 Series

AND90338/D

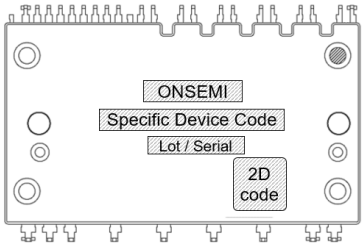
INTRODUCTION

This application note provides practical guidelines for designing with the SPM 31 Series power modules. This series of Intelligent Power Modules (IPM) for 3-phase motor drives contains a three-phase inverter stage, gate drivers.

Design Concept

The SPM 31 design objective is to provide a minimized package and a low power consumption module with improved reliability. It is achieved by applying new gate-driving High-Voltage Integrated Circuit (HVIC), a new Silicon Carbide Metal-Oxide-Semiconductor Field-Effect Transistor (SiC MOSFET) of advanced silicon technology and improved Direct Bonded Copper (DBC) substrate based on transfer mold package. The SPM 31 achieves reduced board size and improved reliability compared to existing discrete solutions. Target applications are inverter motor drives for industrial use, such as commercial air conditioners, general-purpose inverters and servo motors. The temperature sensing function of SPM 31 products are implemented in the LVIC to enhance the system reliability. The analog voltage proportional to the temperature of the LVIC in module is provided for monitoring the module temperature and necessary protections against over-temperature situations. Figure 1 shows the package outline structure.

MARKING DIAGRAM



1. NFAMxx12SCBUT = Specific Device Code
2. ZZZ = Assembly Lot Code
3. A = Assembly Location
4. T = Test Location
5. Y = Year
6. WW = Work Week

2D Code
Device marking is on package top side

ORDERING INFORMATION

Device	Package	Shipping (Q'ty / Packing Type)
NFAMxx12SCBUT	DIP39, 31.0x54.5	90 / BOX

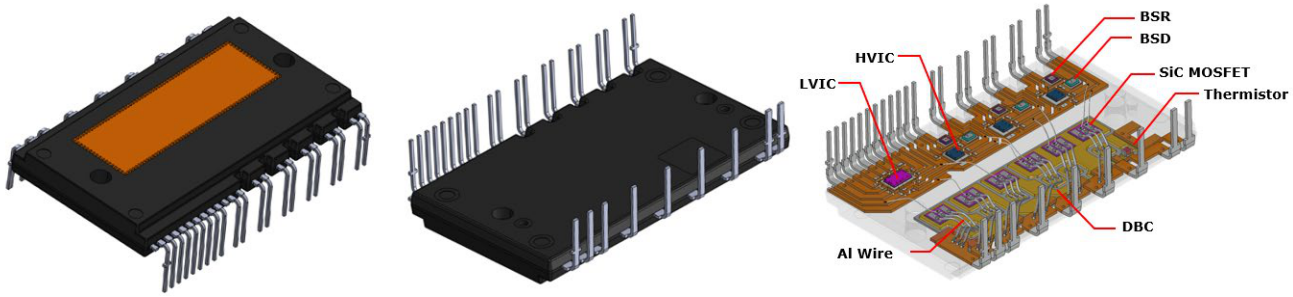


Figure 1. External View and Internal Structure of SPM 31

Key Features

- 1200 V / 40, 50, 70 A, three phase SiC MOSFET inverter including control ICs for gate driving and protections
- Very low thermal resistance by adopting DBC substrate
- Easy PCB layout thanks to built-in bootstrap circuits
- Open source configuration for easy monitoring of each phase current sensing
- Single-grounded power supply thanks to built-in HVICs and bootstrap operations
- Built-in temperature sensing function by LVIC and NTC
- Isolation Rating of 2500 Vrms / min.

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PRODUCT DESCRIPTION

Ordering Information

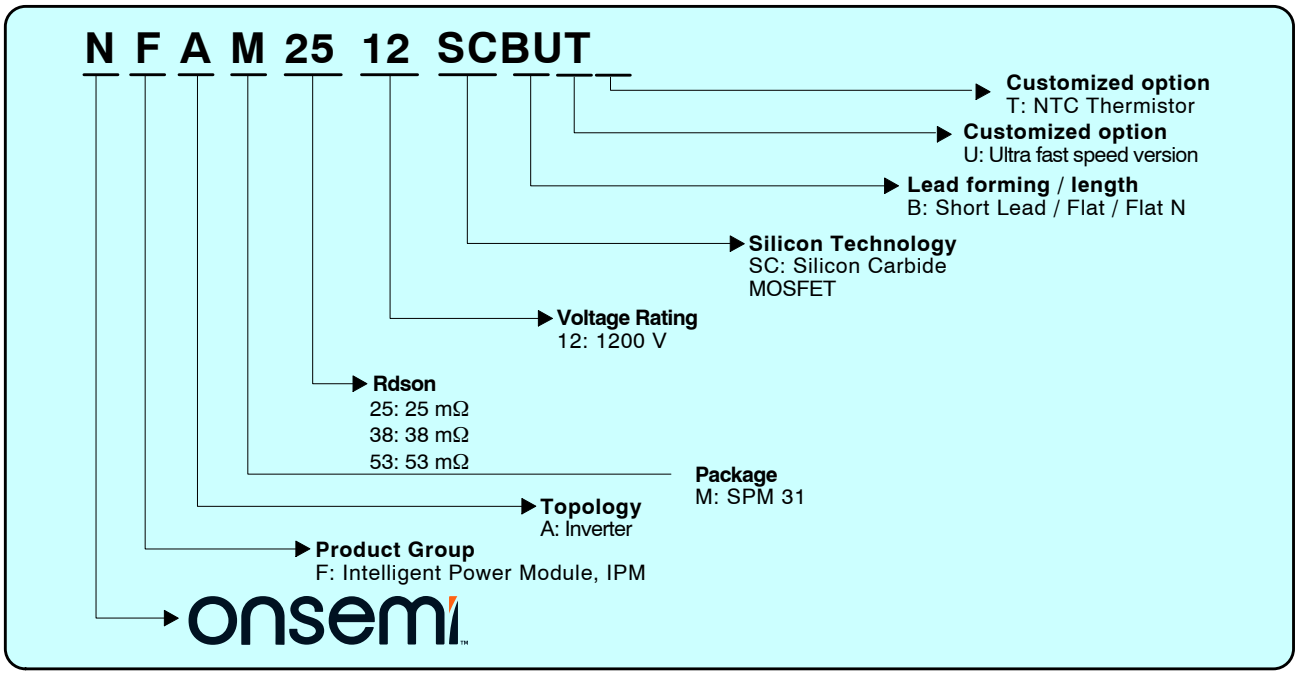

Figure 2. Ordering Information

Product Line-up

Table 1 shows the SPM31 product line up without package variations. Online simulation tool (Click for simulation tool) is recommended to find out the right product for the desired application. For package drawing, please refer to chapter Package Outline.

Table 1. PRODUCT LINE-UP

Product	Current/Voltage	Recommend Power (Note 1)	Target Application	Isolation Voltage
NFAM5312SCBUT	40 A / 1200 V	7. 0 kW	Air Conditioners, Industrial motors, General-purpose inverters, Servo motors	V_{ISO} = 2500 V_{RMS} (Sine 60 Hz, 1-min All Shorted Pins Heat Sink)
NFAM3812SCBUT	50 A / 1200 V	9.0 kW		
NFAM2512SCBUT	70 A / 1200 V	12.0 kW		

1. These power ratings are simulated result by specific operating conditions, so it can be changed by the operating conditions.
2. Under development.

Internal Circuit Diagram

Three bootstrap circuits generate the voltage needed for driving the high-side MOSFETs. The bootstrap diodes are internal part in HVIC and driving voltage of high-side MOSFETs is sourced from VDD (18 V) through bootstrap circuits. There is an internal level shift circuit for the high-side drive signals allowing all control signals to be driven directly from GND levels common with the control circuit such as the microcontroller without requiring external isolation with opto-couplers. LVIC temperature sensing signal is output from the VTS pin. SPM31 has built-in NTC that senses the temperature of the power chip. NTC is shown on pins 38 and 39 of the internal circuit diagram as shown in Figure 3.

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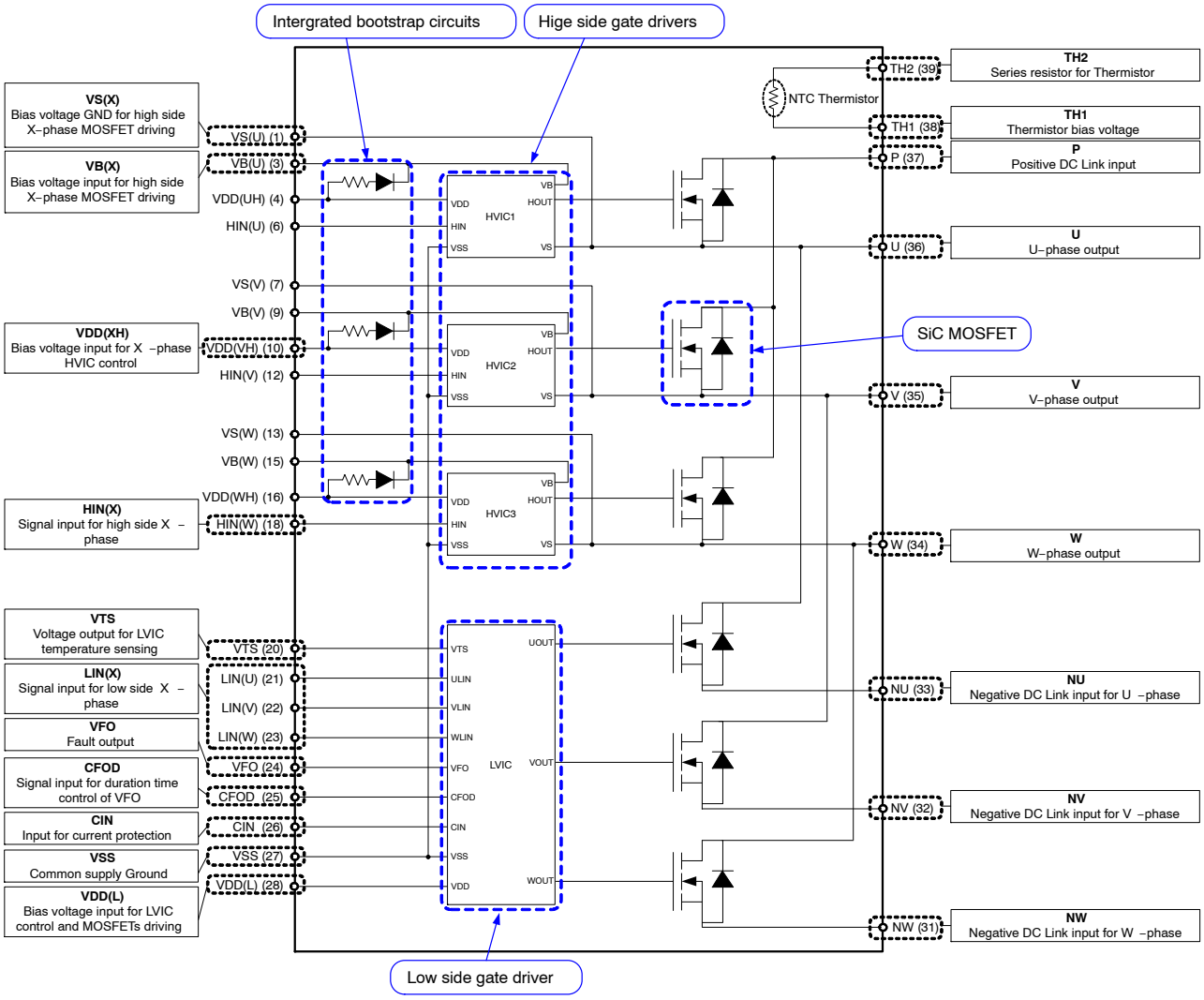

Figure 3. Internal Equivalent Circuit Diagram

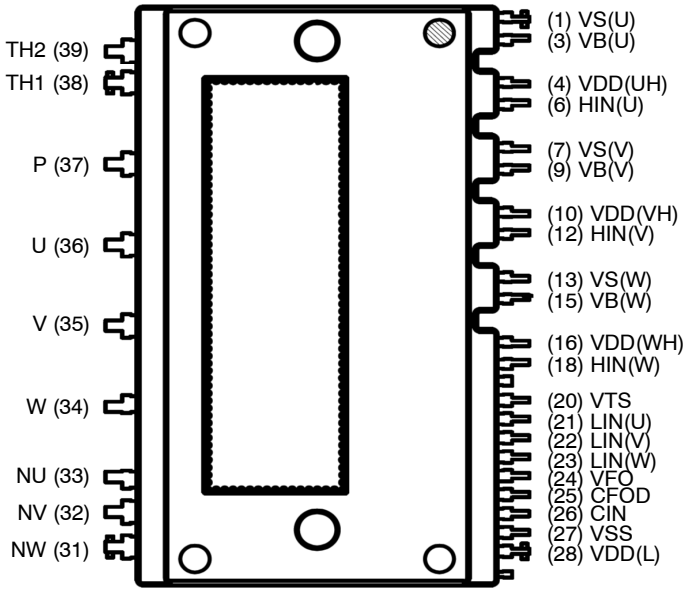

Figure 4. Package Top-View and Pin Assignment

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Table 2. NUMBERS, NAMES AND DUMMY PINS

Pin Number	Name	Description
1	VS(U)	High-Side Bias Voltage GND for U Phase MOSFET Driving
(2)	–	Dummy
3	VB(U)	High-Side Bias Voltage for U Phase MOSFET Driving
4	VDD(UH)	High-Side Bias Voltage for U Phase IC
(5)	–	Dummy
6	HIN(U)	Signal Input for High-Side U Phase
7	VS(V)	High-Side Bias Voltage GND for V Phase MOSFET Driving
(8)	–	Dummy
9	VB(V)	High-Side Bias Voltage for V Phase MOSFET Driving
10	VDD(VH)	High-Side Bias Voltage for V Phase IC
(11)	–	Dummy
12	HIN(V)	Signal Input for High-Side V Phase
13	VS(W)	High-Side Bias Voltage GND for W Phase MOSFET Driving
(14)	–	Dummy
15	VB(W)	High-Side Bias Voltage for W Phase MOSFET Driving
16	VDD(WH)	High-Side Bias Voltage for W Phase IC
(17)	–	Dummy
18	HIN(W)	Signal Input for High-Side W Phase
(19)	–	Dummy
20	VTS	Voltage Output for LVIC Temperature Sensing Unit
21	LIN(U)	Signal Input for Low-Side U Phase
22	LIN(V)	Signal Input for Low-Side V Phase
23	LIN(W)	Signal Input for Low-Side W Phase
24	VFO	Fault Output
25	CFOD	Capacitor for Fault Output Duration Selection
26	CIN	Input for Over Current Protection
27	VSS	Low-Side Common Supply Ground
28	VDD(L)	Low-Side Bias Voltage for IC and MOSFETs Driving
(29)	–	Dummy
(30)	–	Dummy
31	NW	Negative DC-Link Input for W Phase
32	NV	Negative DC-Link Input for V Phase
33	NU	Negative DC-Link Input for U Phase
34	W	Output for W Phase
35	V	Output for V Phase
36	U	Output for U Phase
37	P	Positive DC-Link Input
38	TH1	Thermistor Bias Voltage (T) / Not connection
39	TH2	Series Resistor for Thermistor (Temperature Detection) *optional for T

3. Pins of ( ) are the dummy for internal connection. These pins should be no connection.

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Detailed Pin Definition and Notification

Pins: VB(U)−VS(U), VB(V)−VS(V), VB(W)−VS(W)

- High-side bias voltage pins for driving the MOSFETs and high-side bias voltage ground pins for driving the MOSFETs.
- VB(U), VB(V), VB(W) pins are connected to cathode pins of bootstrap diodes on each phase.
- These are drive power supply pins for providing gate drive power to the high-side MOSFETs.
- The virtue of the ability to bootstrap the circuit scheme is that no external power supplies are required for the high-side MOSFETs.
- Each bootstrap capacitor is charged from the VDD supply during ON state of the corresponding low-side MOSFETs.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low-ESR, low-ESL) filter capacitor should be mounted very close to these pins.

Pins: VDD(L), VDD(UH), VDD(VH), VDD(WH)

- Low-side and high-side bias voltage pins.
- These are control supply pins for the built-in ICs.
- These four pins should be connected externally.
- To prevent malfunctions caused by noise and ripple in the supply voltage, a good quality (low-ESR, low-ESL) filter capacitor should be mounted very close to these pins.

Pins: VSS

- Common supply ground pin.
- This is supply ground pin for the built-in ICs.
- Important! To avoid noise influences, the main power circuit current should not be allowed to blow through this pin.

Pins: HIN(U/V/W), LIN(U/V/W)

- Signal input pins.
- These pins control the operation of the built-in MOSFETs.
- They are activated by voltage input signals. The terminals are internally connected to a Schmitt-trigger circuit composed of 5 V-class CMOS.
- The signal logic of these pins is active high. The MOSFET associated with each of these pins is turned ON when a sufficient logic voltage is applied to these pins.
- The wiring of each input should be as short as possible to protect the SPM 31 products against noise influences.
- To prevent signal oscillations, an RC coupling as illustrated in Figure 22 is recommended.

Pin: CIN

- Over-current and short-circuit detection input pin.
- The current sensing shunt resistor should be connected between the low-pass filter before the CIN pin and the low-side ground pin VSS to detect over or short circuit current.
- The shunt resistor should be selected to meet the detection levels matched for the specific application.
- An RC filter should be connected to the CIN pin to eliminate noise.
- The connection length between the shunt resistor and CIN pin should be minimized.

Pin: VFO

- Fault output pin.
- This is the fault output alarm pin. An active low output is given on this pin for a fault state condition in the SPM 31 products.
- The alarm conditions are Over-Current Protection (OCP), or low-side bias Under-Voltage Lock Out (UVLO) operation.
- The VFO output is open drain configured. The VFO signal line should be pulled up to the 5 V logic power supply with approximately 10 kΩ resistance.

Pin: CFOD

- Input pin for duration time control of fault-out.
- The duration time of fault-out depends on the capacitance between CFOD and VSS pins.

Pin: TH1, TH2

- For case temperature (Tc) detection, this pin should be connected to an external series resistor.
- The external series resistor should be selected to meet the detection range matched for the specification of each application (for details, refer to Figure 19).

Pin: VTS

- Analog temperature sensing output pin.
- This is to indicate the temperature of LVIC with analog voltage. LVIC itself creates some power loss, but mainly heat generated from the MOSFETs will increase the temperature of the LVIC.
- VTS versus temperature characteristics is illustrated in Figure 15.

Pin: P

- Positive DC-link pin.
- This is the DC-link positive power supply pin of the inverter.
- It is internally connected to the drains of the high-side MOSFETs.
- To suppress surge voltage caused by the DC-link wiring or PCB pattern inductance, connect a smoothing filter capacitor close to this pin (tip: metal film capacitor is typically used).

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Pins: NU, NV, NW

- Negative DC-link pins.
- These are the DC-link negative power supply pins (power ground) of the inverter.
- These pins are connected to the low-side MOSFET sources of each phase.
- These pins are used to connect one shunt resistor or three shunt resistors for current sensing.

Pins: U, V, W

- Inverter power output pins.
- Inverter output pins for connecting to the inverter load (e.g. motor).

PACKAGE

Package Structure

Since heat dissipation is an important factor limiting the power module's current capability, the heat dissipation characteristics of a package are important in determining the performance. A trade-off exists among heat dissipation characteristics, package size, and isolation characteristics. The key to a good package technology lies in the optimization package size while maintaining outstanding heat dissipation characteristics without compromising the isolation rating.

In SPM 31, technology was developed with DBC substrate that resulted in excellent heat dissipation characteristics. This technology made it possible to achieve improved reliability and heat dissipation. Power chips are attached directly to the DBC substrate.

Figure 5 and Figure 6 show the package outline and the cross-sections of the SPM 31 package.

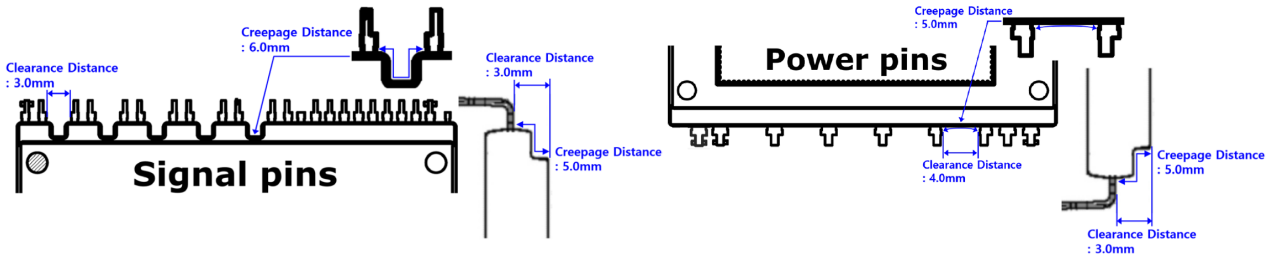

Figure 5. Isolation Distance for Signal Pins, Power Pins and Pins to Heatsink

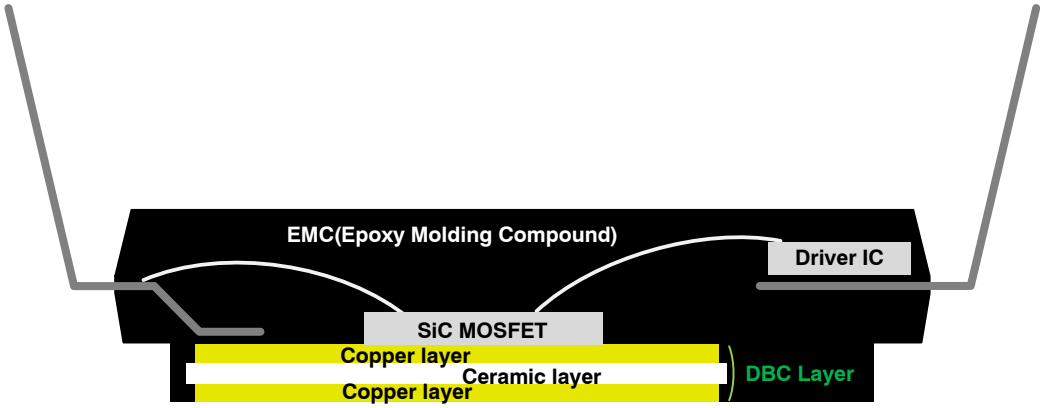

Figure 6. Package Structure and Cross Section for SPM 31

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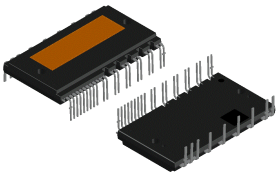
Package Outline

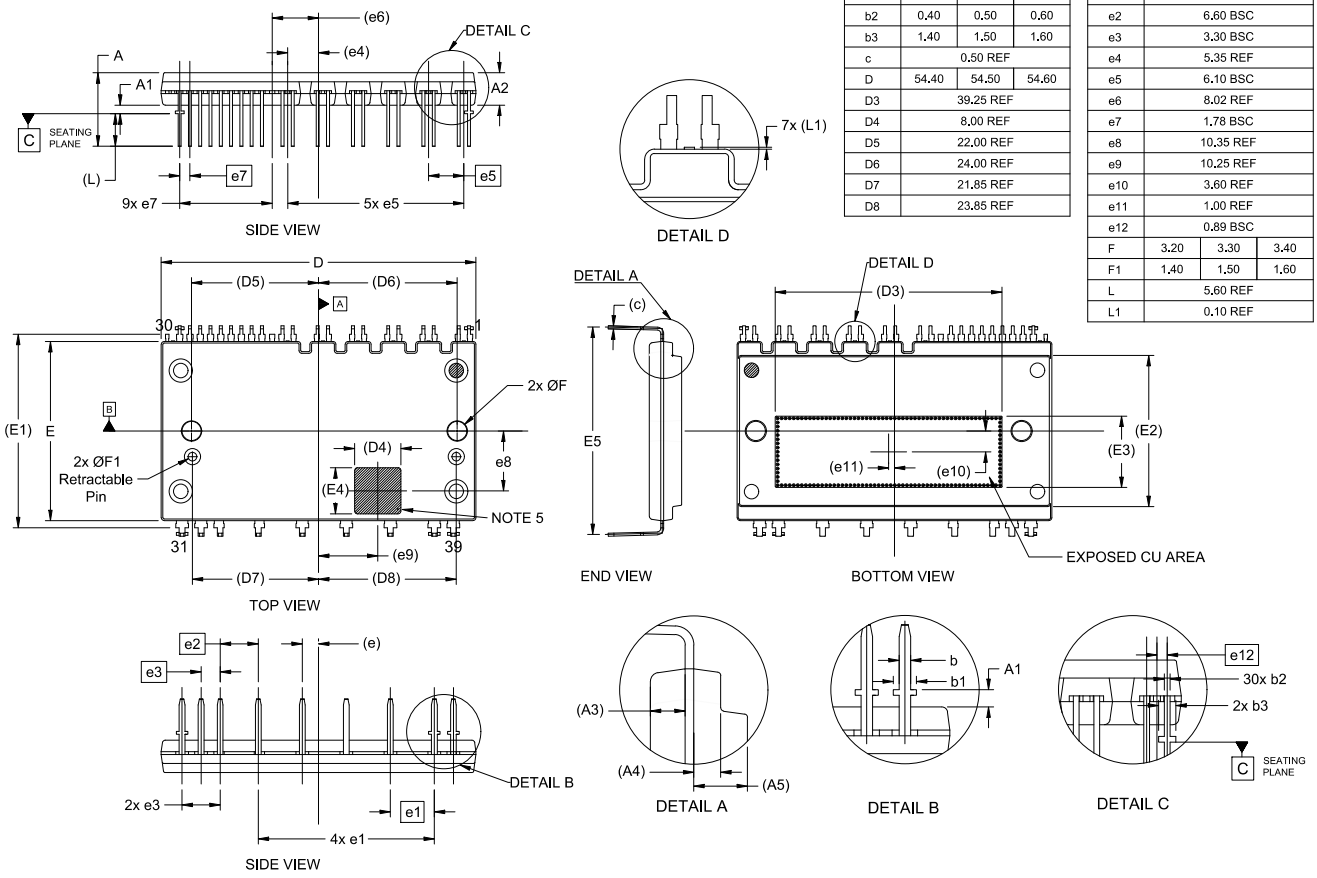


DIP39, 54.50x31.00x5.60, 1.78P
CASE MODGC
ISSUE C

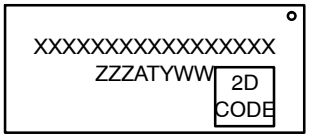
NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b and c APPLY TO THE PLATED LEADS AND ARE MEASURED BETWEEN 1.00 AND 2.00 FROM THE LEAD TIP
4. POSITION OF THE LEAD IS DETERMINED AT THE BASE OF THE LEAD WHERE IT EXITS THE PACKAGE BODY
5. AREA FOR 2D BAR CODE
6. SHORTENED/CUT PINS ARE 2,5,8,11,14,17,19,29 AND 30
7. DIMENSIONS "D" AND "E" DO NOT INCLUDE THE SIDE FLASH PROTRUSION WHICH IS ~0.12 FOR EACH SIDE

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	12.20	12.7	13.2
A1	1.00	1.50	2.00
A2	5.50	5.60	5.70
A3		2.00 REF	
A4		1.55 REF	
A5		3.10 REF	
b	0.90	1.00	1.10
b1	1.90	2.00	2.10
b2	0.40	0.50	0.60
b3	1.40	1.50	1.60
c		0.50 REF	
D	54.40	54.50	54.60
D3		39.25 REF	
D4		8.00 REF	
D5		22.00 REF	
D6		24.00 REF	
D7		21.85 REF	
D8		23.85 REF	

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E	30.90	31.00	31.10
E1		33.50 REF	
E2		26.14 REF	
E3		12.35 REF	
E4		8.00 REF	
E5	35.40	35.90	36.40
e		2.81 REF	
e1		7.62 BSC	
e2		6.60 BSC	
e3		3.30 BSC	
e4		5.35 REF	
e5		6.10 BSC	
e6		8.02 REF	
e7		1.78 BSC	
e8		10.35 REF	
e9		10.25 REF	
e10		3.60 REF	
e11		1.00 REF	
e12		0.89 BSC	
F	3.20	3.30	3.40
F1	1.40	1.50	1.60
L		5.60 REF	
L1		0.10 REF	



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
ZZZ = Assembly Lot Code
AT = Assembly & Test Location
Y = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “ ▪”, may or may not be present. Some products may not follow the Generic Marking.

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PRODUCT SYNOPSIS

Absolute maximum ratings, electric characteristics, recommended operating conditions and mechanical characteristics are focused on in this section. Please refer to respective datasheets for the detailed description of each product

ABSOLUTE MAXIMUM RATING (Tj = 25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Rating	Unit
INVERTER PART (BASE ON NFAM2512SCBUT)				
VPN	Supply Voltage	Applied between P – NU, NV, NW	900	V
VPN(surge)	Supply Voltage (Surge)	Applied between P – NU, NV, NW (Note 4)	1000	
VDS	Drain – Source Voltage		1200	
ID	Each MOSFET Drain Current	Tc = 25 °C, Tj ≤ 150 °C	±70	A
IDP	Each MOSFET Drain Current (Peak)	Tc = 25 °C, Tj ≤ 150 °C, Under 1 ms Pulse Width	±140	
PD	Power Dissipation	Tc = 25 °C per One Chip (Note 5)	187	W
Tj	Operating Junction Temperature		−40~175	°C
CONTROL PART				
VDD	Control Supply Voltage	Applied between VDD(XX) – VSS	20	V
VBS	High-Side Control Bias Voltage	Applied between VB(X) – VS(X)	20	
VIN	Input Signal Voltage	Applied between HIN(X), LIN(X) – VSS	−0.3 ~ VDD + 0.3	
VFO	Fault Output Supply Voltage	Applied between VFO – VSS	−0.3 ~ VDD + 0.3	
IFO	Fault Output Current	Sink Current at VFO Pin	2	mA
VCIN	Current Sensing Input Voltage	Applied between CIN – VSS	−0.3 ~ VDD + 0.3	V
BOOTSTRAP DIODE PART				
VRRM	Maximum Repetitive Reverse Voltage		1200	V
Tj	Operating Junction Temperature		−40~175	°C
TOTAL SYSTEM				
VPN(PROT)	Self-Protection Supply Voltage Limit (Short-Circuit Protection Capability)	VDD(XX), VB(X) = 13.5 ~ 18.0 V, Tj = 150 °C, (Non-Repetitive, < 2 μs)	800	V
Tc	Case Operation Temperature	See Figure 7	−40~125	°C
Tstg	Storage Temperature		−40~125	
Viso	Isolation Voltage	60 Hz, Sinusoidal, 1-minute, Connect Pins to Heat Sink	2500	V rms

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Rth(j-c)T	Junction to Case Thermal Resistance (Note 6)	SiC MOSFET Part (per 1/6 Module)	–	–	0.80	°C/W

4. Surge voltage developed by the switching operation due to the wiring inductance between P and NU, NV, NW terminals.
5. Calculation value considered to design factor.
6. For the measurement point of case temperature (Tc), please refer to Figure 7.

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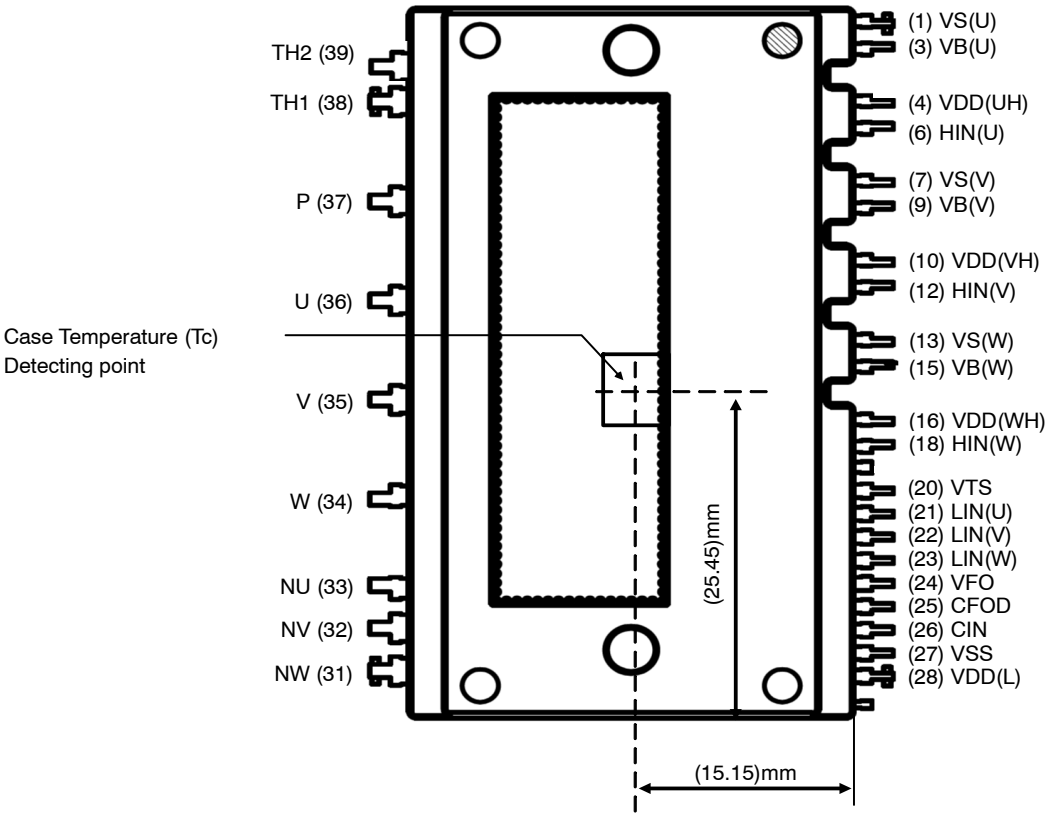

Figure 7. Case Temperature (Tc) Detecting Point

ELECTRICAL CHARACTERISTIC (VDD = 18 V and T_J = 25 °C, unless otherwise noted)

Symbol		Parameter	Condition		Min	Typ	Max	Unit
INVERTER PART (BASE ON NFAM2512SCBUT)								
IDSS		Drain – Source Leakage Current	VDS = 1200 V, Tj = 25 °C				1	mA
			VDS = 1200 V, Tj = 150 °C				10	mA
RDS(ON)		Drain – Source On Resistance	ID = 60 A, VDD = VBS = 18 V, Tj = 25 °C			25	35	mΩ
			ID = 60 A, VDD = VBS = 18 V, Tj = 150 °C			45		mΩ
VSD		Diode Forward Voltage	ISD = 60 A, VDD = VBS = 18 V, Tj = 25 °C	HIN/LIN = OFF		4.45	5.20	V
				HIN/LIN = ON		1.35		V
			ISD = 60 A, VDD = VBS = 18 V, Tj = 150 °C	HIN/LIN = OFF		4.85		V
				HIN/LIN = ON		2.35		V
Switching Times	ton	High Side Switching Times	VPN = 600 V, VDD(XX) = 18 V, VBS(X) = 18 V, ID = 60 A, Tj = 25 °C, HIN(X) = 0 V ↔ 5 V, Inductive Load (Note 7) See Figure 8		0.55	0.83	1.45	μs
	tc(on)					0.13	0.45	μs
	toff					1.15	1.65	μs
	tc(off)					0.16	0.20	μs
	trr					0.10		μs
Eon	Turn-on Switching loss		ID = 60 A, VPN = 600 V, Tj = 25 °C			2.45		mJ
Eoff	Turn-off Switching loss					2.45		mJ

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ELECTRICAL CHARACTERISTIC (VDD = 18 V and T_J = 25 °C, unless otherwise noted) (continued)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
INVERTER PART (BASE ON NFAM2512SCBUT)							
Eon	Turn-on Switching loss	ID = 60 A, VPN = 600 V, Tj = 150 °C			2.35		mJ
Eoff	Turn-off Switching loss				2.95		mJ
Erec	Diode Reverse Recovery Energy	ISD = 60 A, VPN = 600 V, (di/dt set by internal driver)	Tj = 25 °C		0.22		mJ
			Tj = 150 °C		0.27		mJ
BOOTSTRAP CIRCUIT PART							
VF	Forward Voltage	IF = 0.1 A, Tj = 25 °C		2.1	2.5	2.9	V
RBOOT	Built-in Limiting Resistance			12.5	15.5	18.5	Ω
CONTROL PART							
IQDDH	Quiescent VDD Supply Current	VDD(xH) = 18 V, HIN(X), LIN(X) = 0 V	VDD(xH) – VSS			0.3	mA
IQDDL		VDD(L) = 18 V, HIN(X), LIN(X) = 0 V	VDD(L) – VSS			2.5	mA
IPDDH	Operating VDD Supply Current	VDD(xH) = 18 V, fPWM = 60 kHz, duty = 50%, applied to one PWM Signal Input for High-Side	VDD(xH) – VSS			0.4	mA
IPDDL		VDD(xH) = 18 V, fPWM = 60 kHz, duty = 50%, applied to one PWM Signal Input for Low-Side	VDD(L) – VSS			6.0	mA
IQBS	Quiescent VBS Supply Current	VB(X) – VS(X) = 18 V, HIN (X) = 0 V	VB(X) – VS(X)			0.4	mA
IPBS	Operating VBS Supply Current	VDD(xH) = 18 V, VB(X) – VS(X) = 18 V, fPWM = 60 kHz, duty=50%, applied to one PWM Signal Input for High-Side	VB(X) – VS(X)			4.0	mA
VFOH	Fault Output Voltage	CIN = 0 V, 10 kΩ Pulled up to 5 V		4.9			V
VFOL		CIN = 1 V, 10 kΩ Pulled up to 5 V				0.95	
VCIN(ref)	Over Current Trip Level (Note 8)	VDD = 18 V	CIN – VSS	0.46	0.48	0.50	V
UVDDD	Supply Circuit, Under-Voltage Protection	Detection Level		10.3		12.5	V
UVDDR		Reset Level		10.8		13.0	
UVBSD		Detection Level		10.0		12.0	
UVBSR		Reset Level		10.5		12.5	
tFOD	Fault-Out Pulse Width	CFOD = 22 nF (Note 9)		1.6	2.2		ms
VTS	Voltage Output for LVIC Temperature Sensing Unit (Note 10)	Pull down R = 5.1 kΩ, Temp. = 85 °C		2.50	2.63	2.76	V
VIN(ON)	ON Threshold Voltage	Applied between HIN(X), LIN(X) – VSS				2.6	V
VIN(OFF)	OFF Threshold Voltage			0.8			

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

7. ton and toff include the propagation delay time of the internal drive IC. tc(on) and tc(off) are the switching time of MOSFET itself under the given gate driving condition internally. For the detailed information, please see and Figure 8.
8. Short-circuit current protection is functioning only at the low-sides.
9. The fault-out pulse width tFOD depends on the capacitance value of CFOD according to the following approximate equation: The fault-out pulse width tFOD = 0.1 x 10^6 x CFOD [s].
10. TLVIC is the temperature of LVIC itself. VTS is only for sensing temperature of LVIC and cannot shutdown MOSFETs automatically.

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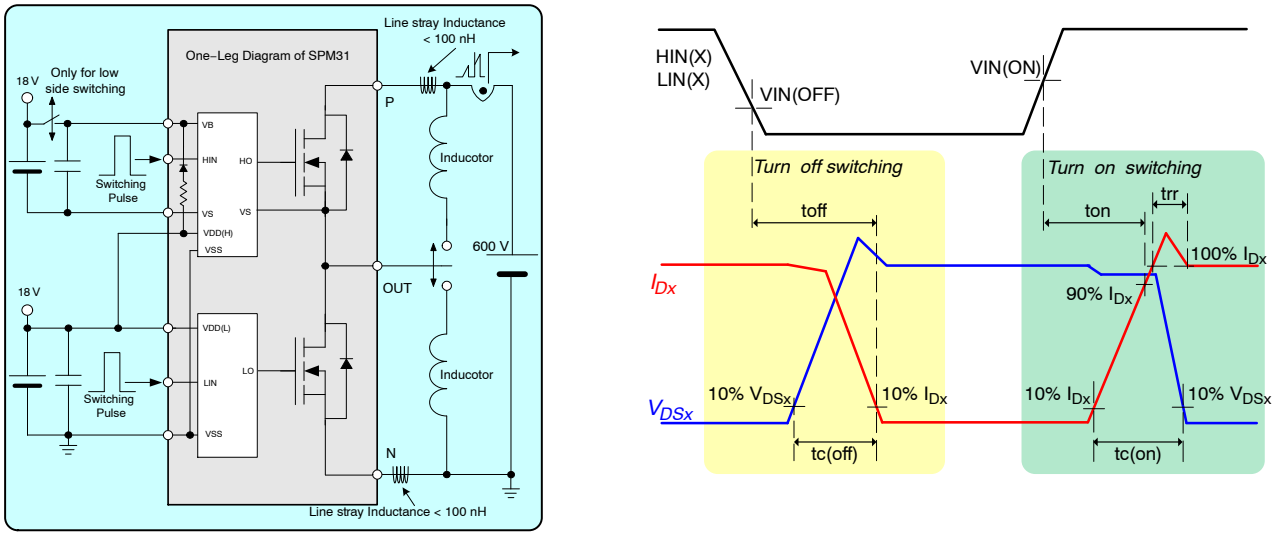

Figure 8. Switching Evaluation Circuit and Switching Time Definition

RECOMMENDED OPERATING CONDITIONS (Base on NFAM2512SCBUT)

Symbol	Parameter	Condition		Min	Typ	Max	Unit
VPN	Supply Voltage	Applied between P – N_x		–	600	800	V
VDD	Control Supply Voltages	Applied between VDD(XH) – VSS		13.0	18.0	19.0	
VBS	High – Side Bias Voltage	Applied between VB(X) – VS(X)		13.5	18.0	19.5	
dVDD / dt, dVBS / dt	Supply Voltage Variation			−1	–	1	V/μs
DT	Blanking Time for Preventing Arm – Short	For Each Input Signal		1.0	–	–	μs
fPWM	PWM Frequency	−40 °C ≤ Tc ≤ 125 °C, −40 °C ≤ Tj ≤ 150 °C			–	60	kHz
Io	Allowable r.m.s Current (Note 11)	VPN = 600 V, VDD = VBS = 18 V, P.F = 0.8, Tc ≤ 125 °C, Tj ≤ 150 °C	fPWM = 5 kHz	–	–	34.0	Arms
			fPWM = 15 kHz			28.0	Arms
			fPWM = 30 kHz	–	–	21.5	Arms
PWIN(ON)	Minimum Input Pulse Width (Note 12)	VDD = VBS = 18 V, Wiring Inductance between NU, NV, NW and DC Link N < 10 nH		1.0	–	–	μs
PWIN(OFF)				1.0	–	–	
Package Mounting Torque		M3 Type Screw		0.6	0.7	0.9	Nm

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

11. Allowable output current value is the reference data for the safe operation of this product. This may be different from the actual application and operating conditions.
12. Product might not make response if input pulse width is less than the recommended value.

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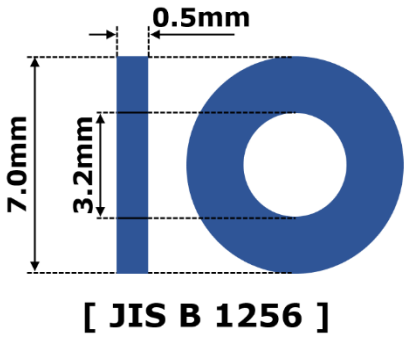
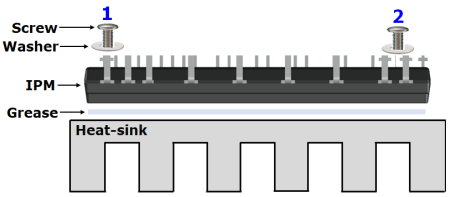
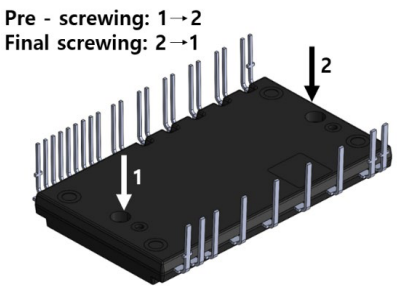
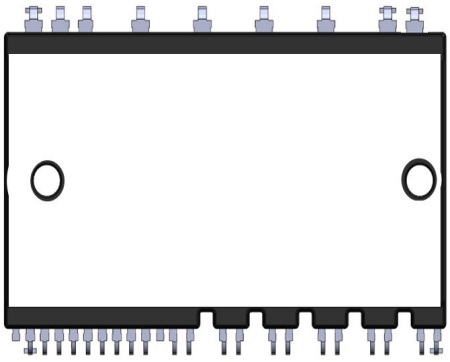
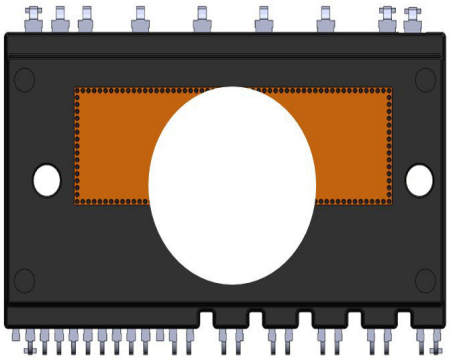
MECHANICAL CHARACTERISTICS

Item	Recommended Conditions
Pitch	46.0 ± 0.1 mm (Please refer to Package Outline Diagram)
Screw	Diameter: M3 Screw head types: pan head, truss head, binding head
Washer	Plane washer dimensions  [JIS B 1256]
Heat Sink	Material: Aluminum or Copper Warpage (the surface that contacts IPM): −50 to 100 μm No contamination on the heat sink surface that contacts IPM
Torque	Pre. tightening: 0.2 ~ 0.3 Nm on first screw Pre. tightening: 0.2 ~ 0.3 Nm on second screw Pre. tightening: 0.6 ~ 0.9 Nm on first screw Pre. tightening: 0.6 ~ 0.9 Nm on second screw  
Grease	Silicone grease. Thickness: 100 to 200 μm Uniformly apply silicon grease on whole IPM TOP surface. Thermal foils are only recommended after careful evaluation. Thickness, stiffness and compressibility parameters have a strong influence on performance.  Recommended  Do not recommended

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OPERATION SEQUENCE FOR PROTECTIONS

Short Circuit Protection

The 1200 V SPM 31 series use external shunt resistor for the short circuit current detection, as shown in Figure 9. The LVIC has a built-in short-circuit current protection function that senses the voltage to the CIN pin. If this voltage (VCIN) exceeds the VCIN(ref) (the threshold voltage trip level of over current protection) specified in the device datasheets (VCIN(ref), typ. is 0.48 V), a fault signal is asserted and all three lower side MOSFETs are turned off. Short circuit is included to over current situation.

Typically, the maximum short-circuit current magnitude is gate-voltage dependent: higher gate voltage (VDD and VBS) is resulted in a larger short-circuit current. To avoid potential problems, the maximum short-circuit trip level is set below 1.5 times the nominal rated drain current. The LVIC over current protection-timing chart is shown in Figure 10.

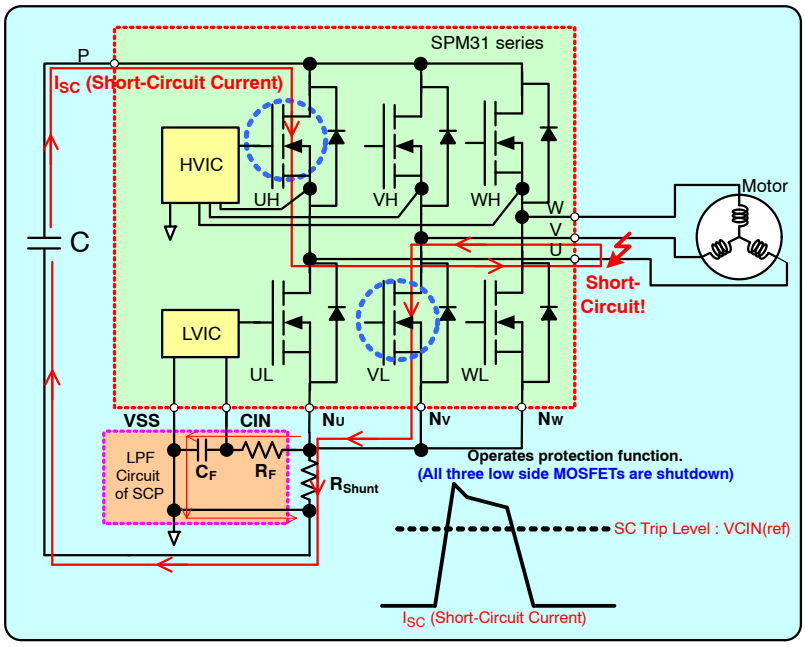

Figure 9. Operation of Short-Circuit Protection

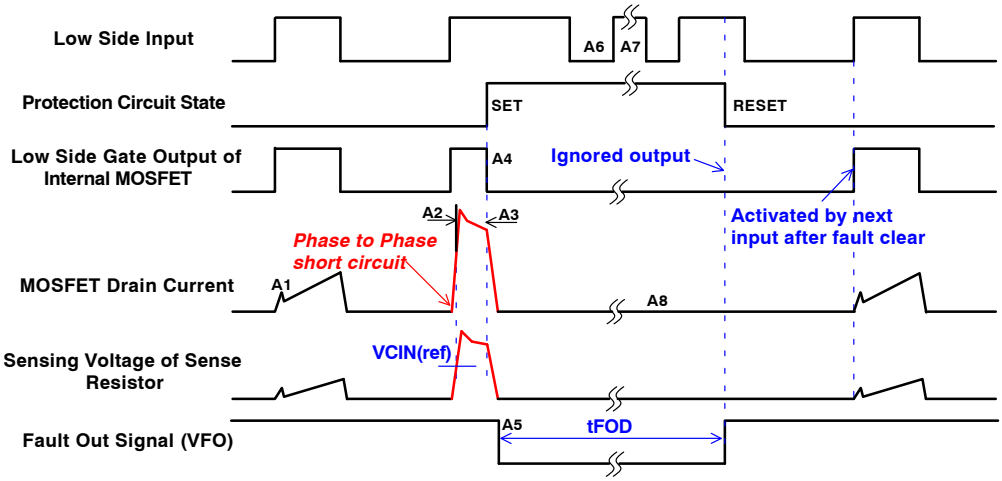

Figure 10. Timing Chart of Short-Circuit Protection Function

13. A1−Normal operation: MOSFETs turn on and carrying current.
14. A2−Short circuit current detection (SC trigger).
15. A3−All low-side MOSFET's gate are hard interrupted.
16. A4−All low side MOSFETs turn off.
17. A5−Fault output timer operation start with internal delay, (Typ. 2.2 ms, CFOD = 22 nF), Fault-out duration time is controlled by CIN.
18. A6−Input "L": Low side MOSFETs OFF state.
19. A7−Input "H": Low side MOSFETs input ON state, but during the active period of fault output the MOSFET doesn't turn ON.
20. A8−Low side MOSFETs keeps OFF state.

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Under-Voltage Lock Out Protection

The LVIC has an Under-Voltage Lock Out protection (UVLO) function to protect the low-side MOSFETs from operation with insufficient gate driving voltage. A timing chart for this protection is shown in Figure 11.

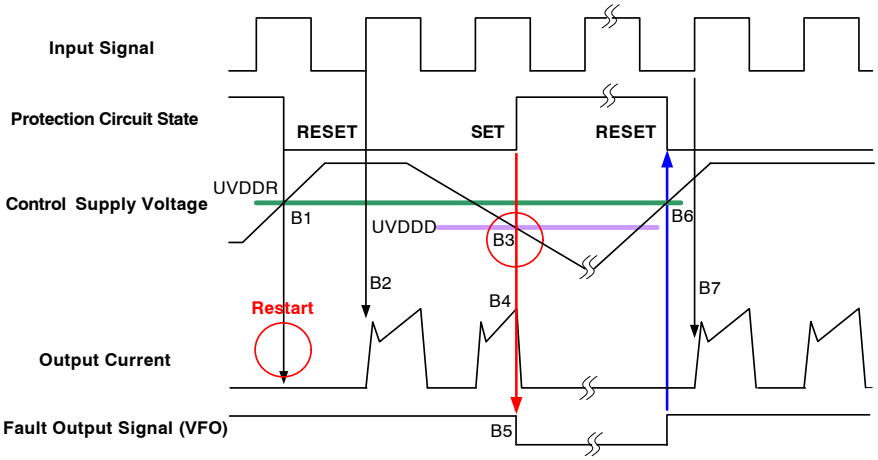

Figure 11. Timing Chart of Low-side Under-Voltage Lock Out Protection

21. B1−Control supply voltage rise: after the voltage rises UVDDR, the circuits start to operate when the next input is applied.
22. B2−Normal operation: MOSFET ON and carrying current.
23. B3−Under-voltage detection (UVDDD).
24. B4−MOSFET OFF in spite of control input is alive.
25. B5−Fault output signal starts.
26. B6−Under-voltage reset (UVDDR).
27. B7−Normal operation: MOSFET ON and carrying current. If fault-out duration (tFOD) by external capacitor at CIN pin is longer than UVDDD timing, fault output and MOSFET state are cleared after tFOD.

The HVIC has an under-voltage lockout function to protect the high-side MOSFET from insufficient gate driving voltage. A timing chart for this protection is shown in Figure 12. A fault-out (VFO) alarm is not given for low at HVIC bias conditions.

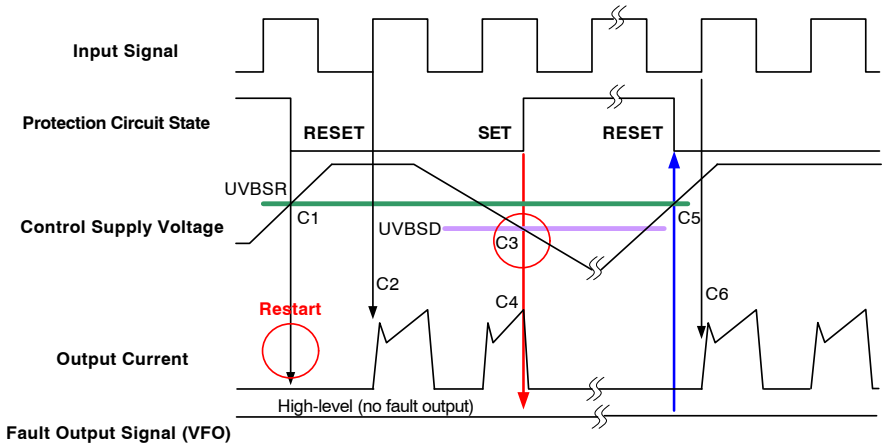

Figure 12. Timing Chart of High-Side Under-Voltage Protection Function

28. C1−Control supply voltage rises: after the voltage reaches UVBSR, the circuit starts when the next input is applied.
29. C2−Normal operation: MOSFET ON and carrying current.
30. C3−Under-voltage detection (UVBSD).
31. C4−MOSFET OFF in spite of control input is alive, but there is no fault output signal.
32. C5−Under-voltage reset (UVBSR).
33. C6−Normal operation: MOSFET ON and carrying current.

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Table 3. THE IPM OPERATING BEHAVIOR VERSUS CONTROL SUPPLY VOLTAGE

Control Supply Voltage [V]	Operating Behavior
0 ~ 4	Built in control IC does not operate. MOSFET and protection function does not work. Normally, unexpected malfunction can be happened by external noise. To prevent malfunction, the control power voltage must be charged to 4 V before the DC link voltage reaches approximately 200 ~ 250 V.
4 ~ UVDDD , UVBSD	Undervoltage protection is activated and output FO is generated. Even if control signals are applied, MOSFETs does not work.
UVDD ~ 13.0 UVBS ~ 13.5	MOSFETs can be operated. However, conducting and switching losses will be increased.
13.0 ~ 19.0 for VDD 13.5 ~ 19.5 for VBS	Normal operation and Recommended conditions.
19.0 ~ 20.0 for VDD 19.5 ~ 20.0 for VBS	MOSFETs can be operated. Its switching speed is faster at this range. The saturation current is larger and short circuit broken risk can be increased.
Over 20.0	Control circuit might be destroyed.

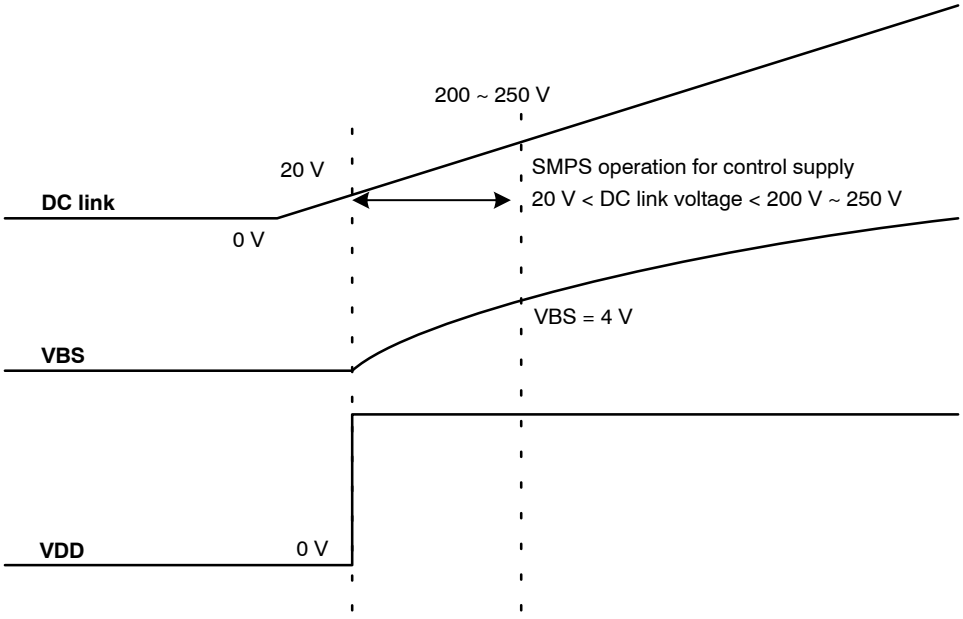

Figure 13. Recommended Power On Sequence

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KEY PARAMETER DESIGN GUIDANCE

For stable operation, there are recommended parameters for passive components and bias conditions, considering operating characteristics of the 1200 V SPM 31 series. This section focuses on the key parameter design guidance.

Circuit of VTS

The Thermal Sensing Unit(VTS) analog voltage output reflects the temperature of the LVIC in 1200 V SPM 31 series products. The relationship between VTS output voltage and LVIC temperature is shown in Figure 15. It does not have any self-protection function, and, therefore, it should be used appropriately based on application requirement. It should be noted that there is a time lag from MOSFET temperature to LVIC temperature. It is very difficult to respond quickly when temperature rises sharply in a transient condition such as shoot-through event. Even though VTS has some limitation, it will be definitely useful in enhancing the system reliability.

Figure 14 shows the LVIC location for VTS function of SPM 31 series and Figure 15 shows that the relationship between VTS voltage and LVIC temperature.

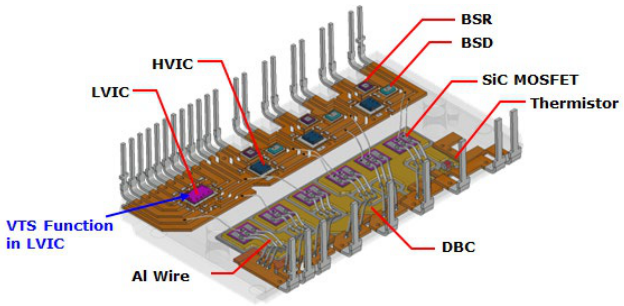

Figure 14. Location of VTS Function (LVIC)

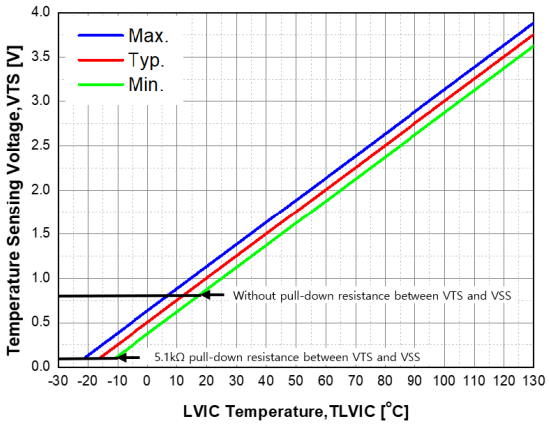

Figure 15. Temperature vs. VTS

Figure 16 shows the equivalent circuit diagram of VTS inside LVIC and a typical application diagram. This output voltage is clamped to 5.2 V by an internal Zener diode, but in case the maximum input range of Analog to Digital converter of MCU is below 5.2 V. An amplifier can be used to change the range of voltage input to MCU to have better resolution of the temperature. It is recommended to add 5.1 kΩ pull-down resistance between VTS and VSS (Signal Ground) as described Figure 16 for linear output characteristics at low temperature. In case of removing pull down resistance between VTS and VSS, VTS output voltage is saturated at 0.8 V and it is normally used under operation conditions over room temperature. To make VTS more stable, a ceramic capacitance of 10 nF is recommended between VTS and VSS as well.

Relationship of VTS and TLVIC can be expressed as the following equation.

$$VTS,_{Min} = 0.025 \times T_{LVIC} + 0.375\ [V]$$

$$VTS,_{Typ} = 0.025 \times T_{LVIC} + 0.505\ [V]$$

$$VTS,_{Max} = 0.025 \times T_{LVIC} + 0.635\ [V]$$

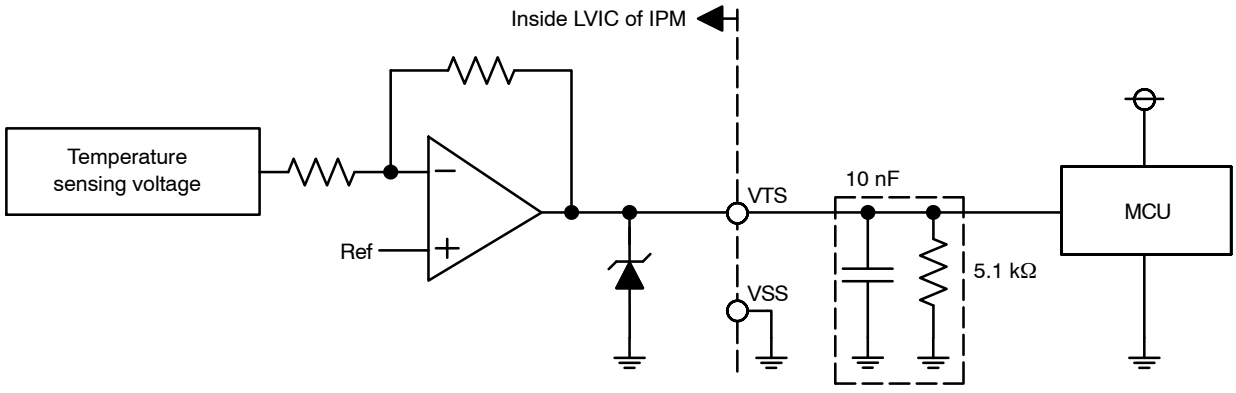

Figure 16. Internal Block Diagram and Interface Circuit of VTS

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Circuit of NTC Thermistor (Monitoring of Tc)

The SPM31 series includes a negative temperature coefficient (NTC) thermistor for module case temperature (Tc) sensing. This thermistor is located in DBC substrate with the power chip (SiC MOSFET). Therefore, the thermistor can accurately reflect the temperature of the power chip. Normally, circuit designers use two kinds of circuit for temperature protection (monitoring) by NTC thermistor. One is circuit by Analog-Digital Converter (ADC). The other is circuit by comparator. Figure 17 shows examples of application circuits with an NTC thermistor.

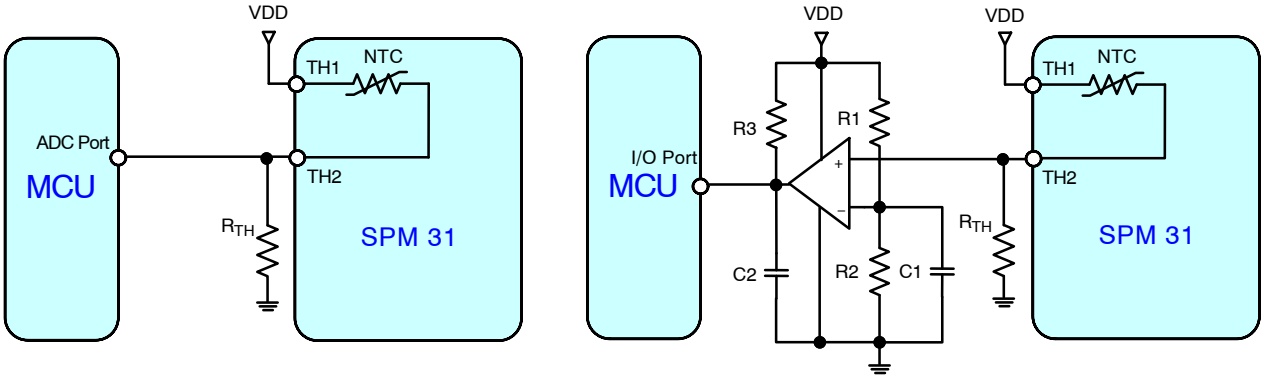

Figure 17. Over Temperature Protection Circuit by MCU and Comparator

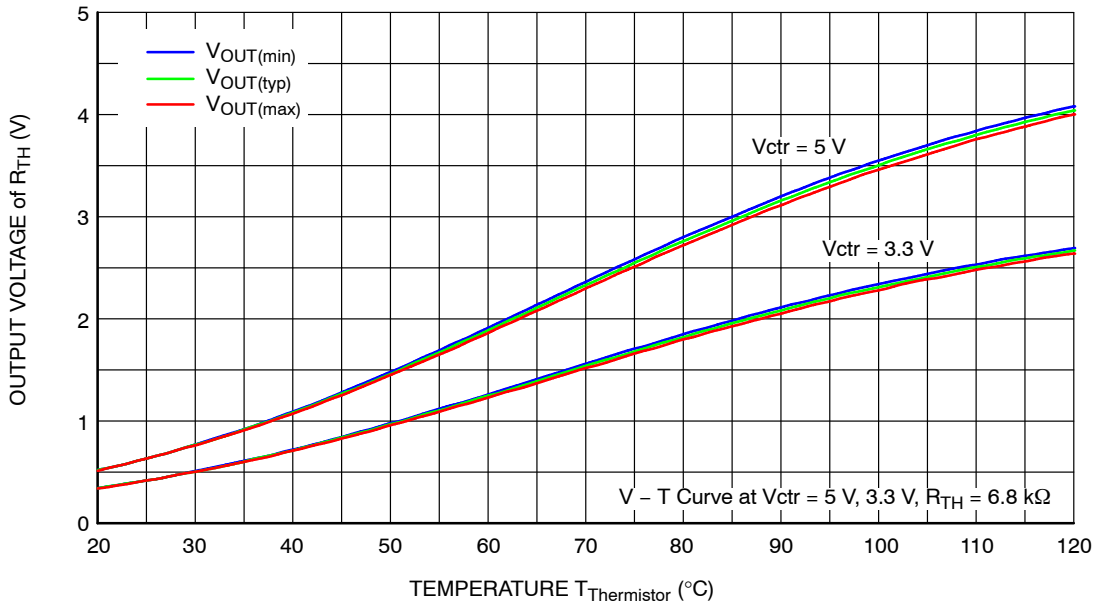

Figure 18. V – T Curve of Figure 17.

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Table 4. THERMISTOR CHARACTERISTICS (BUILT-IN ONLY IN – T TYPE)

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
Resistance	R_{25}	Tc = 25 °C	46.530	47	47.47	kΩ
Resistance	R_{125}	Tc = 125 °C	1.344	1.406	1.471	kΩ
B-Constant (25-50 °C)		B	4009.5	4050	4090.5	K
Temperature Range			–40		+125	°C

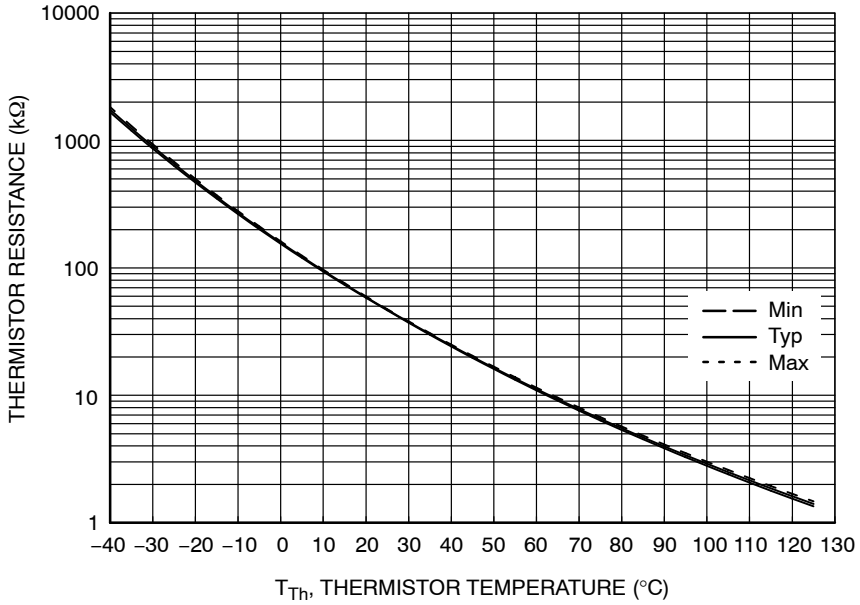

Figure 19. Thermistor Resistance versus Thermistor Temperature Tth

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Table 5. R-T TABLE OF NTC THERMISTOR

T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)	T_{NTC} (°C)	R_{min} (kΩ)	R_{cent} (kΩ)	R_{max} (kΩ)
0	153.8063	158.2144	162.7327	42	22.1759	22.6466	23.1249	85	4.4694	4.6736	4.8866
1	146.0956	150.1651	154.3326	43	21.2753	21.7401	22.2129	86	4.3228	4.5226	4.731
2	138.8168	142.5725	146.4152	44	20.4158	20.8746	21.3416	87	4.1817	4.3771	4.5811
3	131.9431	135.4081	138.9502	45	19.5953	20.0478	20.5088	88	4.0459	4.2369	4.4366
4	125.4497	128.6453	131.9091	46	18.812	19.258	19.7126	89	3.915	4.1019	4.2973
5	119.3135	122.2594	125.2655	47	18.0638	18.5032	18.9514	90	3.789	3.9717	4.1629
6	113.5129	116.2273	118.9947	48	17.3492	17.7818	18.2234	91	3.6675	3.8463	4.0334
7	108.0276	110.5275	113.0739	49	16.6663	17.0921	17.5269	92	3.5505	3.7253	3.9084
8	102.8388	105.1398	107.4814	50	16.0137	16.4325	16.8605	93	3.4377	3.6087	3.7879
9	97.9288	100.0454	102.1974	51	15.3899	15.8016	16.2227	94	3.329	3.4963	3.6716
10	93.2812	95.2267	97.2031	52	14.7934	15.1981	15.6122	95	3.2242	3.3878	3.5593
11	88.8803	90.6673	92.481	53	14.223	14.6205	15.0277	96	3.1235	3.2836	3.4515
12	84.7119	86.3519	88.0148	54	13.6773	14.0677	14.4678	97	3.0264	3.183	3.3473
13	80.7624	82.2661	83.7894	55	13.1552	13.5385	13.9316	98	2.9328	3.086	3.2468
14	77.019	78.3963	79.7903	56	12.6556	13.0318	13.4178	99	2.8425	2.9923	3.1497
15	73.47	74.7302	76.0043	57	12.1774	12.5465	12.9255	100	2.7553	2.9019	3.0559
16	70.1042	71.2558	72.4189	58	11.7195	12.0815	12.4536	101	2.6712	2.8146	2.9654
17	66.9112	67.962	69.0224	59	11.281	11.6361	12.0011	102	2.5901	2.7303	2.8779
18	63.8812	64.8386	65.8039	60	10.861	11.2091	11.5673	103	2.5117	2.6489	2.7933
19	61.005	61.8759	62.753	61	10.4594	10.8007	11.152	104	2.436	2.5703	2.7117
20	58.2739	59.0647	59.8601	62	10.0746	10.4091	10.7536	105	2.363	2.4943	2.6327
21	55.6798	56.3961	57.116	63	9.7058	10.0336	10.3714	106	2.2921	2.4206	2.556
22	53.2152	53.8628	54.5127	64	9.3522	9.6734	10.0046	107	2.2236	2.3493	2.4819
23	50.8732	51.4569	52.0422	65	9.0133	9.3279	9.6525	108	2.1575	2.2805	2.4102
24	48.6469	49.1715	49.6969	66	8.6882	8.9963	9.3145	109	2.0936	2.2139	2.3409
25	46.53	47	47.47	67	8.3764	8.6782	8.9899	110	2.0319	2.1496	2.2739
26	44.4567	44.936	45.4159	68	8.0773	8.3727	8.6782	111	1.9725	2.0877	2.2094
27	42.4868	42.9737	43.4618	69	7.7902	8.0795	8.3787	112	1.9151	2.0278	2.147
28	40.6147	41.1075	41.6021	70	7.5147	7.7979	8.091	113	1.8596	1.9699	2.0866
29	38.8351	39.3323	39.8319	71	7.2496	7.5268	7.8138	114	1.806	1.9139	2.0282
30	37.1428	37.6431	38.1463	72	6.995	7.2663	7.5474	115	1.7541	1.8598	1.9716
31	35.5329	36.0351	36.5408	73	6.7505	7.016	7.2913	116	1.7042	1.8076	1.9171
32	34.0011	34.5041	35.0111	74	6.5157	6.7755	7.045	117	1.6559	1.7572	1.8644
33	32.5433	33.0462	33.5534	75	6.2901	6.5443	6.8082	118	1.6092	1.7083	1.8134
34	31.1555	31.6573	32.164	76	6.0739	6.3227	6.581	119	1.564	1.6611	1.7639
35	29.834	30.3339	30.8392	77	5.8662	6.1096	6.3624	120	1.5203	1.6153	1.7161
36	28.576	29.0734	29.5764	78	5.6665	5.9046	6.1521	121	1.4777	1.5707	1.6694
37	27.3776	27.8717	28.372	79	5.4745	5.7075	5.9498	122	1.4365	1.5276	1.6242
38	26.2356	26.726	27.2228	80	5.2899	5.5178	5.7549	123	1.3966	1.4858	1.5804
39	25.1472	25.6332	26.1261	81	5.1129	5.3358	5.568	124	1.358	1.4453	1.538
40	24.1094	24.5907	25.0792	83	4.7788	4.9921	5.2145	125	1.3206	1.406	1.4969
41	23.1198	23.596	24.0796	84	4.6211	4.8299	5.0475	–	–	–	–

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Selection of Shunt Resistor

Figure 20 shows an example circuit of the short circuit protection using 1-shunt resistor. The line current on the N side DC-ink is detected and the protective operation signal is passed through the RC filter. If the current exceeds the short circuit reference level, all the gates of the N-side three-phase MOSFETs are switched to the off state and the VFO fault signal is transmitted to MCU. Since short circuit protection is non-repetitive, MOSFET operation should be immediately halted when the VFO fault signal is given.

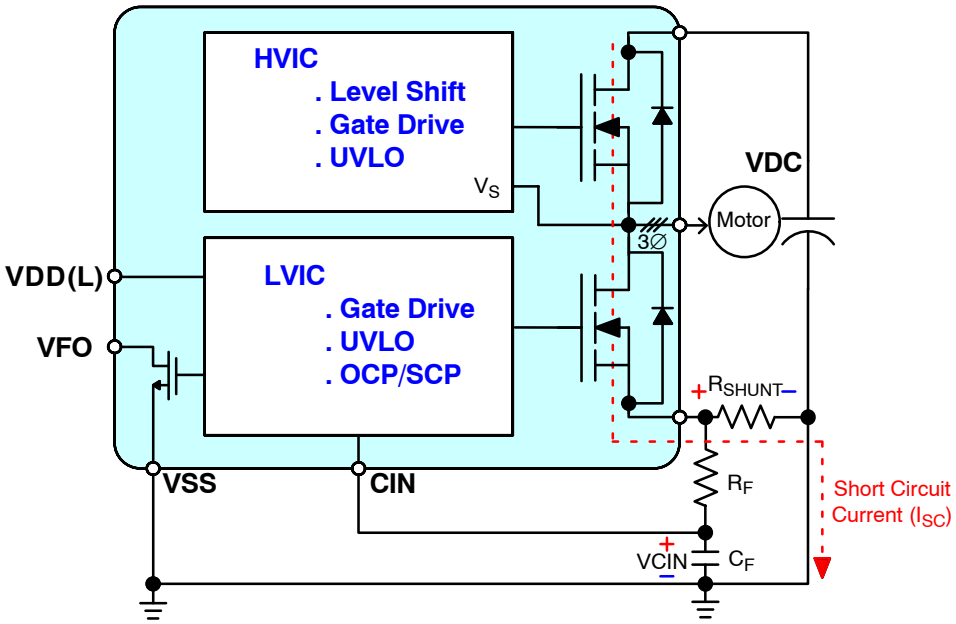

Figure 20. Short Circuit Current Protection Circuit with One Shunt Resistor

The value of shunt resistance is calculated by the following equation.

- Maximum Current Trip Level:
  - Depends on user selection:
  - $I_{SC(max)}$ = 1.5 × ID (Rated current)
- SC trip reference voltage:
  - Depends on datasheet
  - VCIN(ref) = Min. 0.46 V, Typ. 0.48 V, Max. 0.50 V
- Shunt resistance:
  - $I_{SC(max)} = VCIN(Ref.)_{_Max.} / R_{SHUNT(Min.)} \rightarrow R_{SHUNT(Min.)} = V_{SC(Max.)} / I_{SC(Max.)}$
- If the deviation of the shunt resistor should be limited below ±5%,
  - $R_{SHUNT(typ)} = VCIN(Ref.)_{_Typ.} / I_{SC(max)}$,
  - $R_{SHUNT(Min.)} = R_{SHUNT(Typ.)} \times 0.95$,
  - $R_{SHUNT(Max.)} = R_{SHUNT(Typ.)} \times 1.05$
- Actual short circuit trip current level becomes:
  - $I_{SC(Typ.)} = VCIN(Ref)_{_Typ.} / R_{SHUNT(Typ.)}$
  - $I_{SC(Min.)} = V_{SC(Min.)} / R_{SHUNT(Max.)}$
- Inverter output power:
  - $P_{OUT} = \sqrt{3} \times VO, LL \times I_{O(RMS)} \times PF$

  Where:
  - $VO, LL = \frac{\sqrt{3}}{\sqrt{2}} \times MI \times \frac{V_{DC}}{2}$
  - $I_{O(RMS)}$ = Maximum load current of inverter
  - M.I = Modulation Index
  - VDC = DC link voltage
  - PF = Power Factor

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- Average DC Current
  - $I_{DC_AVG} = (P_{out} \times Eff) / V_{DC_Link}$

  Where:
  - Eff = Inverter Efficiency
- The power rating of shunt resistor is calculated by the following equation
  - $P_{SHUNT} = (I_{RMS}^2 \times R_{SHUNT} \times Margin) / De\text{-}rating\ Ratio$

  Where:
  - R_{SHUNT} is shunt resistance typical value at Tc = 25 °C
  - De-rating ratio is ratio of shunt resistor at T_{SHUNT} = 100 °C (From datasheet of shunt resistor)
  - Margin is safety margin (Determine by user)
- Shunt resistor calculation examples:
  - Calculation conditions:
  - DUT: NFAM2512SCBUT
  - Tolerance of shunt resistor: ±5 %
  - SC Trip Reference Voltage, VCIN(ref):
  - $VCIN(ref)_{_Min.}$ = 0.46 V, $VCIN(ref)_{_Typ.}$ = 0.48V, $VCIN(ref)_{_Max.}$ = 0.50 V
  - Maximum Load Current of Inverter (I_{RMS}): 49.5 A_{rms}
  - Maximum Peak Load Current of Inverter (IC(max)): 105 A
  - Modulation Index(MI): 0.9
  - DC Link Voltage(VDC_Link): 600 V
  - Power Factor (PF): 0.8
  - Inverter Efficiency(Eff): 0.95
  - Shunt Resistor Value at Tc = 25 °C (R_{SHUNT}): 4.57 mΩ
  - De-rating Ration of Shunt Resistor at T_{SHUNT} = 100 °C: 70 % (refer to Figure 18)
  - Safety Margin: 20 %
  - Calculation results:
  - $I_{SC(Max.)}$: $1.5 \times I_{C(Max.)} = 1.5 \times 70$ A = 105 A
  - $R_{SHUNT(Typ.)}$: $VCIN(ref)_{_Typ.} / I_{SC(Max.)}$ = 0.48 V / 105 A = 4.57 mΩ
  - $R_{SHUNT(Max.)}$: $R_{SHUNT(Typ.)} \times 1.05 = 4.57\ m\Omega \times 1.05 = 4.79\ m\Omega$
  - $R_{SHUNT(Min.)}$: $R_{SHUNT(Typ.)} \times 0.95 = 4.57\ m\Omega \times 0.95 = 4.34\ m\Omega$
  - $I_{SC(Min.)}$: $VCIN(ref)_{_Min.} / R_{SHUNT(Max.)}$ = 0.46 V / 4.79 mΩ = 96.03 A
  - $I_{SC(Max.)}$: $VCIN(ref)_{_Max.} / R_{SHUNT(Min.)}$ = 0.5 V / 4.34 mΩ = 115.20 A
  - $P_{OUT} = \sqrt{3} \times \left(\frac{\sqrt{3}}{\sqrt{2}} \times MI \times V_{DC}\right) \times I_{0(RMS)} \times PF = \frac{3}{\sqrt{2}} \times 0.9 \times (600/2) \times 49.5 \times 0.8 = 22.681$ W
  - $I_{DC_AVG} = (P_{OUT} \times Eff) / V_{DC_Link}$ = 35.91 A
  - $P_{SHUNT} = (I_{DC}^2{}_{_AVG} \times R_{SHUNT} \times Margin) / De\text{-}rating\ Ratio = ((35.91)^2 \times 0.00457 \times 1.2) / 0.7$ = 10.10 W (therefore, the proper power rating of shunt resistor is over 10.10 W).

When over-current events are detected, the 1200 V SPM 31 series shuts down all low-side MOSFETs and sends out the fault-out (VFO) signal. FAULT output timer operation starts with internal delay (typ. 2.4 ms, CFOD = 22 nF), Fault-out duration time is controlled by CFOD.

To prevent malfunction, it is recommended that an RC filter is inserted between Nx and CIN pin. To shut down MOSFETs within 3 μs when over-current situation occurs, a time constant of 1.5 ~ 2 μs is recommended.

Table 6 shows the shunt resistance by typical current level of short-circuit protection for each product.

Table 6. OVER-CURRENT (OC) PROTECTION TRIP LEVEL

Device	R_{SHUNT}	Over Current Trip Level	Remark
NFAM5312SCBUT	8.00 mΩ	60 A	Typical value
NFAM3812SCBUT	6.40 mΩ	75 A	
NFAM2512SCBUT	4.57 mΩ	105 A	

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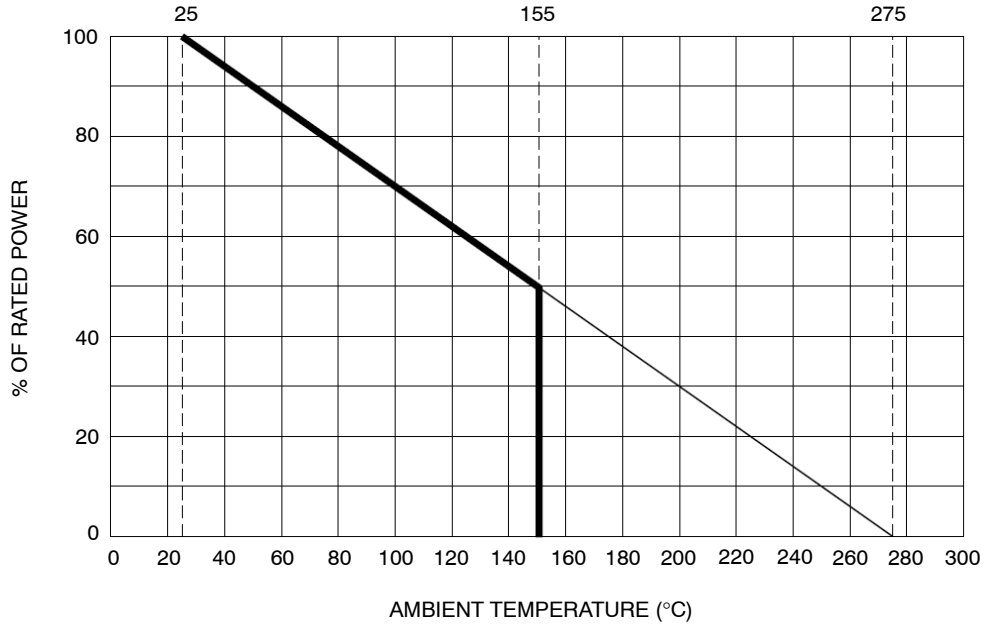

Figure 21. De-rating Curve Example of Shunt Resistor (from RARA Elec.)

Time Constant of Internal Delay

An RC filter prevents unexpected malfunction by related noise such as current protection and short circuit current protection (OCP, SCP) situation. The RC time constant is determined by the applied noise time and the Short-Circuit Withstanding Time (SCWT) of SPM 31 series. When the voltage of R_{shunt} exceeds the VCIN(ref) level, It is applied to the CIN pin via the RC filter. The RC filter delay is the time required for the CIN voltage to rise to the referenced over current protection level. The LVIC has an internal filter time (logic filter time for noise elimination: around 0.85 μs). User should consider this filter time when they design the RC filter between shunt resistor and CIN pin. Figure 22 shows timing diagram of over current protection and short circuit protection. Measured time is shown Table 7. User should be considering each time sections for distribution under protection situation.

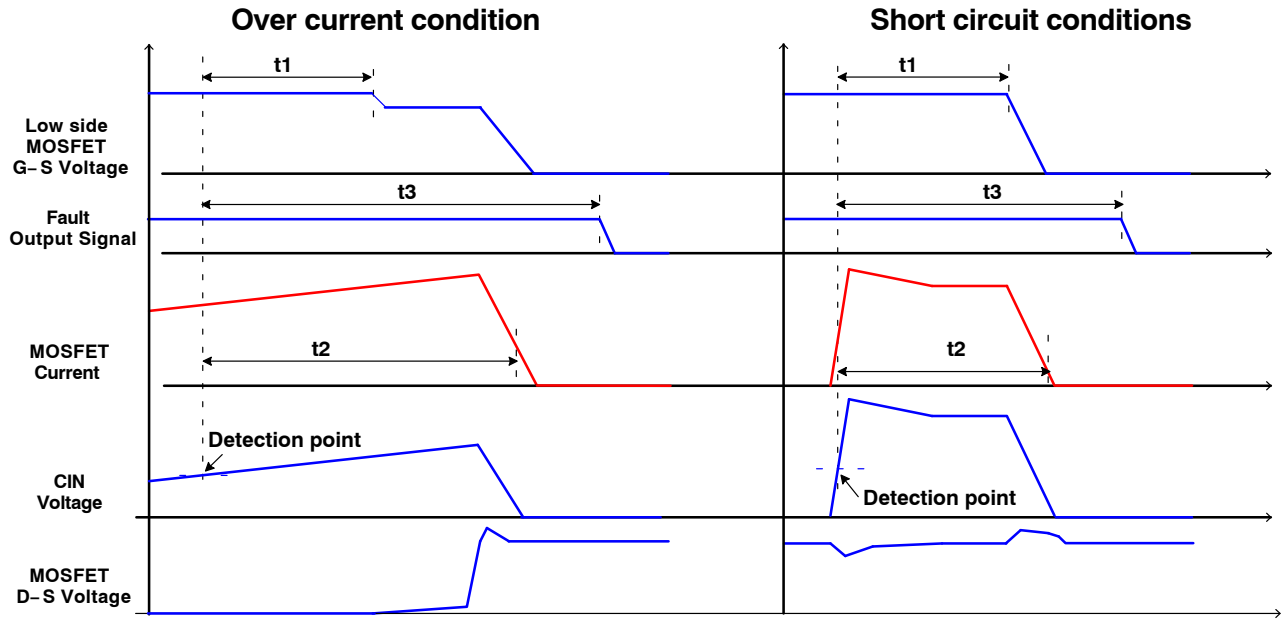

Figure 22. Timing Diagram of Over and Short Circuit Protection

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Table 7. TIME TABLE OF O.C AND S.C PROTECTION; VCIN(REF) TO LOW SIDE GATE, DRAIN CURRENT AND VFO

Ref. Conditions VPN = 600 V, VDD = 18 V		Over Current (2 × Rated Current)						Short Circuit					
		t1 [μs] (Note 34)		t2 [μs] (Note 35)		t3 [μs] (Note 36)		t1 [μs] (Note 34)		t2 [μs] (Note 35)		t3 [μs] (Note 36)	
Device	Tj [°C]	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.	Typ.	Max.
NFAM5312SCBUT	25	0.90	1.15	1.10	1.40	3.70	4.70	0.90	1.15	1.00	1.30	3.70	4.70
	150	0.85	1.10	1.15	1.45	3.00	4.00	0.85	1.10	1.05	1.35	3.00	4.00
NFAM3812SCBUT	25	0.90	1.15	1.15	1.45	3.70	4.70	0.90	1.15	1.05	1.35	3.70	4.70
	150	0.85	1.10	1.20	1.50	3.00	4.00	0.85	1.10	1.10	1.40	3.00	4.00
NFAM2512SCBUT	25	0.90	1.15	1.20	1.50	3.70	4.70	0.90	1.15	1.10	1.40	3.70	4.70
	150	0.85	1.10	1.25	1.55	3.00	4.00	0.85	1.10	1.15	1.45	3.00	4.00

NOTE: To guarantee safe short-circuit protection under all operating conditions, VCIN should be detected within 1.0 μs after short circuit occurs. (Recommendation: SCWT < 2.0 μs, Conditions: VDC = 800 V, VDD = 18 V, Tj = 150 °C).
It is recommended that delay time should be minimized from short-circuit to CIN triggering

34. t1: from CIN detection to gate driver LO shut down
35. t2: from CIN detection to drain current 10 %
36. t3: from CIN detection to fault out signal activation

Fault Output Circuit

VFO pin is the fault output alarm pin to give a fault state condition in SPM31 products. And an active low output is given on this pin for a fault state condition. The alarm conditions are Over-Current Protection (OCP), or low-side bias Under-Voltage Lock Out (UVLO) operation. The VFO output is open drain configured and VFO signal line should be pulled up to control power supply with 10 kΩ resistance as shown in Figure 23. The RC coupling shown dotted in Figure 23 can be changed depending on the application and the wiring impedance.

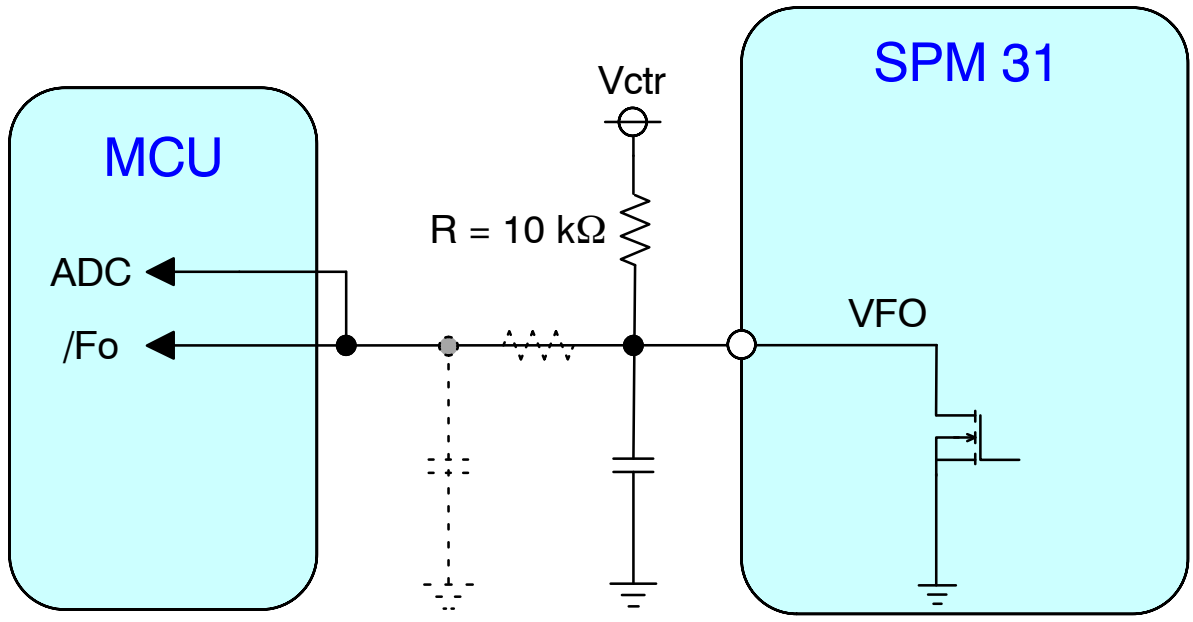

Figure 23. Propose Circuit for Fault Output Function

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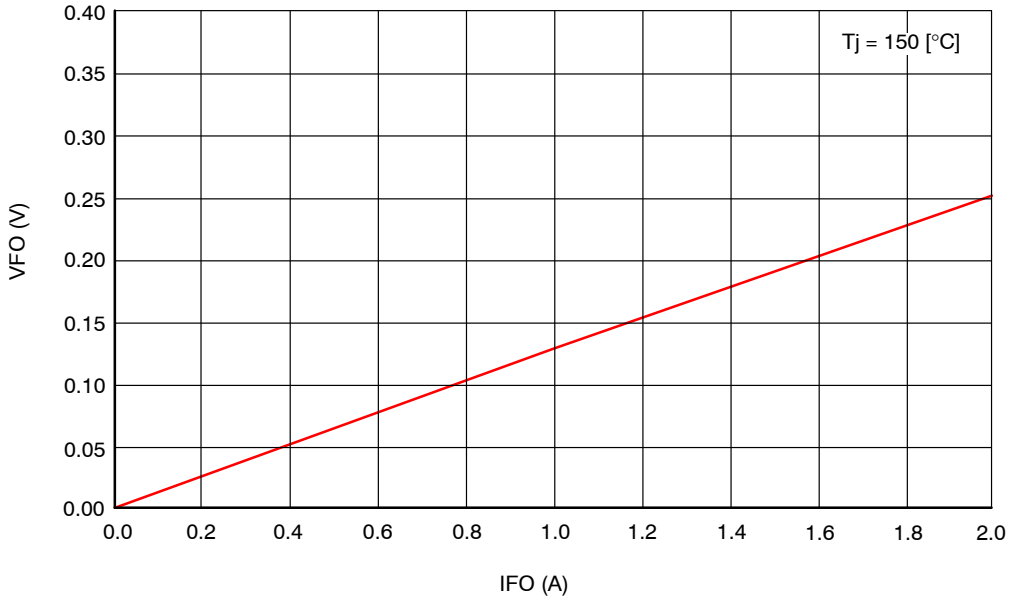

Figure 24. Voltage-Current Characteristics of VFO Terminal

Circuit of Input Signal (HINx, LINx)

Figure 25 shows recommended I/O interface circuit between the MCU and SPM 31. Because SPM 31 input logic is active HIGH and there are built-in pull-down resistors, external pull-down resistors are not needed. Since the fault output is open drain and its rating is VDD + 0.3 V, 18 V supply interface is possible.

However, it is recommended that the fault output is configured with the 5 V logic supplies, which is the same as the input signals. It is also recommended that the decoupling capacitors is placed at both the MCU and Motion SPM 31 ends of the VFO signal line, as close as possible to each device. The RC coupling at each input (parts shown dotted in Figure 25) can be changed depending on the PWM control scheme used in the application and the wiring impedance of the PCB layout.

The input signal section of the SPM 31 series integrates a 5 kΩ (typical) pull-down resistor. Therefore, when using an external filtering resistor between the MCU output and the Motion SPM 31 input, attention should be given to the signal voltage drop at the Motion SPM 31 input terminals to satisfy the turn-on threshold voltage requirement. For instance, R = 100 Ω and C = 1 nF for the parts shown dotted in Figure 25.

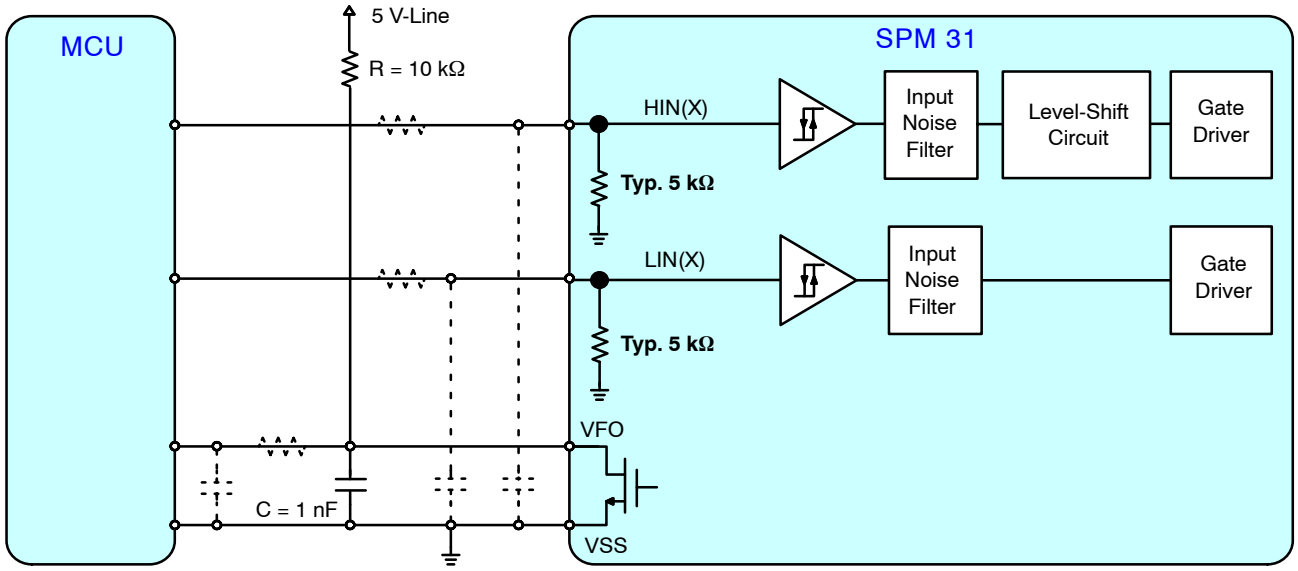

Figure 25. Recommended MCU I/O Interface Circuit

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Bootstrap Circuit Design

Operation of Bootstrap Circuit

The VBS voltage, which is the voltage difference between VB(U,V,W) and VS(U,V,W), provides the supply to the HVIC within the 1200 V SPM 31 series. This supply must be in the range of 13.5 V ~ 19.5 V to ensure that the HVIC can fully drive the high-side MOSFET. The SPM 31 series includes an under-voltage lock out protection function for the VBS to ensure that the HVIC does not drive the high-side MOSFET, if the VBS voltage drops below a specified voltage. This function prevents the MOSFET from operating in a high dissipation mode. There are a number of ways in which the VBS floating supply can be generated. One of them is the bootstrap method described here (refer to Figure 26). This method has the advantage of being simples and inexpensive. However, the duty cycle and on-time are limited by the requirement to refresh the charge in the bootstrap capacitor. The bootstrap to ground (either through the low-side or the load), the bootstrap capacitor (C_{BOOT}) is charged through the bootstrap diode (D_{BOOT}) and the resistor (R_{BOOT}) from the VDD supply.

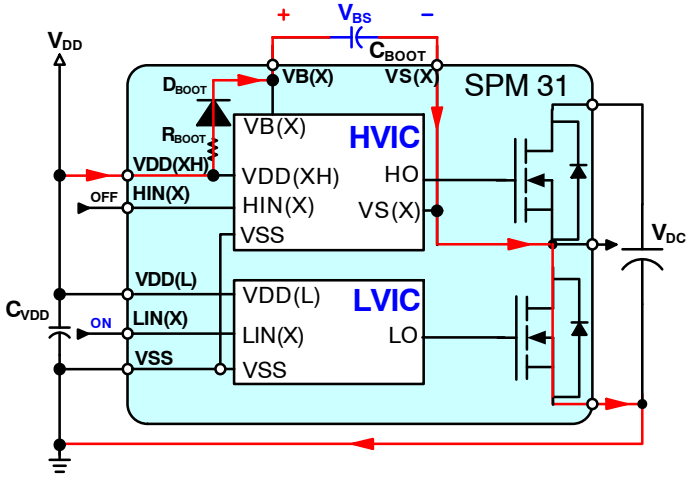

Figure 26. Current Path of Bootstrap Circuit

Selection of Bootstrap Capacitor Considering Initial Charging

Adequate on-time duration of the low-side MOSFET to fully charge the bootstrap capacitor is required for initial bootstrap charging. The initial charging time (t_{charge}) can be calculated by:

$$t_{charge} = C_{BOOT} \times R_{BOOT} \times \frac{1}{\delta} \times \ln \frac{VDD}{VDD - VBS(Min.) - VF - VLS} \quad \text{(eq. 1)}$$

Where:

VF	is a forward voltage drop across the bootstrap diode;
VBS(Min.)	is the minimum value of the bootstrap capacitor;
VLS	is a voltage drop across the low-side MOSFET or load; and
δ	is duty ratio of PWM.

Charging bootstrap capacitor is initially required before normal operation of PWM starts for the SPM 31 series. When the bootstrap capacitor is charged initially; VDD drop voltage is generated based on initial charging method, VDD line SMPS output current, VDD source capacitance, and bootstrap capacitance. If VDD drop voltage reaches UVDDD level, the low side is shut down and a fault signal is activated.

To avoid this malfunction, related parameter and initial charging method should be considered. To reduce VDD voltage drop at initial charging, a large VDD source capacitor and selection of optimized low-side turn-on method are recommended.

Figure 27 shows an example of initial bootstrap charging sequence. Once VDD establishes, VBS needs to be charged by turning on the low-side MOSFETs. PWM signals are typically generated by an interrupt triggered by a timer with a fixed interval, based on the switching carrier frequency.

Therefore, it is desired to maintain this structure without creating complementary high-side PWM signals. The capacitance of VDD should be sufficient to supply necessary charge to VBS capacitance in all three phases. If a normal PWM operation starts before VBS reaches UVLO reset level, the high-side MOSFETs cannot switch without creating a fault signal. It may lead to a failure of motor start in some applications. If three phases are charged synchronously, initial charging current through a single shunt resistor may exceed the over-current protection level.

Therefore, initial charging time for bootstrap capacitors need to be separated, as shown in Figure 28 if amount of initial current during short time should be minimized. The effect of the bootstrap capacitance factor and charging method (low-side MOSFET driving method) is shown in Figure 27.

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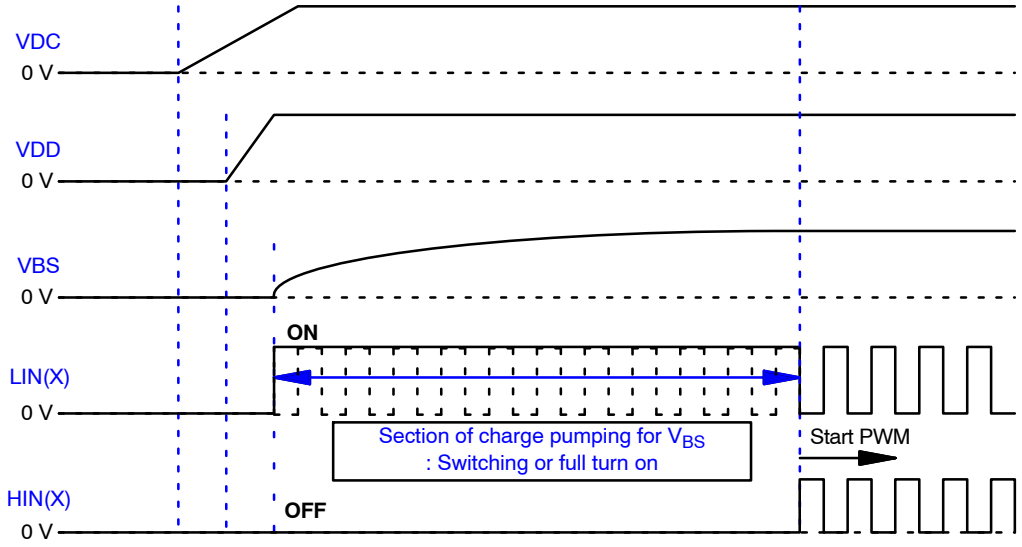

Figure 27. Timing Chart of Initial Bootstrap Charging

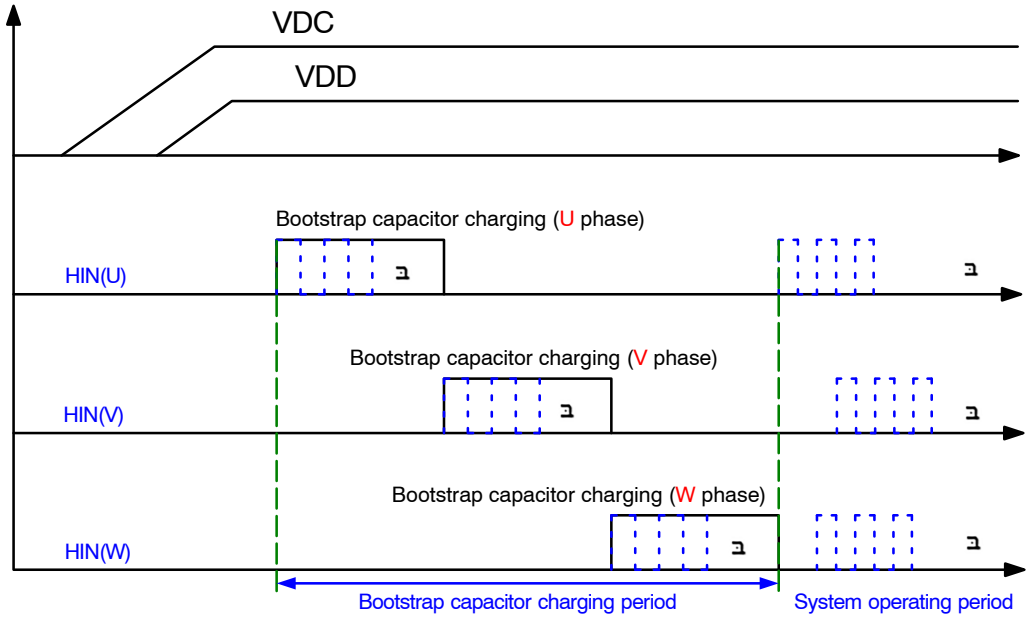

Figure 28. Recommended Initial Bootstrap Capacitors Charging Sequence

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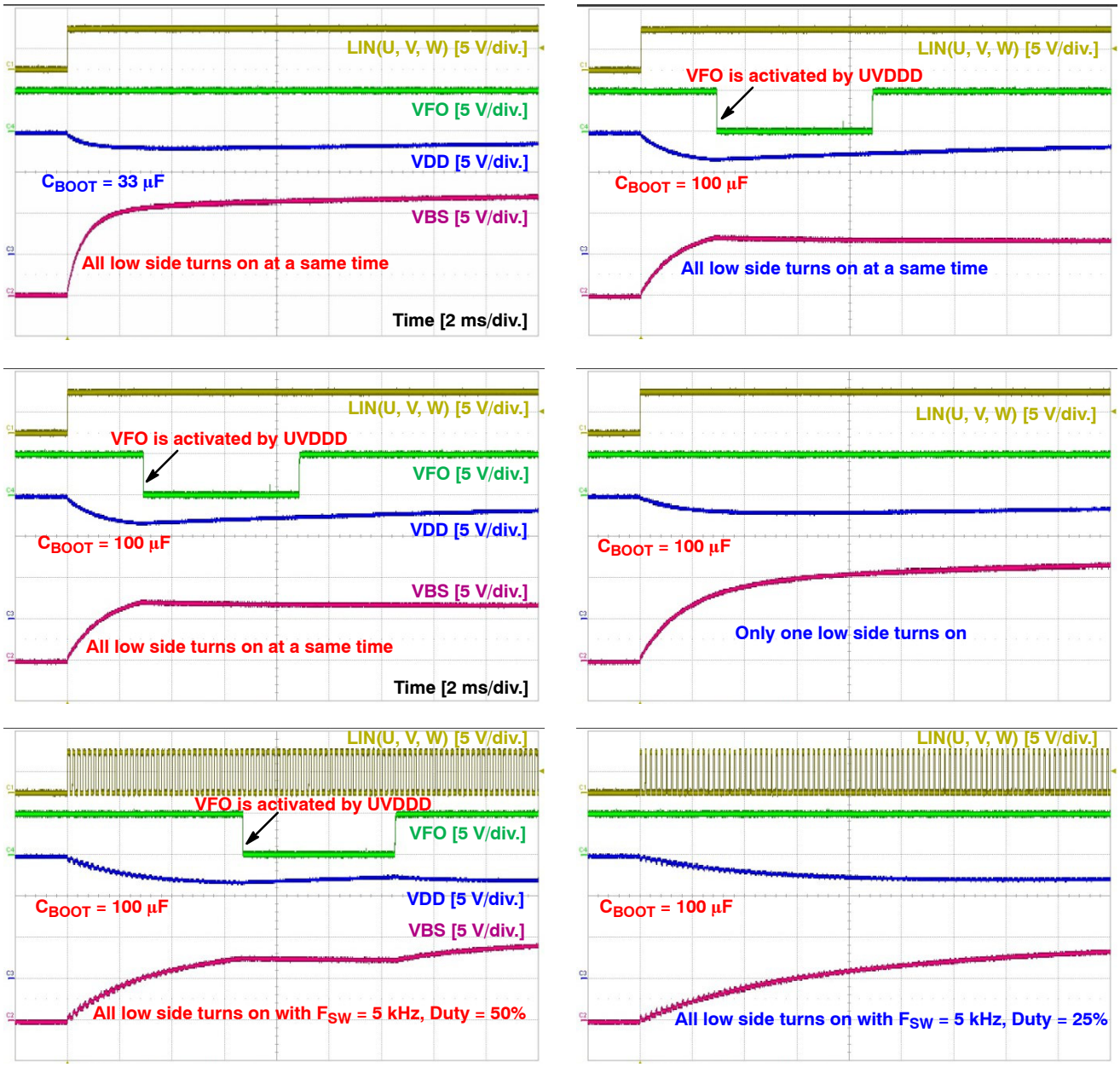

Figure 29. Initial Charging According to Bootstrap Capacitance and Charging Method (Ref. Condition: VDD = 15 V / 300 mA, VDD Capacitor = 220 µF, C_{BOOT} = 100 µF, R_{BOOT} = 20 Ω)

Selection of Bootstrap Capacitor Considering Operating

The bootstrap capacitance can be calculated by:

$$C_{BOOT} = \frac{I_{leak} \times \Delta t}{\Delta VBS} \quad \text{(eq. 2)}$$

Where

- Δt is the maximum on pulse width of high-side MOSFET;
- ΔVBS is the allowable discharge voltage of the C_{BOOT} (voltage ripple); and
- Ileak is the maximum discharge current of the C_{BOOT}.

Mainly via the following mechanisms:

- Gate charge for turning the high-side MOSFET on.
- Quiescent current to the high-side circuit in HVIC.
- Level-shift charge required by level-shifters in HVIC.
- Leakage current in the bootstrap circuit.
- C_{BOOT} capacitor leakage current (ignored for non-electrolytic capacitors).
- Bootstrap diode reverse recovery charge.

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Practically, 3.5 mA of I_{Leak} is recommended for the 1200 V SPM 31 series. By considering dispersion and reliability, the capacitance is generally selected to be 2 ~ 3 times of the calculated one. The C_{BOOT} is only charged when the high-side MOSFET is off and the VS(x) voltage is pulled down to ground.

The on-time of the low-side MOSFET must be sufficient to ensure that the charge drawn from the C_{BOOT} capacitor to be fully replenished. This creates an inherent minimum on-time of the low-side MOSFET (or off-time of the high-side MOSFET).

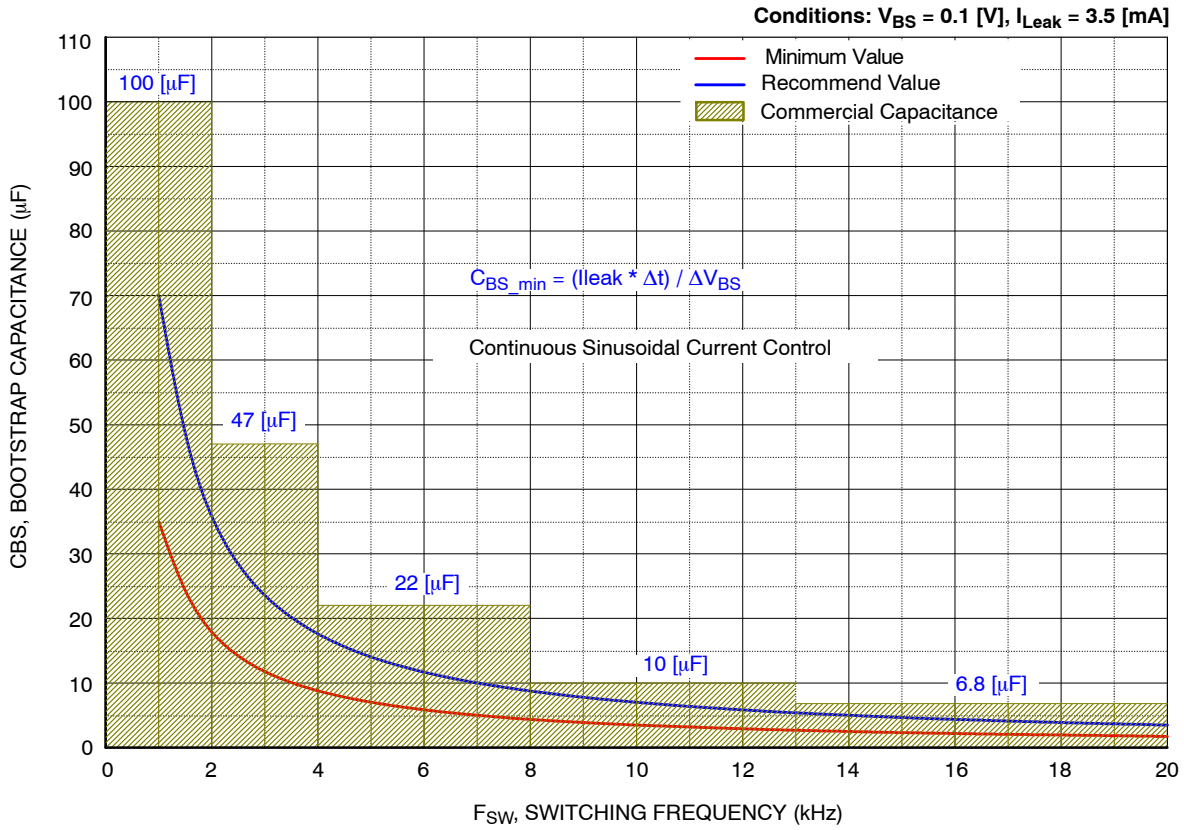

Figure 30. Capacitance of Bootstrap Capacitor on Variation of Switching Frequency

Based on switching frequency and recommended ΔVBS (Note 37).

I_{Leak}: circuit current = 3.5 mA (recommended value)

ΔVBS: discharged voltage = 0.1 V (recommended value)

Δt: maximum on pulse width of high-side MOSFET = 0.2 ms (depends on application)

Built-in Bootstrap Circuit

When the low-side MOFET or body diode conducts, the bootstrap diode (D_{BOOT}) supports the entire bus voltage. Hence, a diode with withstand voltage of more than 1200 V is recommended. It is important that this diode has a fast recovery (recovery time < 100 ns) characteristic to minimize the amount of charge fed back from the bootstrap capacitor into the VDD supply. The bootstrap resistor (R_{BOOT}) is to slow down the dVBS/dt and limit initial charging current (I_{charge}) of bootstrap capacitor.

Normally, a bootstrap circuit consists of bootstrap diode (D_{BOOT}), bootstrap resistor (R_{BOOT}), and bootstrap capacitor (C_{BOOT}). As shown in Figure 31, the built-in bootstrap circuit of SPM 31 product has special VF characteristics with bootstrap resistor. Therefore, only external bootstrap capacitors are needed to make bootstrap circuit.

The characteristics of the built-in bootstrap diode in the SPM 31 products are:

Fast recovery diode: more than 1200 V / 2 A

Resistive characteristic: equivalent resistor of approximately 15.5 Ω

NOTE:

37. The capacitance can be changed according to the switching frequency, capacitor type, and VBS voltage. The above result is a calculation example. So, This value can be changed according to the control method and lifetime of the component.

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Table 8 shows the specification of bootstrap circuit. Figure 31 shows forward voltage drop of the bootstrap diode.

Table 8. SPECIFICATION FOR INTEGRATED BOOTSTRAP CIRCUIT

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
VF	Forward Voltage	IF = 0.1 A, Tj = 25 °C	2.1	2.5	2.9	V
RBOOT	Built-in Limiting Resistance		12.5	15.5	18.5	Ω

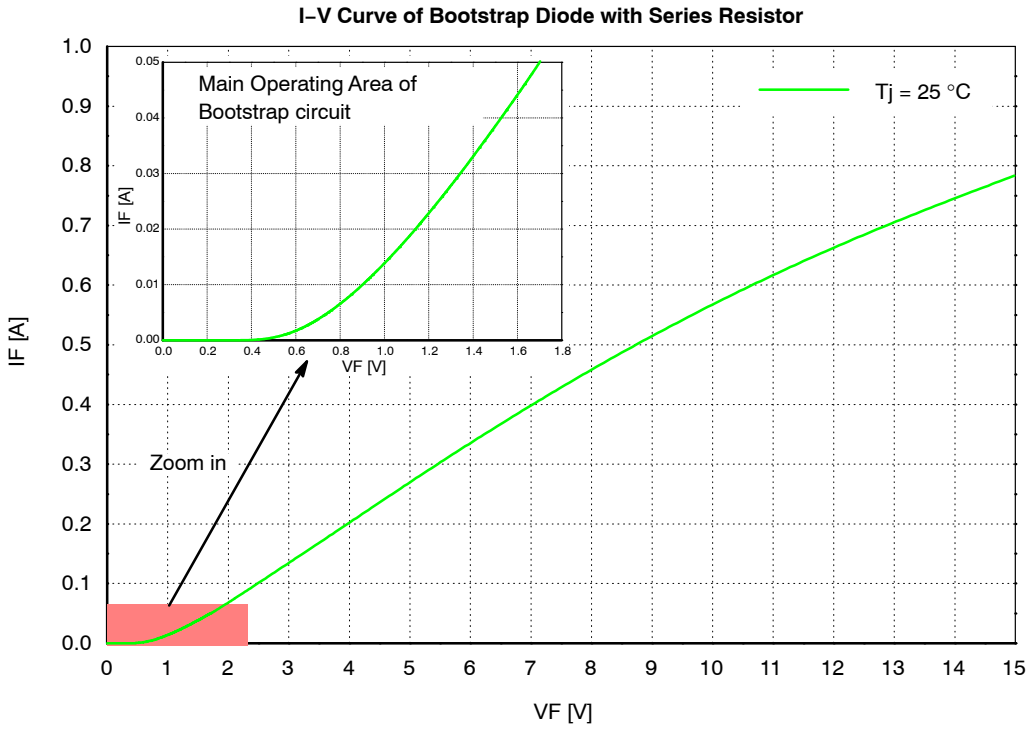

Figure 31. V-I characteristics of Bootstrap Circuit in SPM 31 Series Products

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PRINT CIRCUIT BOARD (PCB) DESIGN

General Application Circuit Example

Figure 32 shows a general application circuitry of interface schematic with control signals connected directly to MCU. Figure 33 shows guidance of PCB layout for the 1200 V SPM 31 series.

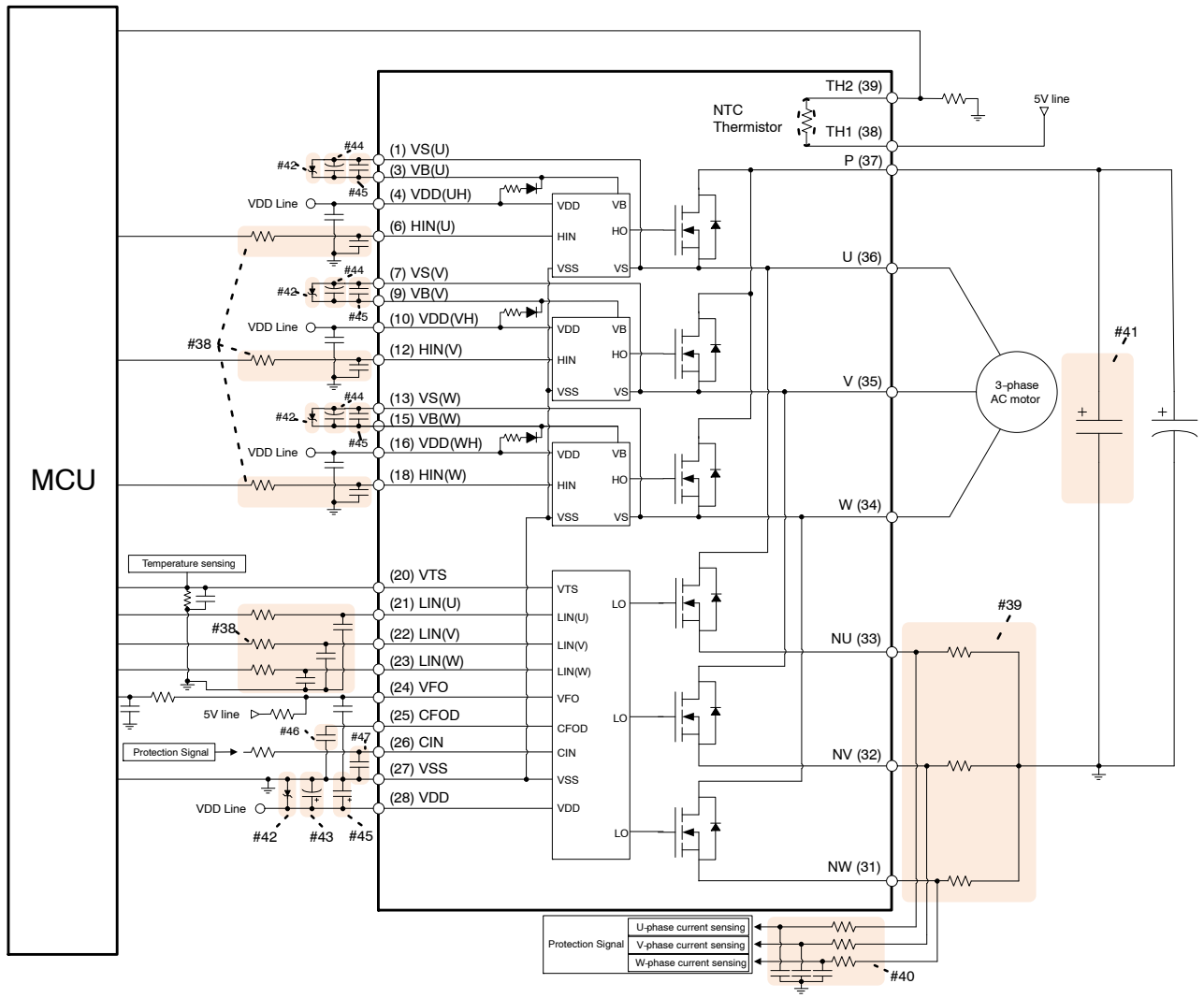

Figure 32. General Application Circuitry for 1200 V Motion SPM 31

To avoid malfunction, the wiring of each input should be as short as possible (less than 2–3 cm). Each capacitor should be mounted as close to the pins of the product as possible. VFO output is open-drain type. This signal line should be pulled up to the positive side of the MCU or control power supply with a resistor that makes IFO up to 1mA. Please refer to Figure 24.

NOTES:

38. Input signal is active-HIGH type. There is a 5 kΩ resistor inside the IC to pull-down each input signal line to GND. RC coupling circuits should be adopted for the prevention of input signal oscillation. RC time constant should be selected in the range 50 ~ 150 ns. (Recommended R = 100 Ω, C = 1nF)
39. Each wiring pattern inductance should be minimized (Recommend less than 10 nH). Use the shunt resistor of surface mounted (SMD) type to reduce wiring inductance. To prevent malfunction, wiring should be connected to the terminal of the shunt resistor as close as possible.
40. In the short-circuit protection circuit, please select the RC time constant in the range 1.5 ~ 2.0 μs. Do enough evaluation on the real system because short-circuit protection time may vary wiring pattern layout and value of the RC time constant.
41. To prevent surge destruction, the wiring between the snubber capacitor and the P & GND pins should be as short as possible. The use of a high-frequency non-inductive capacitor of around 0.1 ~ 0.22 μF between the P & GND pins is recommended.
42. The zener diode or transient voltage suppressor should be adopted for the protection of ICs from the surge destruction between each pair of control supply terminals (recommended zener diode is 22 V / 1 W, which has the lower zener impedance characteristic than about 15 Ω).
43. VDD electrolytic capacitor is recommended around 7 times larger than VBS electrolytic bootstrap capacitor.
44. Please choose the VBS electrolytic bootstrap capacitor with good temperature characteristic.
45. 0.1 ~ 0.2 μF R-category ceramic capacitors with good temperature and frequency characteristics is recommended.
46. Fault out pulse width can be adjusted by capacitor connected to the CFOD terminal.
47. To prevent protection function errors, CIN capacitor should be placed as close to CIN and VSS pins as possible.

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PCB Layout Guidance

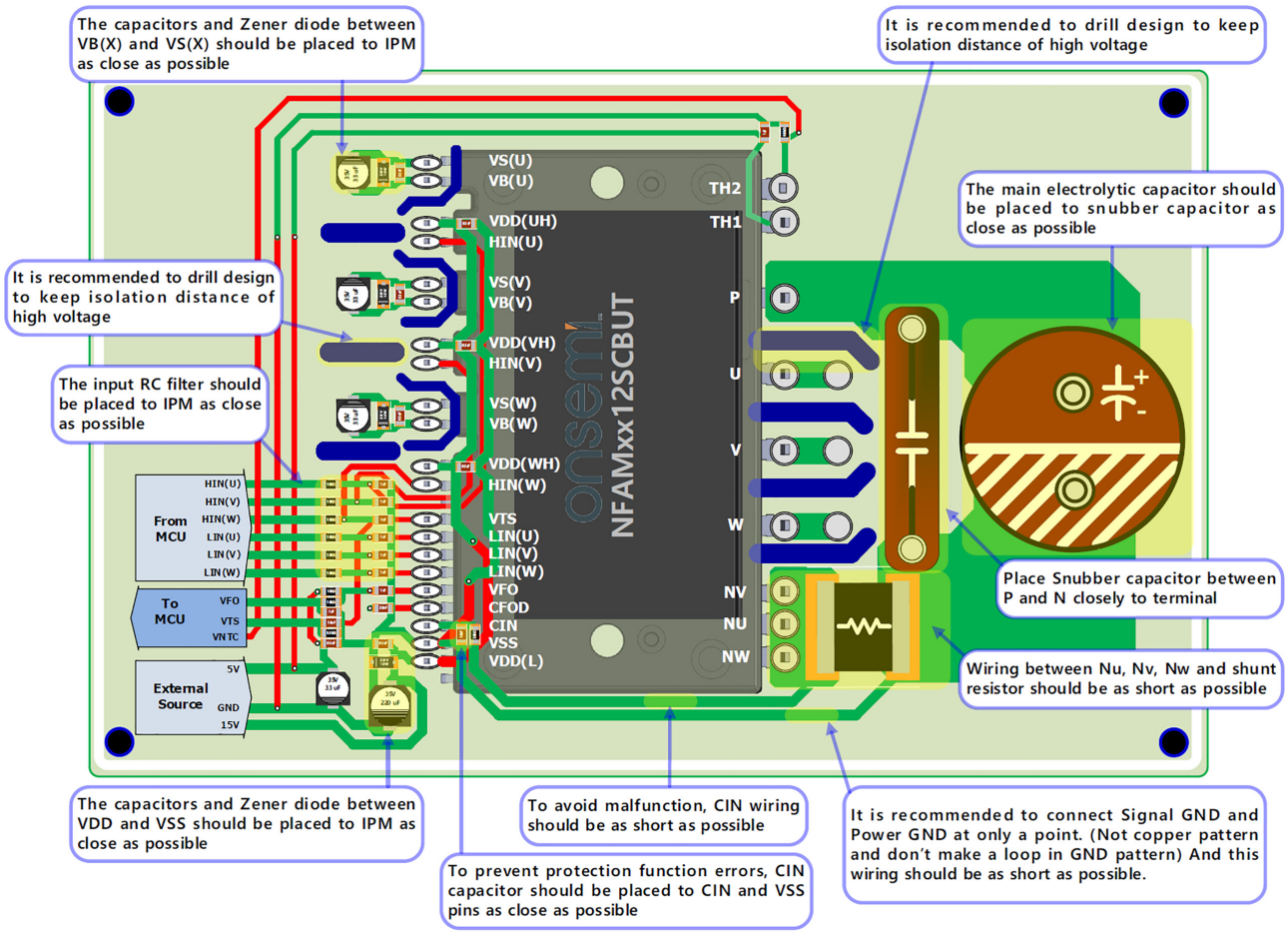

Figure 33. Print Circuit Board (PCB) Layout Guidance for SPM 31 Series

If the wiring length between the IPM and the shunt resistor is long, it will cause excessive surges that might damage the IPM. To decrease the pattern inductance, the wiring pattern length between IPM and snubber capacitor should be as short as possible. As shown in Figure 34. snubber capacitor should be installed in the right location to suppress surge voltage effectively. Generally, snubber capacitor of around 0.1 μF ~ 0.22 μF is recommended. There are three locations where the snubber capacitor can be installed (A), (B) or (C). If the snubber capacitor is installed in location (A) as shown in Figure 34, it cannot suppress the surge voltage effectively. The location (B) for surge suppression effect is greater than location (A) or (C). However, if the capacitor is installed in location (B), the charging and discharging currents generated by the wiring inductance and the snubber capacitor will not be flowed through the shunt resistor. The current sensing accuracy and short circuit protection level will be a little lower than the calculated design value. The location (C) is better suppression than location (A) without impacting the current sensing signal accuracy.

The location (B) is excellent in terms of surge suppression, and location (C) is excellent in terms of current sensing signal accuracy.

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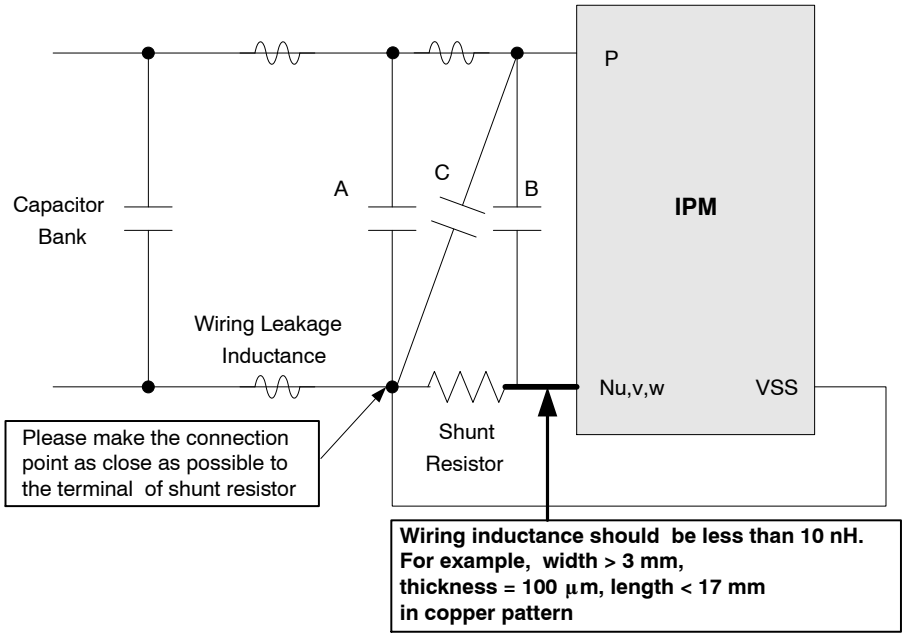

Figure 34. Recommended Snubber Capacitor and Wiring of Shunt Resistor

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REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document version release.	3/12/2025
1	Updated Figure 4 – Pin 28 description added.	4/8/2025
2	Replaced incorrect “x” characters with proper multiplication symbols (x) in formulas on page 20.	6/27/2025
3	Update of Electrical Characteristics table, Figure 8, Figure 11, addition of Table 3, Figure 13, new paragraph in the “PCB Layout Guidance” section and Figure 34.	4/1/2026
4	Updated Figure 15 and corrected VTS threshold voltage equations on page 16. Updated CASE MODGC Package Outline on page 7, changing the issue level from B to C.	7/2/2026

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