# Loop Compensation of Voltage -Mode Buck Converters – Example for FAN65004B

# AND90404/D

## INTRODUCTION

This application note focuses on a voltage-mode buck converter that uses a standard error amplifier. The term “error amplifier” in this context refers specifically to an operational amplifier, rather than a transconductance amplifier or any other type. This approach is one of the simplest ways to learn about compensation in power supply design.

Most engineers are already familiar with the fundamental concepts needed for this topic, so the emphasis here is on connecting that knowledge in a clear and practical manner. Simplifications are applied whenever possible to maintain clarity while ensuring accuracy.

To design an effective compensation scheme, a basic simulation using resistors, capacitors, inductors, and an ideal op-amp – or even just logarithmic graph paper – will be sufficient. This will help ensure the stable operation of the voltage-mode buck converter with a good transient response.

With this method, there is no need to delve into transfer functions or complex formulas, making it an accessible introduction to switch-mode power supply loop compensation. This foundational understanding can pave the way for exploring more advanced control methods and topologies, such as current-mode control and other topologies like boost converters.

### Purpose of Compensation

The simplest starting point for a switch-mode power supply is an architecture that operates with a fixed duty cycle (Figure 1). This setup lacks feedback or control of the Pulse Width Modulation (PWM) signal.

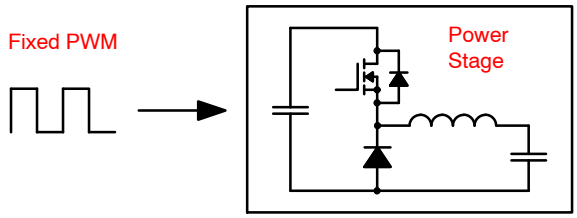



**Figure 1. Fixed Duty Cycle**

In this configuration, a fixed PWM signal is applied to the high-side MOSFET of a non-synchronous buck power stage. Because the duty cycle of the PWM is fixed, the output voltage is dependent on the input voltage, meaning the desired output voltage is only achieved at a specific operating point. For other operating conditions, such as higher or lower loads, the output voltage will have either a positive or negative deviation due to the absence of any regulation.

The next step is to integrate an operational amplifier that compares the power stage’s output voltage with a fixed reference voltage (Figure 2). This error amplifier operates without local feedback, meaning there is no connection between the output and the non-inverting input.

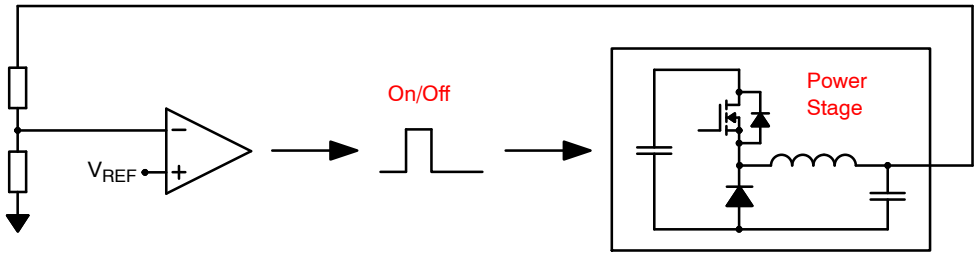



**Figure 2. Error Amplifier without Compensation**

In this setup, the non-inverting input of the operational amplifier is connected to a reference voltage, while the inverting input is connected to the power supply’s output via a voltage divider. The voltage divider is designed so that its output equals the reference voltage at the nominal output voltage of the buck converter. Without feedback, the operational amplifier behaves like a comparator with only two states:

1. If the output voltage is too low, the MOSFET is switched on.
2. If the output voltage is too high, the MOSFET is switched off.

This constitutes a hysteretic regulation, where the converter continuously oscillates between these two states without a fixed switching frequency.

The final step involves adding a compensation network between the output and the inverting input of the error amplifier (Figure 3). This configuration feeds a portion of the amplifier's output voltage back to the inverting input.

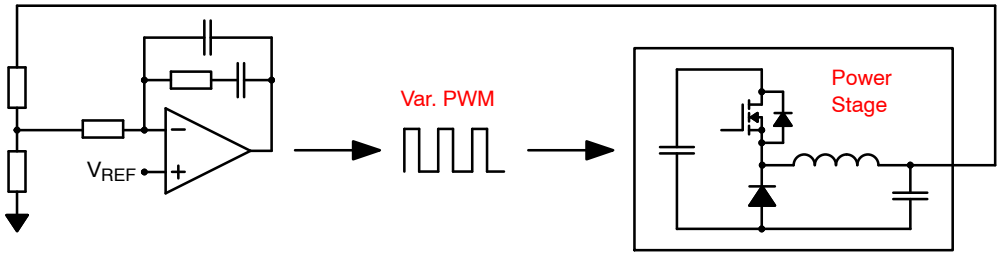



**Figure 3. Error Amplifier with Compensation**

Introducing this feedback allows for output voltage stability against variations in input and output voltage and enables fixed-frequency operation. The compensation network must be carefully designed to ensure proper operation and quick output voltage regulation.

## FUNDAMENTALS

A review of several fundamental concepts is beneficial prior to examining the details.

### Decade

A decade refers to a frequency range from 10 Hz to 100 Hz or from 1 kHz to 10 kHz, essentially representing the ratio of two numbers by a factor of 10.

### Decibel

A decibel (dB) is a unit of measurement for gain expressed on a logarithmic scale with a base of 10. In this context, all calculations are performed for voltage rather than power. The formula to calculate the gain based on the ratio of two voltages, U1 and U2, is as follows:

$$dB[V] = 20 \cdot \log_{10}\left(\frac{U_1}{U_2}\right) \quad \text{(eq. 1)}$$

When calculations involve power instead of voltage, a factor of 10 should be used instead of 20, since doubling the voltage leads to a quadrupling of the power. Using dB has several advantages, such as simplifying the representation of very small or very large numbers and facilitating easier calculations. Here are some key factors to remember:

- A factor of 1 equals 0 dB
- A factor of 2 equals 6 dB
- A factor of 4 equals 12 dB
- And a factor of 10 equals 20 dB

To determine a gain of 26 dB, the following simple calculation can be performed without a calculator:

$$26\ dB = 20\ dB + 6\ dB = (\text{Gain of } 10) \cdot (\text{Gain of } 2) = \text{Gain of } 20 \quad \text{(eq. 2)}$$

As shown, when converting from dB to factors, addition and subtraction are replaced by multiplication and division, and vice versa.

### Bode Plot

A Bode plot (Figure 4) graphically represents the transfer function of a system. For a switch-mode power supply, it typically contains the following information:

- The gain curve in decibels (dB) is represented on the left scale (red in this example)
- The phase curve in degrees (°) is represented on the right scale (blue in this example)
- The gain range is generally symmetrical, such as ±40 dB in this example
- The phase range is typically also symmetrical, usually ±180°

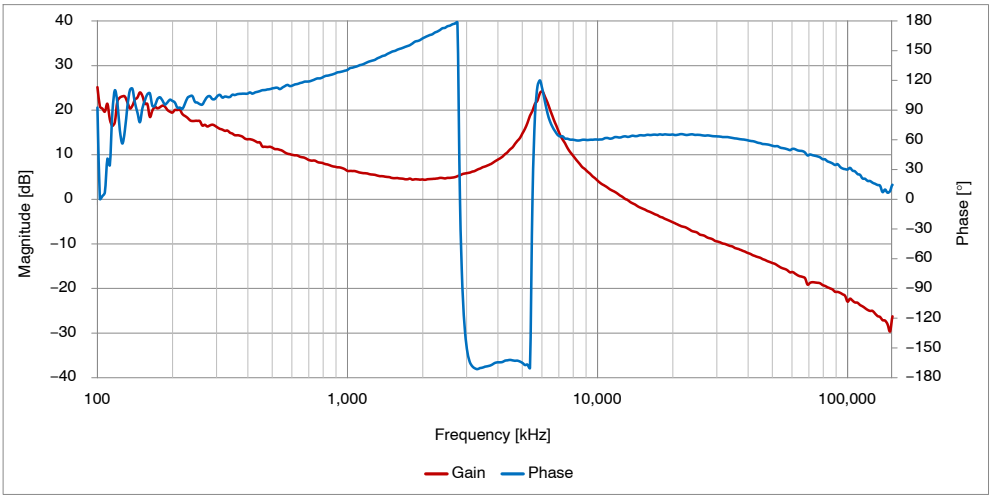



**Figure 4. Bode Plot**

It is important to note that the total phase can only reach a maximum of 360°. For example, the range can extend from −180° to +180° or from −90° to +270°. Aligning 0 dB with 0° simplifies the interpretation of phase and gain margins.

The phase illustrated in this example shows a jump due to the phase limits. Once the phase exceeds +180°, it resets to −180° at the bottom of the chart. This behavior results from the selected limits and should not be interpreted as an issue. With limits set to 90° and +270°, this phenomenon would not appear; however, it would lead to a misalignment of the 0 dB and 0° lines, as mentioned before.

### Non-Inverting and Inverting Amplifier

This section presents the basic circuits that are used to illustrate the gain characteristics of operational amplifiers.

The first circuit is a “non-inverting amplifier” with a gain of +2.0.

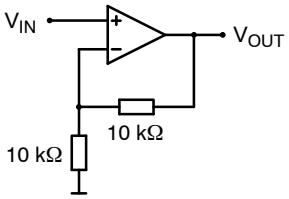



**Figure 5. Non-Inverting Amplifier with a Gain of +2.0**

In this configuration, the input is connected to the non-inverting input of the operational amplifier. The gain is set by two resistors according to the following equation:

$$G = 1 + \frac{10\ k\Omega}{10\ k\Omega} = 2.0 \qquad \text{(eq. 3)}$$

A gain of +2.0 corresponds to +6 dB. Since the signal is neither inverted nor frequency-dependent, there is no phase change, resulting in a phase of zero degrees. Under ideal conditions, the Bode plot illustrates a constant gain of +6 dB and a constant phase of 0° from 10 Hz to 1 MHz, as shown in Figure 6.

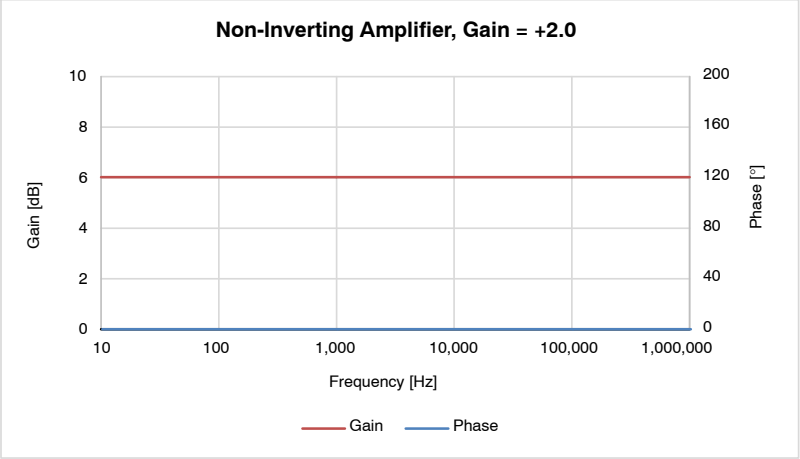



**Figure 6. Bode Plot of a Non-Inverting Amplifier with a Gain of +2.0**

The second circuit is an “inverting amplifier” with a gain of −2.0:

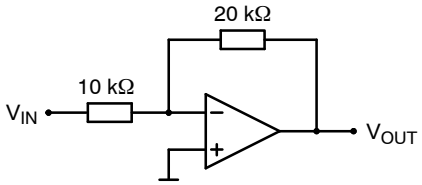



**Figure 7. Inverting Amplifier with a Gain of −2.0**

In this configuration, the input is connected to the inverting input of the operational amplifier, with the gain also determined by two resistors as described by:

$$G = -\frac{20\ k\Omega}{10\ k\Omega} = -2.0 \qquad \text{(eq. 4)}$$

For an inverting amplifier with a gain of −2.0, the gain remains at +6 dB, but the negative sign indicates a phase shift of +180°. Again, the Bode plot shows a constant gain of +6 dB along with a phase of 180° from 10 Hz to 1 MHz.

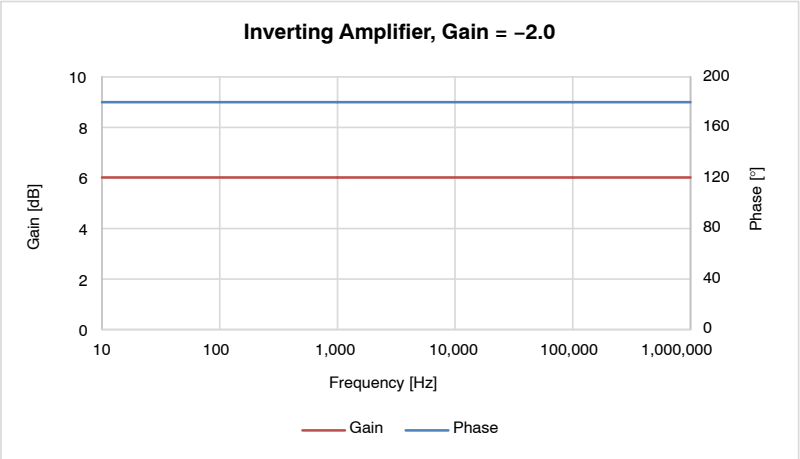



**Figure 8. Bode Plot of an Inverting Amplifier with a Gain of −2.0**

### RC Low-Pass and High-Pass Filters

An “RC (resistor-capacitor) low-pass filter” is a simple, frequency-dependent circuit. Low-frequency signals can pass through without any change in gain or phase, while high-frequency signals are attenuated, leading to a change in phase. The circuit comprises a resistor of 1 kΩ and a capacitor of 100 nF, where only the capacitor can store energy.

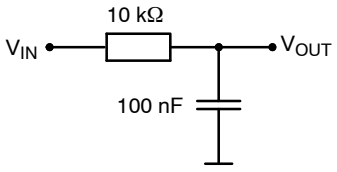



**Figure 9. RC Low-Pass Filter**

The corner frequency, also known as bandwidth or cut-off frequency, for this circuit is 1.59 kHz. This is the frequency at which the gain decreases by 3 dB, and the phase shifts to −45°.

$$f_{3dB} = \frac{1}{2\pi \cdot R \cdot C} = \frac{1}{2\pi \cdot 1\ k\Omega \cdot 100\ nF} = 1.59\ kHz \quad \text{(eq. 5)}$$

This frequency is marked in the plot by the purple line.

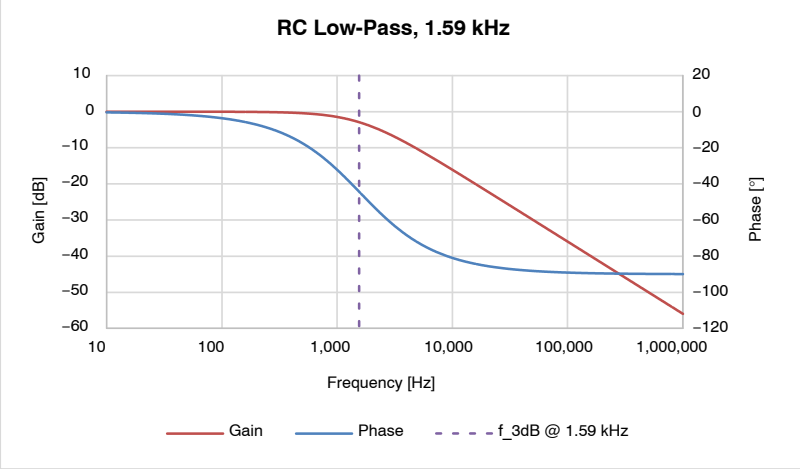



**Figure 10. Bode Plot of a RC Low-Pass Filter**

The phase of the output signal begins to change approximately one decade below the corner frequency. As the frequency increases, the negative phase shift becomes more pronounced, reaching a limit of –90°. The gain starts to decrease near the corner frequency, with higher frequencies resulting in greater attenuation. In an ideal circuit, there is no upper limit to this attenuation. The gain slope is −20 dB per decade because of the single storage element in the filter. If more storage elements are present, such as in an LC filter, the slope changes to −40 dB per decade, resulting in a phase shift of up to −180°.

Reversing the positions of the resistor and capacitor results in the formation of an “RC high−pass filter”. In this configuration, high−frequency signals can pass through without changes to gain or phase, while low−frequency signals are attenuated and undergo a phase change.

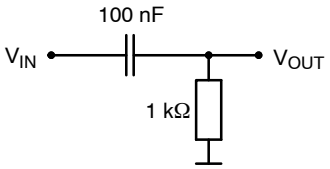



**Figure 11. RC High-Pass Filter**

Since the component values remain the same, the corner frequency does not change.

$$f_{3dB} = \frac{1}{2\pi \cdot R \cdot C} = \frac{1}{2\pi \cdot 1\ k\Omega \cdot 100\ nF} = 1.59\ kHz \quad \text{(eq. 6)}$$

Similar principles apply regarding the initiation and conclusion of the phase shift. However, for low−frequency signals, there is a +90° phase shift, and the gain increases by +20 dB per decade until reaching the corner frequency.

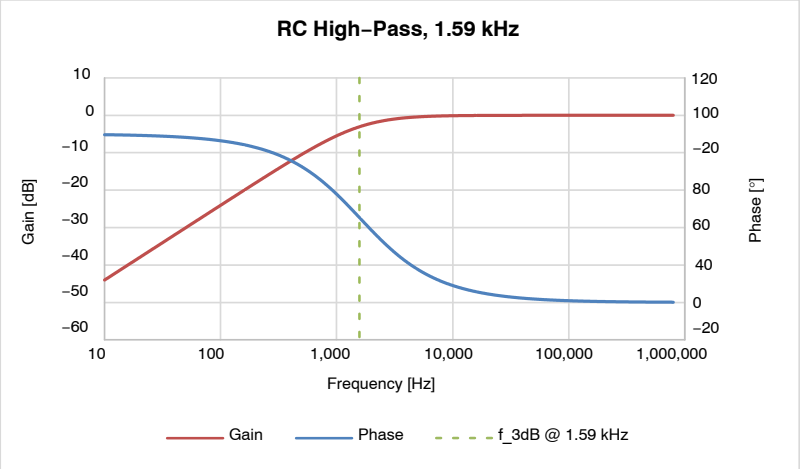



**Figure 12. Bode Plot of a RC High-Pass Filter**

### Combination of Gain, RC High- and Low-Pass Filters

Combining multiple circuits in series is straightforward. The calculations maintain consistency, with gains and phases simply adding up. The order of the series connection does not affect the results.

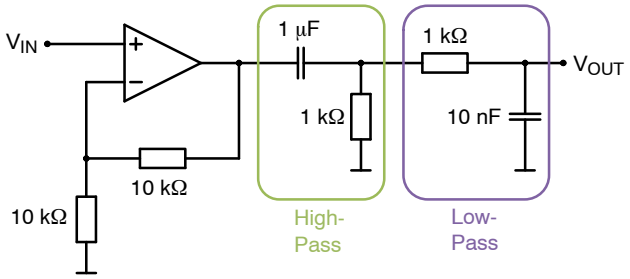



**Figure 13. Amplifier, High- and Low-Pass**

This example involves the combination of three sub-circuits described in the previous sections:

- A non-inverting amplifier with a gain of +6 dB
- A high-pass filter with a corner frequency of 159 Hz
- A low-pass filter with a corner frequency of 15.9 kHz

Figure 14 illustrates the gain of each of the three sub-circuits individually.

- Red represents the gain of the amplifier at +6 dB
- Green denotes the gain of the high-pass filter at a 159 Hz corner frequency
- Purple illustrates the gain of the low-pass filter at a 15.9 kHz corner frequency

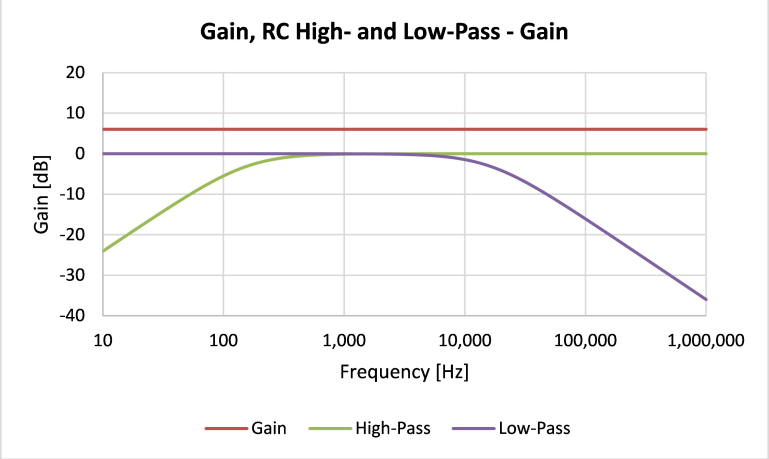



**Figure 14. Gain of Each Individual Circuit**

Figure 15 shows the phase of each individual circuit:

- Red indicates the phase of the amplifier at 0°
- Green represents the phase of the high-pass filter, which shifts from +90° to 0°
- Purple depicts the phase of the low-pass filter, transitioning from 0° to −90°

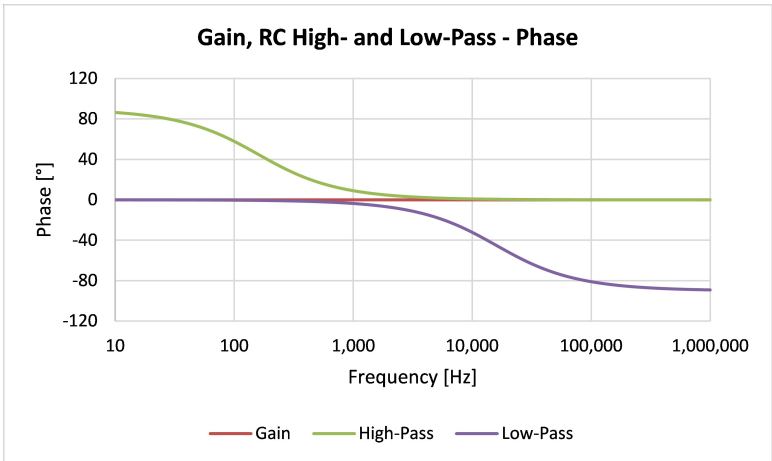



**Figure 15. Phase of Each Individual Circuit**

To determine the total response of the combined system, simply sum the gains and phases. For example, at 10 Hz, the gain is +6 dB from the amplifier, −24 dB from the high-pass filter, and 0 dB from the low-pass filter. The total gain is −18 dB, as illustrated in Figure 16.

The result is a band-pass filter that allows frequencies between 159 Hz and 15.9 kHz to pass through without attenuation.

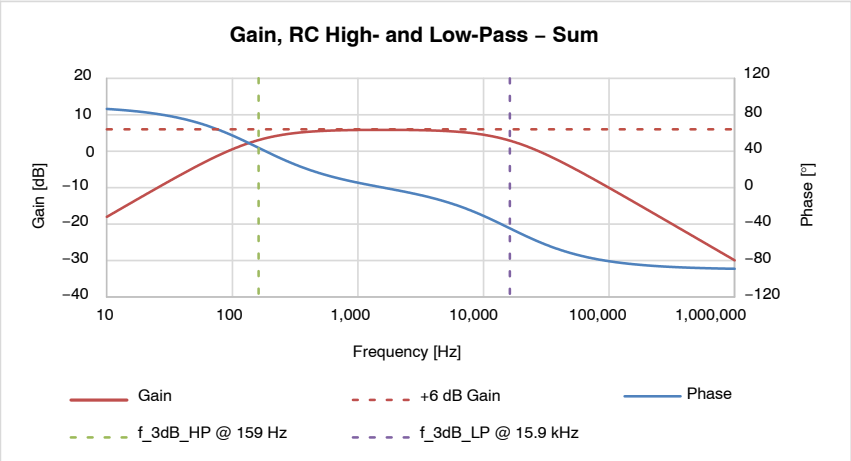



**Figure 16. Gain and Phase of the Combined Circuit**

### Pole and Zero

Poles and zeros are integral to compensation in circuits, although they lack the straightforward representation found in resistor-capacitor combinations. A pole can be illustrated with a specific circuit, which demonstrates its characteristics: it decreases the gain by −20 dB per decade and alters the phase by −90°. The frequency of a pole is determined by the highlighted resistor and capacitor within the circuit.

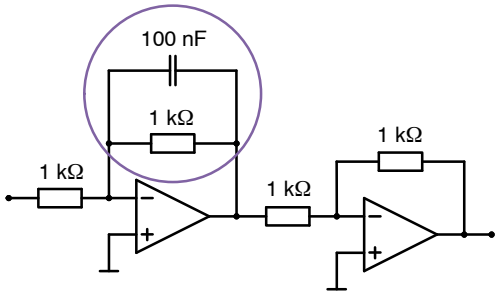



**Figure 17. Circuit for a Pole**

In an inverting configuration, the first operational amplifier introduces a phase shift of +180°. To achieve compensation, a second operational amplifier with a gain of −1 is included, contributing another phase shift of +180°. This results in a total phase shift of 360°, which effectively translates to 0° in terms of phase alignment.

The frequency of the pole is calculated using the same formula employed in previous examples, arriving at a value of 1.59 kHz.

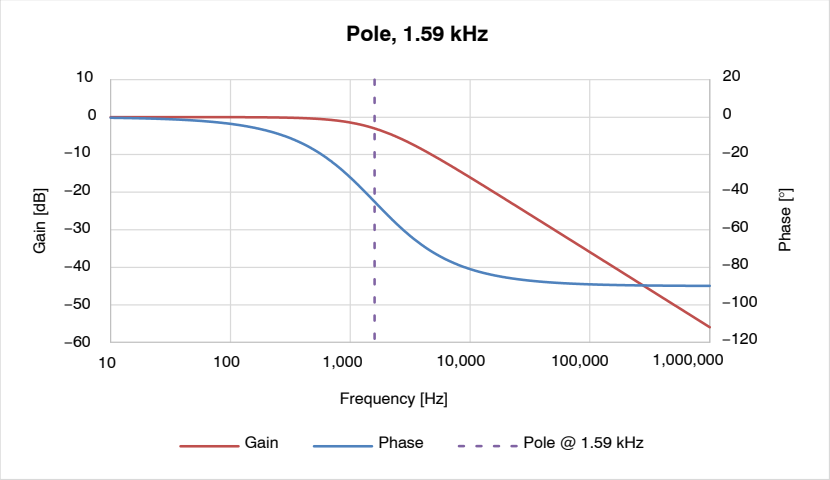



**Figure 18. Bode Plot of a Pole**

The Bode plot (Figure 18) illustrates the gain and phase response of a pole. At the corner frequency, the gain decreases at a rate of −20 dB per decade, while the phase shifts from 0° to −90°. This behavior is similar to that of a low-pass filter. The phase transition begins approximately one decade before reaching the corner frequency and is completed about one decade afterward.

A zero influences the gain by +20 dB per decade and the phase by +90° per decade. To implement a zero in place of a pole, the position of the capacitor must be adjusted. The circuit illustrated in Figure 19 generates a zero at a frequency of 1.59 kHz.

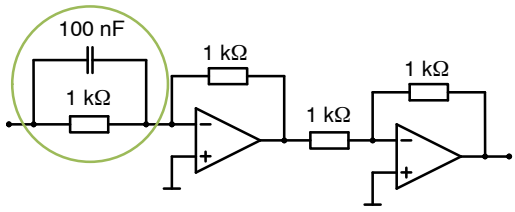



**Figure 19. Circuit for a Zero**

- As before, a second operational amplifier is necessary to compensate for the phase shift introduced by the first operational amplifier.
- The frequency of the zero is calculated using the same formula as in previous examples, which yields a value of 1.59 kHz.

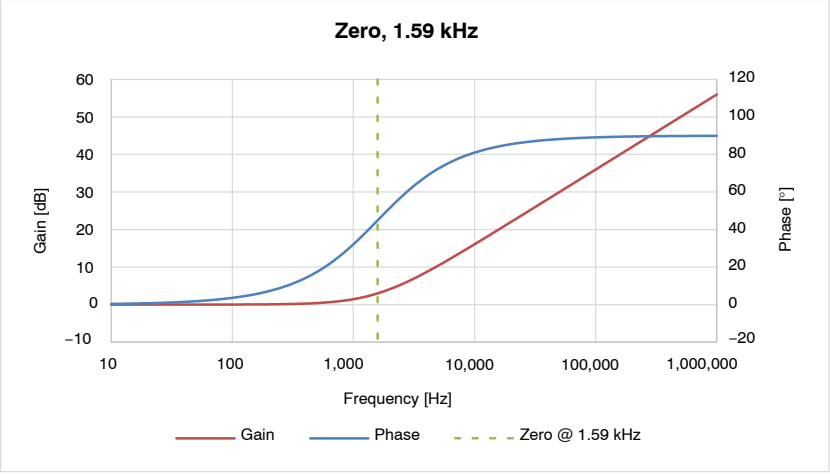



**Figure 20. Bode Plot of a Zero**

Figure 20 illustrates the gain and phase characteristics of a zero. At the corner frequency, the gain slope increases by +20 dB per decade, while the phase transition moves from 0° to +90°. Similar to the behavior of a pole, the phase shift begins approximately one decade before the corner frequency and concludes around one decade after it.

## CLOSED LOOP SYSTEM

After reviewing the fundamental concepts, the relationship between the theoretical closed-loop system model and an actual buck converter can be examined. Figure 21 shows the block diagram of a typical closed-loop system with all its necessary components.

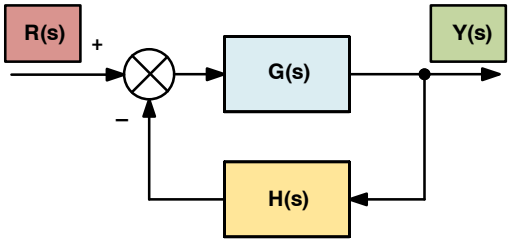



**Figure 21. Closed Loop System Block Diagram**

In this diagram, R(s) represents the reference input, G(s) denotes the open-loop gain, Y(s) is the system output, and H(s) is the feedback path. At the summing junction, the signal from the feedback path H(s) is subtracted from the reference input R(s). This process is known as “negative feedback.”

The various blocks of a voltage-mode buck converter are depicted in Figure 22.

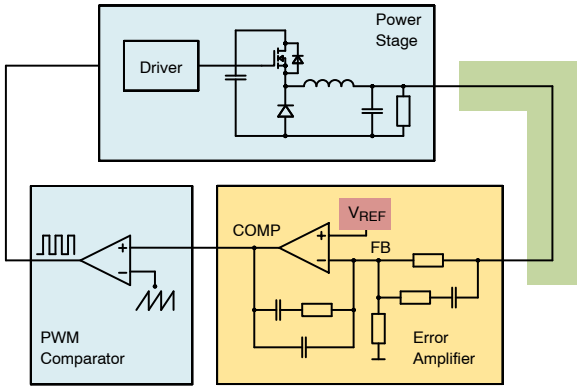



**Figure 22. Buck Converter Block Diagram**

The first block is the power stage, which includes the driver, MOSFET, freewheeling diode, input capacitor, and output filter (inductor + capacitor). The second block is the error amplifier, which is based on an operational amplifier in an inverting configuration along with a compensation network. The third block is the PWM comparator, responsible for generating the on-off signal for the MOSFET in the power stage.

The error amplifier compares the output voltage of the power stage with its reference voltage and produces a DC signal at its output, referred to as COMP. This COMP signal is fed into the comparator and is compared to the sawtooth waveform at the inverting input. Depending on the level of the COMP signal, the duty cycle of the PWM increases or decreases. The duty cycle of the PWM signal ultimately determines the DC output voltage of the buck converter and is adjusted to ensure that the output voltage remains stable and equal to the programmed voltage. The output voltage is set via a voltage divider in the feedback network.

The link between the theoretical model and the buck converter blocks is straightforward:

- The reference voltage corresponds to the reference input R(s).
- The PWM comparator and power stage correspond to the open-loop gain G(s).
- The output voltage corresponds to the system output Y(s).
- The error amplifier, including the compensation network, senses that the output voltage corresponds to the feedback path H(s) at the summing point.

Since the error amplifier operates in an inverting configuration, the input signal – derived from the output voltage after the voltage divider – is subtracted from the signal of the non-inverting input. This process of feedback is known as “negative feedback”, which introduces a –180° phase shift to the system.

## CROSSOVER FREQUENCY, PHASE MARGIN AND GAIN MARGIN

The key parameters of the Bode plot for a switch-mode power supply that relate to stability are the crossover frequency (also referred to as “bandwidth”), phase margin, and gain margin.

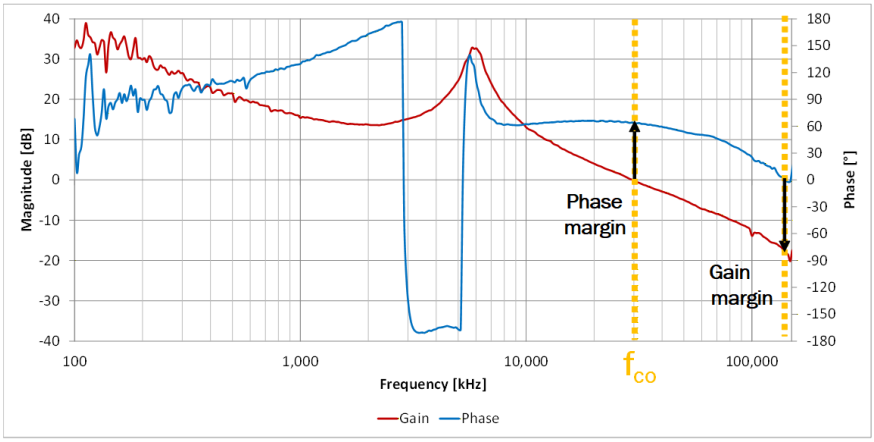



**Figure 23. Bode Plot of a Voltage Mode Buck Converter**

At a specific frequency, the gain plot intersects 0 dB. This point is referred to as the crossover frequency ($f_{co}$) or bandwidth. A higher crossover frequency indicates a quicker response of the power supply to load changes, resulting in lower deviation of the output voltage. For a buck converter, the crossover frequency typically ranges between 1/10 and 1/5 of the switching frequency.

The phase at the crossover frequency represents the phase margin. This margin indicates how much phase can change before the system becomes unstable. Typical values for phase margin range from 45° to 60°. The gain margin is the corresponding gain at which the phase intersects 0°. It reflects the amount of gain that can be adjusted without leading to instability, with typical values of −10 dB or lower.

Sufficient phase and gain margins are crucial for ensuring stable operation, especially given tolerances, aging, and temperature variations of external components, particularly in the power stage. The slope at the crossover frequency should ideally range from −25 to −20 dB per decade. A steeper slope could bring the system closer to instability. Components in the power stage that have high tolerances or temperature dependencies, such as aluminum capacitors – generally avoided at the output for these reasons – require additional margin to maintain stability.

## FAN65004B SYNCHRONOUS VOLTAGE MODE BUCK REGULATOR

The FAN65004B is a synchronous buck regulator designed to accommodate an input voltage of up to 65 V and an output current of 6 A. It functions as a voltage mode controller, which means that only the output voltage is used for regulation. In contrast to current-mode controllers, current measurement is employed solely for overcurrent protection and not for regulation purposes. The error amplifier is a standard operational amplifier. Figure 24 illustrates the block diagram of the converter alongside its external circuitry, including the power stage and compensation network.

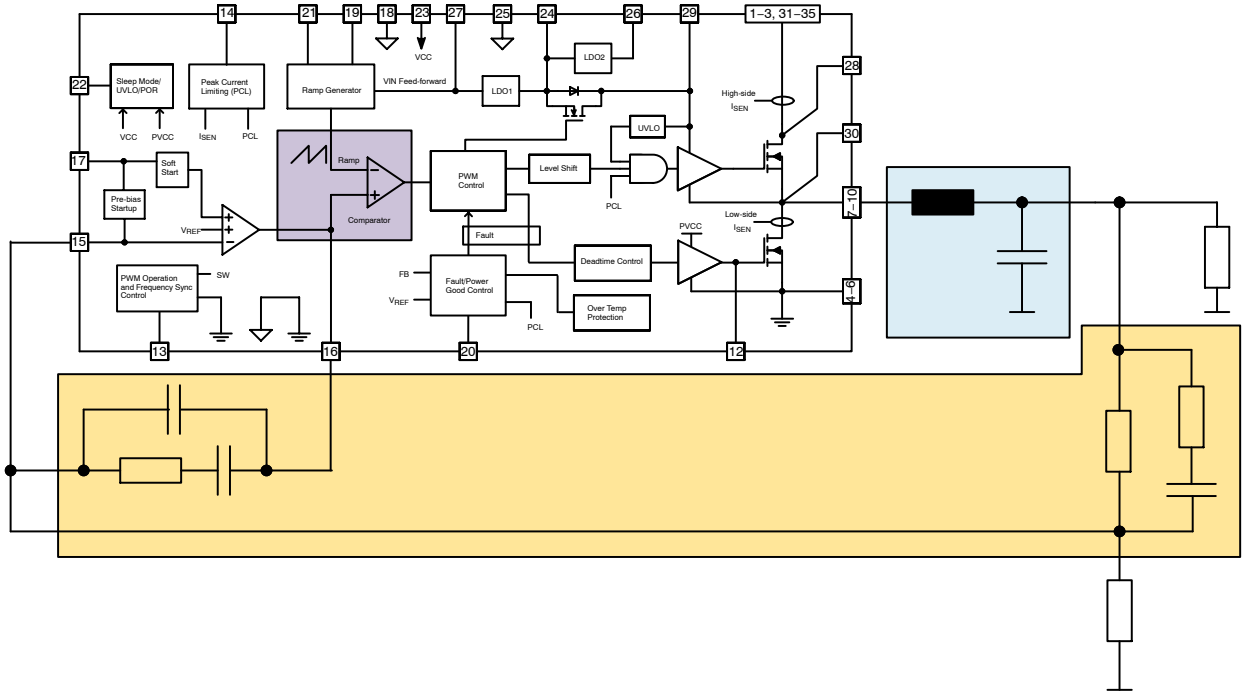



**Figure 24. FAN65004B Block Diagram**

The relevant blocks for designing the compensation are highlighted as follows:

- “Modulator Gain”: Purple
- “Output Filter”: Blue
- “Compensation Network”: Yellow

The following explanations are based on the FAN65004B evaluation board under these conditions:

**Table 1.**

| | |
|---|---|
| Input Voltage | 30.0 V |
| Output Voltage | 13.4 V |
| Load Current | 3.0 A |
| Switching Frequency | 300 kHz |

Using this device provides an easy way to understand the principles of compensation. Simple simulations based on an operational amplifier are sufficient, eliminating the need for a dedicated model.

### Modulator Gain

The first aspect considered for compensation is the modulator gain. The modulator acts as a comparator that compares the DC output voltage of the error amplifier with the sawtooth voltage on the non-inverting input (Figure 25).

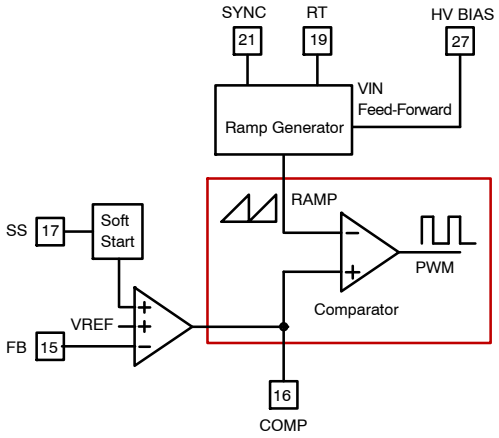



**Figure 25. PWM Comparator of FAN65004B**

Figure 26 illustrates how the modulator functions.

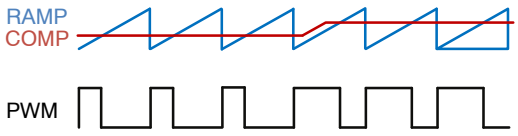



**Figure 26. PWM Generation**

In this diagram:

- The blue curve represents the sawtooth waveform, referred to as RAMP.
- The red curve represents the output of the error amplifier, referred to as COMP.

These two signals are compared by the comparator, resulting in a PWM signal whose duty cycle depends on the COMP voltage, as depicted.

This comparator circuit introduces a specific gain to the system, known as modulator gain. The gain is calculated by dividing the input voltage of the power supply by the peak voltage of the RAMP signal (Equation 7). As a result, the modulator gain is influenced by the input voltage and may change during operation, leading to unpredictable system responses. To mitigate this, most devices automatically adjust the ramp voltage to keep the ratio between VIN and VRAMP constant, thus maintaining the gain. For the FAN65004B, the gain is fixed at 28 dB, contributing to the overall system gain.

$$G_{mod} = \frac{V_{in}}{V_{ramp}} = 20 \cdot \log\left(\frac{V_{in}}{V_{ramp}}\right) \quad \text{(eq. 7)}$$

### Output Filter

The next component of the converter to consider is the LC output filter. It is essential to include the parasitic elements of the components – namely, the DC resistance of the inductor and capacitor – to achieve accurate results that align with reality.

The LC filter consists of two storage elements (the inductor and capacitor), resulting in two poles at the same frequency, known as a “double pole”. This leads to a gain change of −40 dB per decade and a phase shift of −180°.

The series resistance of the capacitor (equivalent series resistance, or ESR) introduces a single zero, referred to as the “ESR zero”. This generates a gain change of +20 dB per decade and a phase shift of +90°.

Inductor

- Pulse PA4343.223NLT
- 22 μH inductance, 33 mΩ (typ.) DC resistance

Output Capacitance

- Taiyo Yuden UMK325AB7106KM-T
- 10 μF, 50 V, X7R, 1210
- 10x capacitors in parallel

The output capacitance is made up of ten 10 μF ceramic capacitors in parallel. At a DC voltage of 13.4 V, the effective capacitance per capacitor drops to around 5 μF due to the DC biasing effect, totaling approximately 50 μF. At 300 kHz, the nominal ESR per capacitor is around 5 mΩ. When accounting for the ten capacitors in parallel, the ideal total ESR would be 0.5 mΩ. However, due to solder joints and PCB resistance, the actual total ESR is estimated to be between 3 and 5 mΩ. For subsequent calculations, an ESR of 4 mΩ will be used.

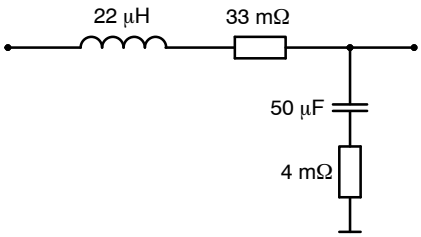



**Figure 27. LC Output Filter**

Calculation of the double pole frequency and the zero frequency is required to create the Bode plot. The LC resonant frequency, which forms the double pole, is determined by the inductance and the effective output capacitance, yielding a frequency of 4.8 kHz (Equation 8).

$$f_{LC} = \frac{1}{2 \cdot \pi \sqrt{L \cdot C_{out}}} = \frac{1}{2 \cdot \pi \sqrt{22\ \mu H \cdot 50\ \mu F}} = 4.8\ kHz \quad \text{(eq. 8)}$$

The ESR zero is formed by the effective output capacitance and the total ESR. With 50 μF and 4 mΩ, the frequency is close to 800 kHz (Equation 9).

$$f_{ESR} = \frac{1}{2 \cdot \pi \cdot R_{ESR} \cdot C_{out}} = \frac{1}{2 \cdot \pi \cdot 4\ m\Omega \cdot 50\ \mu F} = 796\ kHz \quad \text{(eq. 9)}$$

The Bode plot of the output filter, considering the double pole and zero, is depicted in Figure 28.

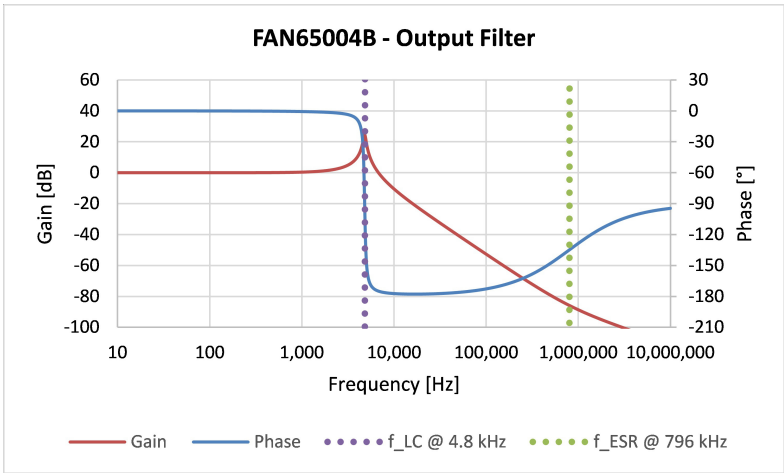



**Figure 28. Bode Plot of LC Output Filter**

The LC resonant frequency is indicated by the purple dotted line. Beyond this point, the gain declines at a rate of −40 dB per decade, while the phase shifts from 0° to −180°.

The magnitude of gain peaking and the steepness of the phase shift depend on the filter's quality factor and load:

- A low DC resistance in the inductor, low ESR, and low load result in a higher peak and steeper phase shift.
- Conversely, high DC resistance, high ESR, and high load lead to a lower peak and gentler slope.

Though it is possible to calculate the peak, it will not be considered in this context.

The frequency of the ESR zero is marked by the green dotted line. This zero causes a gain increase of +20 dB per decade, which flattens the gain plot from −40 dB per decade to −20 dB per decade. It also prompts a phase recovery from −180° (caused by the double pole) to −90° at roughly 10 MHz.

### Combining Modulator Gain and Output Filter

The modulator gain of the FAN65004B is +28 dB, as previously discussed. This gain combines with the power stage and is represented by the operational amplifier shown in Figure 29.

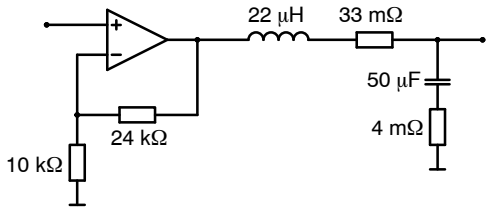



**Figure 29. Modulator Gain and Output Filter**

The Bode plot in Figure 30 for the output filter and modulator closely resembles that of the output filter itself, but the gain curve is shifted up by +28 dB. The shape of the gain curve remains unchanged, and the phase is unaffected.

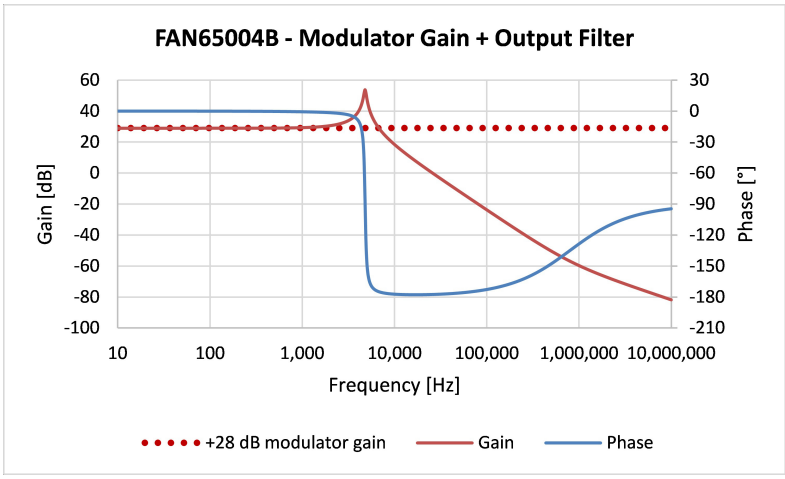



**Figure 30. Bode Plot of Modulator Gain and Output Filter**

### Relevant Frequency Range

To illustrate the impact of the ESR zero, the frequency range of the Bode plot in Figure 30 extends up to 10 MHz. This raises a relevant question: what is the maximum frequency to consider for a switch-mode power supply?

The sampling theorem states that the sampling frequency must be at least twice the maximum frequency you wish to sample. If this criterion is not met, it is impossible to accurately reconstruct the original signal. In the case of a switch-mode power supply, the sampling frequency is equivalent to the switching frequency. Therefore, the valid frequency range for a Bode plot is limited to half of the switching frequency.

Consequently, the maximum frequency for the Bode plat is set to 150 kHz, as the switching frequency in this case is 300 kHz (Figure 31).

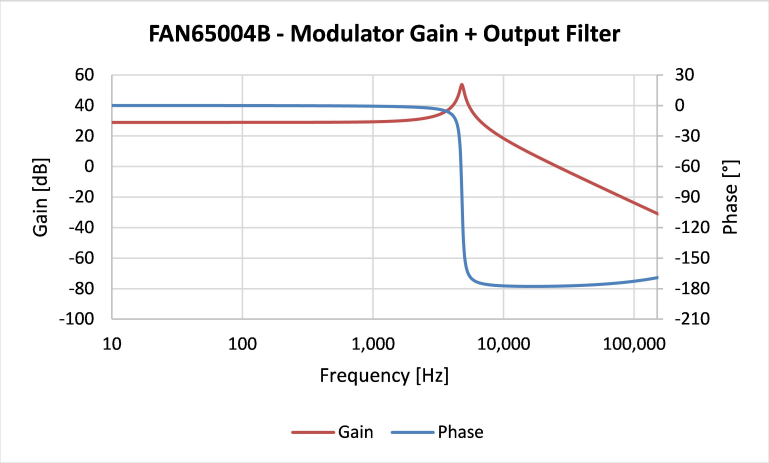



**Figure 31. Bode Plot with Relevant Frequency Range**

The minimum frequency of the Bode plot should be well below the crossover frequency to provide a clear understanding of the curve's progression. Typical values for the minimum frequency are 10 Hz and 100 Hz.

### Combining Modulator Gain, Output Filter and Error Amplifier

The preceding sections analyzed the effects of modulator gain and output filter on the system's gain and phase characteristics. The error amplifier (without compensation for now) is necessary to create a negative feedback voltage loop. Its inverting configuration introduces an additional phase shift of +180°.

In the Bode plot shown in Figure 32, the purple curve represents the phase without the error amplifier's phase shift, while the blue curve reflects the phase including the +180° shift.

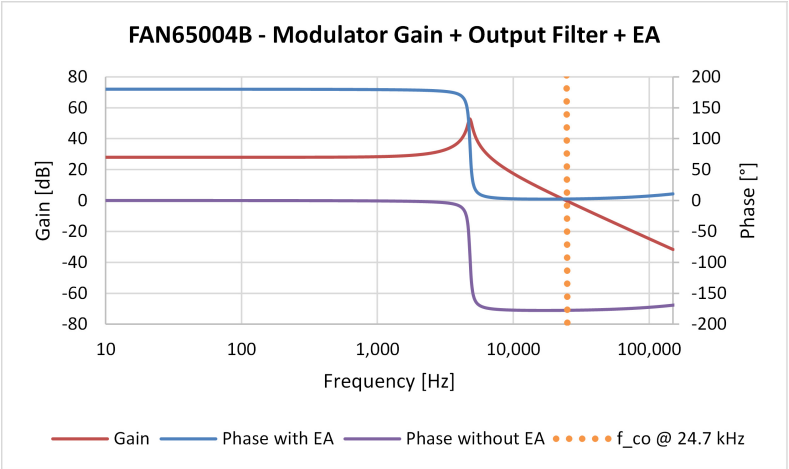



**Figure 32. Bode Plot of Modulator Gain, Output Filter and Error Amplifier**

Both configurations are indicated with the same colors in the schematic.

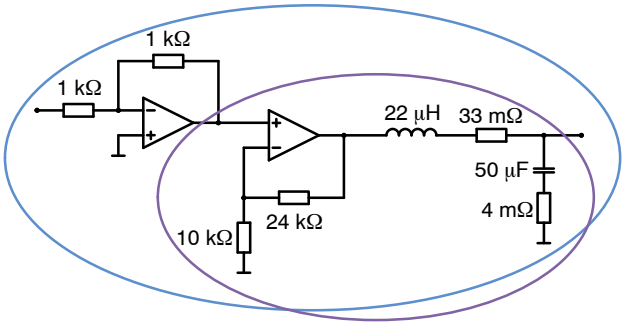



**Figure 33. Modulator Gain, Output Filter and Error Amplifier**

Currently, the crossover frequency is set at 25 kHz. Without the error amplifier, the phase is −178°, and the system would be stable. However, since there is no regulation, this is not advantageous.

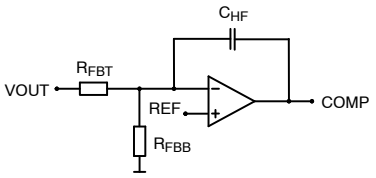
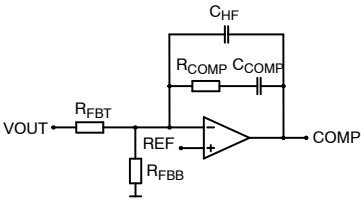
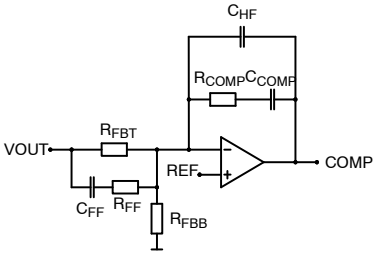
Introducing the error amplifier into the circuit brings the phase to −2° at 25 kHz, which is nearly zero. This indicates that the overall feedback at this frequency is positive and could lead to instability.

To regulate the output voltage, negative feedback is essential. However, adding just the error amplifier would result in instability. To ensure circuit stability, a compensation network is integrated into the error amplifier to provide additional phase at the desired crossover frequency.

## COMPENSATION

There are generally three types of compensation networks used in switch-mode power supplies:

**Table 2.**

| Type | Circuit | Setting | Typical Usage |
|---|---|---|---|
| 1 |   | • 1x Pole | Debugging |
| 2 |   | • Gain<br>• 1x Pole<br>• 1x Zero<br>• Pole at the Origin | Current Mode Controllers |
| 3 |   | • Gain<br>• 2x Pole<br>• 2x Zero<br>• Pole at the Origin | Voltage Mode Controllers |

Type 1 compensation is straightforward, consisting of a single pole. It is primarily used for debugging purposes. If a converter is unstable and it is unclear whether the issue arises from layout or compensation, a 100 nF or 1 µF capacitor is introduced for compensation. This configuration acts as an integrator, resulting in a low bandwidth but providing high phase and gain margins. If the instability is resolved, it indicates that the issue is likely related to compensation rather than layout.

Type 2 compensation incorporates one pole and one zero, along with a pole at the origin created by the integrator formed with the feedback resistor ($R_{FBT}$) and the capacitors ($C_{COMP}$ and $C_{HF}$). This type is commonly used for current-mode controllers.

Type 3 compensation consists of two poles and two zeros, along with a pole at the origin introduced by the same integrator setup as Type 2. This compensation is typically employed for voltage mode controllers and will serve as the foundation for subsequent calculations.

### Locations of Poles and Zeros

In Type 3 compensation, the positions of the two poles and two zeros are dependent on the power stage of the buck converter. It is crucial to distinguish whether the frequency of the ESR zero is higher than half of the switching frequency or falls between the desired crossover frequency and half the switching frequency.

- First Case: This applies to all-ceramic output capacitances with an ESR in the single-digit mΩ range.
- Second Case: This applies when low ESR electrolytic output capacitors (such as polymer capacitors) are used, where ESR is in the double-digit mΩ range.

For both cases, zeros should be positioned around one-half of the resonant frequency of the output filter, or even at the resonant frequency itself. Zeros help to compensate for the phase shift of the output filter and improve phase margin.

The placement of the poles varies based on the ESR. In the first case with very low ESR, both poles should be located around one-half of the switching frequency to ensure a −20 dB per decade roll-off and provide gain margin. In the second case with higher ESR, one pole is set at the frequency of the ESR zero, while the other pole is placed at half of the switching frequency.

These guidelines serve as reliable starting points, but it is highly recommended to verify and optimize based on measurements of the Bode plots using a network analyzer.

**Table 3.**

| Variant | Zero Location | Pole Location |
|---|---|---|
| $f_{ESR}$ > ½ $f_{switch}$ (all ceramic) | Both at ½ $f_{LC}$ | Both at ½ $f_{switch}$ |
| $f_{co}$ < $f_{ESR}$ , ½ $f_{switch}$ (low ESR electrolytic) | | One pole at $f_{ESR}$ and one pole at ½ $f_{switch}$ |

The Bode plot for Type 3 compensation is illustrated in Figure 34.

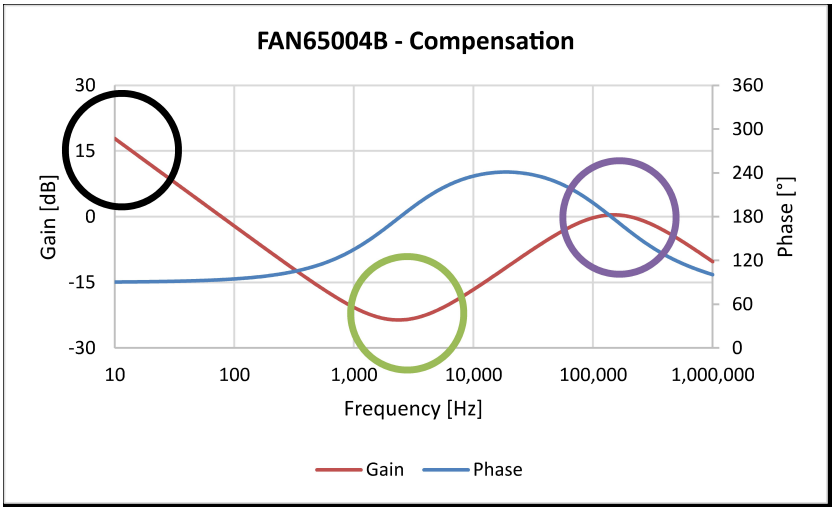



**Figure 34. Bode Plot of a Type 3 Compensation**

In the Bode plot, the gain declines at −20 dB per decade due to the pole at the origin, indicated by a black circle. The locations of the two zeros are marked by the green circle; each zero contributes a gain change of +20 dB per decade. Consequently, the resulting slope becomes +20 dB per decade. The locations of the two poles, indicated by the purple circles, result in a final slope of −20 dB per decade, as each pole reduces the slope by −20 dB per decade. The phase shifts begin at +90°, increase to +270° due to the two zeros, and decrease back down to 90° as influenced by the poles.

The gain, along with the positions of the poles and zeros, is determined by resistors and capacitors connected to the error amplifier, as shown in Figure 35. These components are color-coded to match the Bode plot.

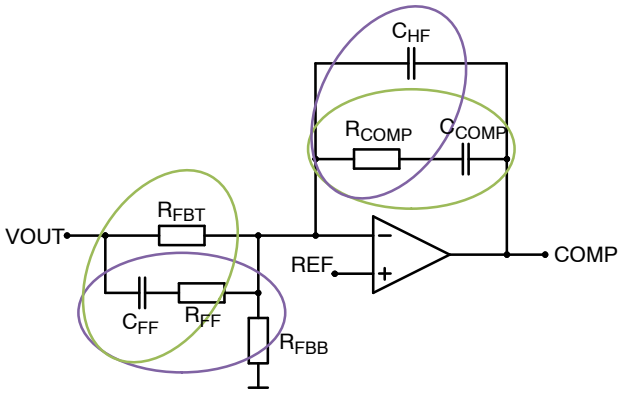



**Figure 35. Error Amplifier with Type 3 Compensation**

The DC gain is regulated by the resistors $R_{FBT}$ and $R_{COMP}$ (Equation 10), which adjust the gain curve vertically without affecting the phase or overall shape of the curve.

$$G = \frac{R_{COMP}}{R_{FBT}} \quad \text{(eq. 10)}$$

The frequencies of the poles and zeros can be calculated using the following formulas:

$$f_{Z1} = \frac{1}{2 \cdot \pi \cdot (R_{FBT} \cdot C_{FF})} \quad \text{(eq. 11)}$$

$$f_{Z2} = \frac{1}{2 \cdot \pi \cdot (R_{COMP} \cdot C_{COMP})} \quad \text{(eq. 12)}$$

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot (R_{FF} \cdot C_{FF})} \quad \text{(eq. 13)}$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot (R_{COMP} \cdot C_{HF})} \quad \text{(eq. 14)}$$

$$f_{P3} = \frac{1}{2 \cdot \pi \cdot (R_{FBT} \cdot C_{COMP})} \quad \text{(eq. 15)}$$

**Crossover Frequency**

When starting the design of the compensation for a voltage-mode buck converter, the first step is to select the crossover frequency. Typically, this frequency is set to be between one-tenth and one-fifth of the switching frequency. In the case of isolated topologies and boost converters, the bandwidth is generally lower for various reasons. Generally, a higher bandwidth leads to a better transient response.

For this example, a crossover frequency of approximately 10 kHz is targeted, consistent with the evaluation board. Currently, without compensation, the crossover frequency is 25 kHz (Figure 36).

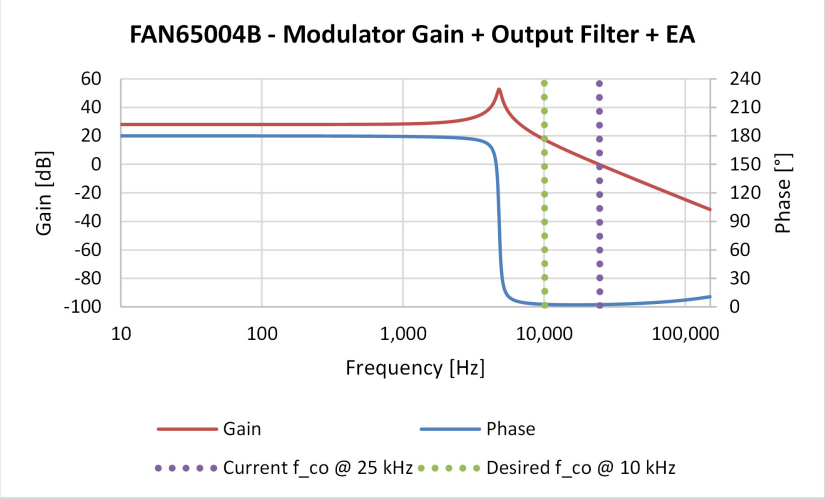



**Figure 36. Bode Plot of Modulator Gain, Output Filter and Error Amplifier**

At 10 kHz, the gain is +17 dB. To achieve the desired crossover frequency of 10 kHz, the gain curve needs to be shifted down by −17 dB.

To determine the appropriate values for the resistors $R_{FBT}$ and $R_{COMP}$ and to set the proper gain, two pieces of information are required:

1. The Bode plot of the output filter, including the modulator gain.
2. A basic understanding of the shape of type 3 compensation, which is always consistent.

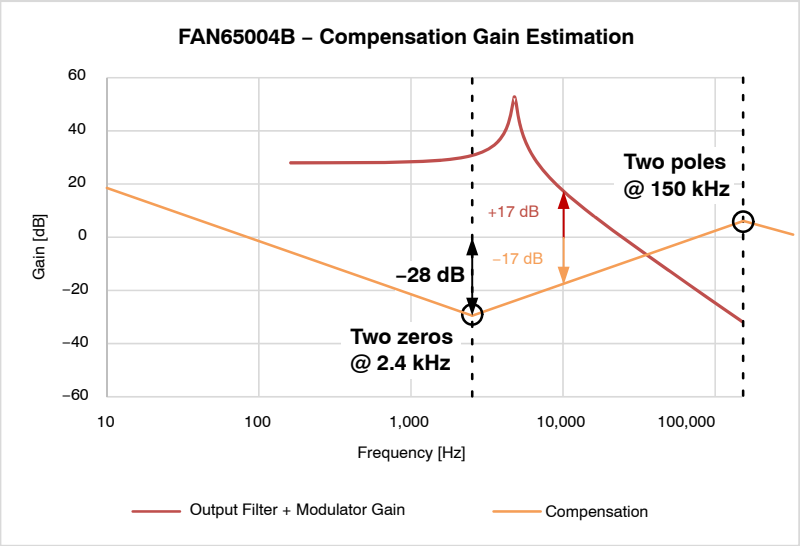



**Figure 37. Compensation Gain Estimation**

The process involves four steps to determine the necessary gain:

1. Determine the gain at the desired crossover frequency, which is +17 dB in this case.
2. To bring the gain curve down to 0 dB, the compensation needs a gain of −17 dB at 10 kHz. Given that the compensation gain curve exhibits a slope of +20 dB per decade at the crossover frequency, a line is drawn in the Bode plot starting at –17 dB at 10 kHz with this slope.
3. Mark the frequency of the double zero on this line; for this example, it is 2.4 kHz.
4. Read the gain at this frequency, which is −28 dB. This corresponds to a DC gain factor of 0.04, which is required for the compensation to set the crossover frequency at 10 kHz.

$R_{FBT}$ is fixed at 20 kΩ and should remain unchanged because it also determines the output voltage (Figure 38 – Gain Setting).

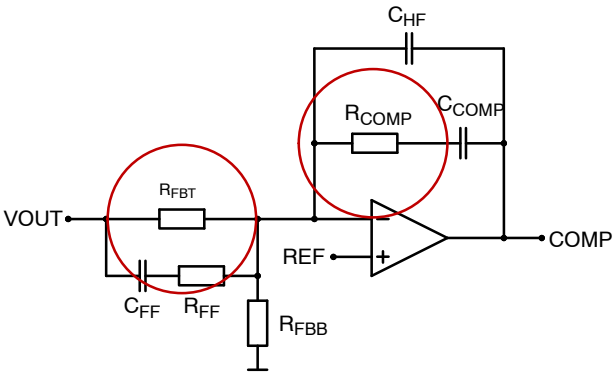



**Figure 38. Gain Setting**

According to the calculations (Equation 16), $R_{COMP}$ needs to be 796 Ω. To match the evaluation board, a resistance value of 680 Ω is used.

$$G = \frac{R_{COMP}}{R_{FBT}}$$

$$R_{COMP} = G \cdot R_{FBT} = 0.04 \cdot 20\ k\Omega = 796\ \Omega \quad \text{(eq. 16)}$$

### Placement of Poles and Zeros

After setting the gain, the next step is to place the poles and zeros.

As explained earlier, zeros are typically positioned at one-half of the switching frequency for a voltage-mode buck converter, which in this case is 2.4 kHz. The frequency of the zeros is set by $R_{FBT}$ and $C_{FF}$, as well as $R_{COMP}$ and $C_{COMP}$ (Figure 39). Since the resistors have already been defined by the gain calculation, the capacitors marked in green need to be set accordingly.

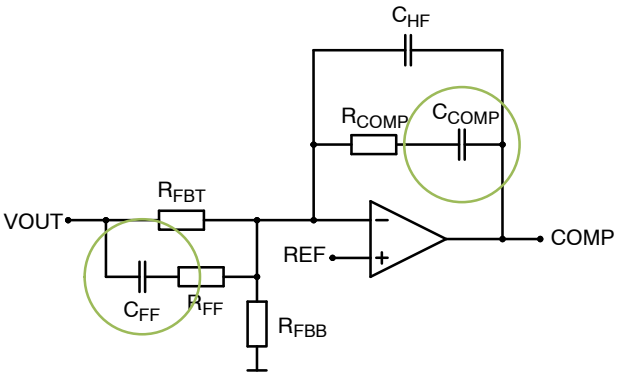



**Figure 39. $C_{FF}$ and $C_{COMP}$**

For the first zero, $C_{FF}$ should be set to 3.3 nF, and for the second zero, $C_{COMP}$ should be set to 97.5 nF (Equation 17, Equation 18).

$$f_{Z1} = \frac{1}{2 \cdot \pi \cdot (R_{FBT} \cdot C_{FF})}$$

$$C_{FF} = \frac{1}{2 \cdot \pi \cdot (R_{FBT} \cdot f_{Z1})} = \frac{1}{2 \cdot \pi \cdot (20\ k\Omega \cdot 2.4\ kHz)} = 3.3\ nF \quad \text{(eq. 17)}$$

$$f_{Z2} = \frac{1}{2 \cdot \pi \cdot (R_{COMP} \cdot C_{COMP})}$$

$$C_{COMP} = \frac{1}{2 \cdot \pi \cdot (R_{COMP} \cdot f_{Z2})} = \frac{1}{2 \cdot \pi \cdot (680\ \Omega \cdot 2.4\ kHz)} = 97.5\ nF \quad \text{(eq. 18)}$$

The closest standard values available are 3.3 nF and 100 nF, which align well with the evaluation board.

The final step involves placing the poles.

Due to the low ESR of the ceramic output capacitors, both poles are set to one-half of the switching frequency, which is 150 kHz.

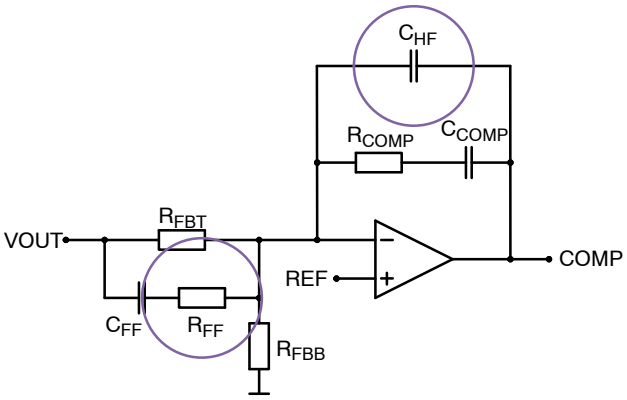



**Figure 40. $R_{FF}$ and $C_{HF}$**

The first pole is defined by $R_{FF}$ and $C_{FF}$. Since $C_{FF}$ has already been determined in previous calculations for the zeros, $R_{FF}$ must now be calculated, as indicated in Figure 40. The second pole is defined by $R_{COMP}$ and $C_{HF}$; with $R_{COMP}$ established during the gain calculations, $C_{HF}$ must now be calculated, also marked in purple.

$$f_{P1} = \frac{1}{2 \cdot \pi \cdot (R_{FF} \cdot C_{HF})}$$

$$R_{FF} = \frac{1}{2 \cdot \pi \cdot (C_{HF} \cdot f_{P1})} = \frac{1}{2 \cdot \pi \cdot (3.3\ nF \cdot 150\ kHz)} = 322\ \Omega \quad \text{(eq. 19)}$$

$$f_{P2} = \frac{1}{2 \cdot \pi \cdot (R_{COMP} \cdot C_{HF})}$$

$$C_{HF} = \frac{1}{2 \cdot \pi \cdot (R_{COMP} \cdot f_{P2})} = \frac{1}{2 \cdot \pi \cdot (680\ \Omega \cdot 150\ kHz)} = 1.6\ nF \quad \text{(eq. 20)}$$

To match the values on the evaluation board, $R_{FF}$ is set to 280 Ω and $C_{HF}$ to 1.8 nF, both of which are very close to the calculated values.

### Closing the Loop

To obtain the complete Bode plot of the buck converter as a closed-loop system, you need to sum the Bode plots of the output filter (Figure 36) and the compensation network (Figure 37).

Summing the gain and phase at each frequency produces the Bode plot shown in Figure 41, which displays the characteristic response of a voltage-mode buck converter.

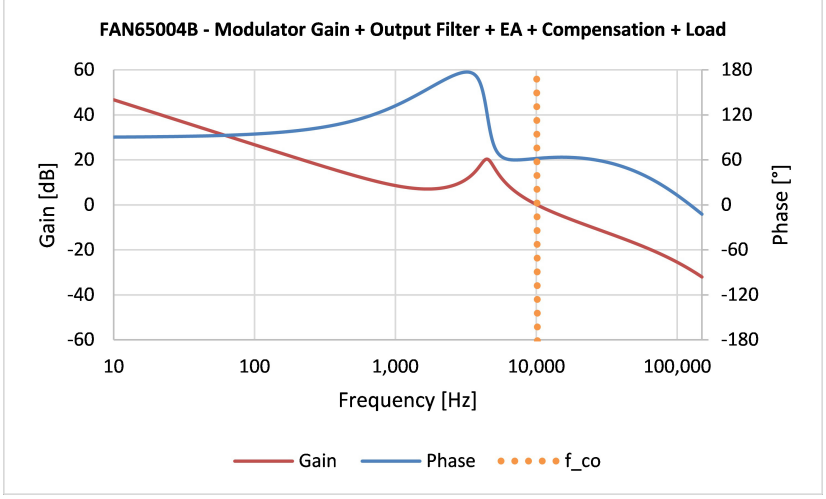



**Figure 41. Bode Plot of the Closed Loop System**

The crossover frequency is 9.5 kHz, with a phase margin of 62° and a gain margin of −31 dB. The bandwidth aligns with expectations, providing ample phase and gain margins. Overall, this is an example of a robust compensation network design.

The frequency response of the entire converter can be simulated using the simple schematic illustrated in Figure 42. Although the operational amplifiers are represented as ideal models, the gain bandwidth and DC gain must be constrained to the specifications of the FAN65004B error amplifier (10 MHz, 80 dB).

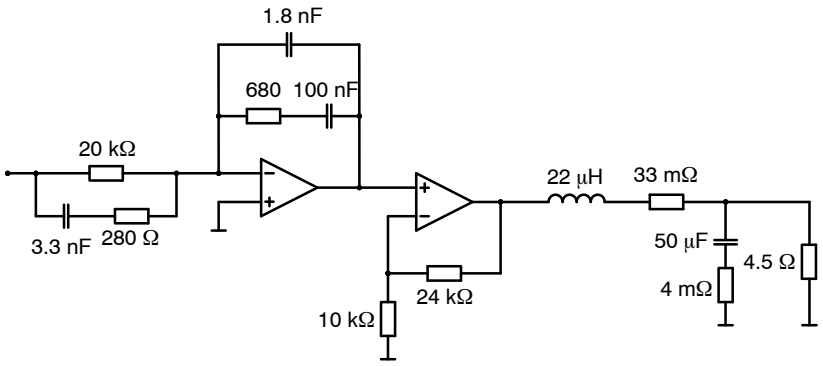



**Figure 42. Simulation Model**

## Measurement

Verification of the calculations and simulated results is performed by measuring the Bode plot of the FAN65004B evaluation board (Figure 43).

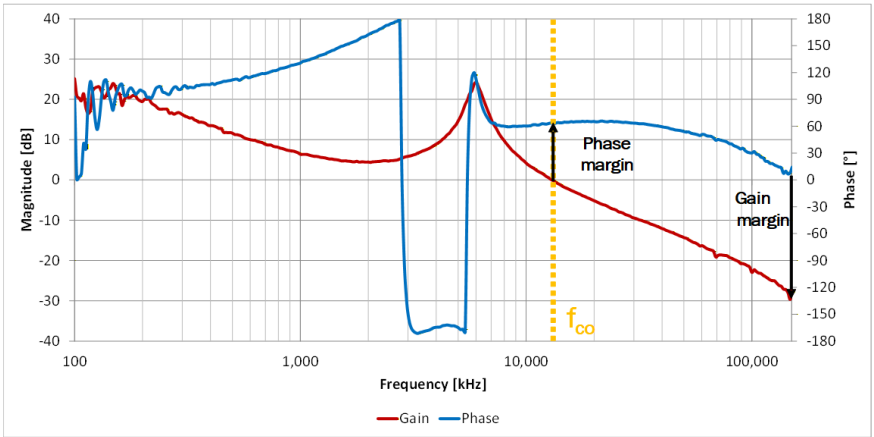



**Figure 43. FAN65004B Evaluation Board Bode Plot**

Table 4 presents the comparison of results from calculations/simulations with the measurements. On the evaluation board, the crossover frequency is slightly higher, but the phase and gain margins are nearly identical. Due to component tolerances, some deviations are expected; however, the overall results match very well.

**Table 4.**

| | Crossover Frequency | Phase Margin | Gain Margin |
|---|---|---|---|
| **Calculation / Simulation** | 9.5 kHz | 62° | −31 dB |
| **Measurement** | 12.1 kHz | 64° | −29 dB |

## OPTIMIZATION

Substantial phase and gain margins in this example allow for an increase in crossover frequency to improve transient response, with a target of 30 kHz.

Tripling the crossover frequency will reduce the voltage deviation during a load step by a factor of three. Alternatively, you can maintain the same load step response while reducing the output capacitance by a factor of three.

To achieve the new target crossover frequency of 30 kHz, the gain curve must be shifted upward without altering its shape or affecting the phase. This means the frequencies of the poles and zeros must remain the same.

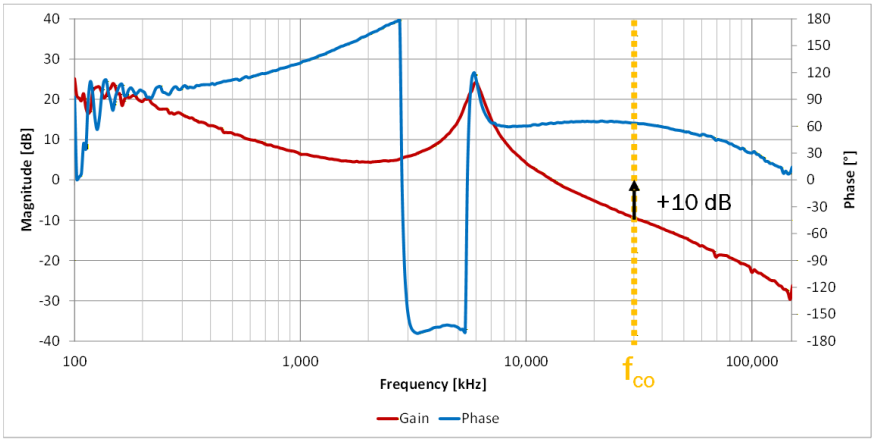



**Figure 44. Bode Plot of Initial Compensation**

Figure 44 illustrates that the gain curve needs to be increased by +10 dB to set 30 kHz as the new crossover frequency. By retaining the existing poles and zeros, the expected phase margin remains around 60° and the gain margin is approximately −20 dB.

**Table 5.**

| | |
|---|---|
| New Gain | +10 dB (factor 3.2) |
| Zero 1 | 2.4 kHz |
| Zero 2 | 2.4 kHz |
| Pole 1 | 172 kHz |
| Pole 2 | 130 kHz |

### Detailed Method

The current gain is –29.4 dB (Equation 21); increasing it by +10 dB results in –19.4 dB, corresponding to a factor of 0.11.

$$G_{ACTUAL} = \frac{R_{COMP}}{R_{FBT}} = \frac{680\ \Omega}{20\ k\Omega} = 0.034 = -29.4\ dB$$

$$G_{NEW} = G_{ACTUAL} + 10.0\ dB = -29.4\ dB + 10.0\ dB = -19.4\ dB = 0.11 \quad \text{(eq. 21)}$$

Establishing the new gain requires adjusting either $R_{FBT}$ or $R_{COMP}$, but since $R_{FBT}$ also sets the output voltage, only $R_{COMP}$ should be modified.

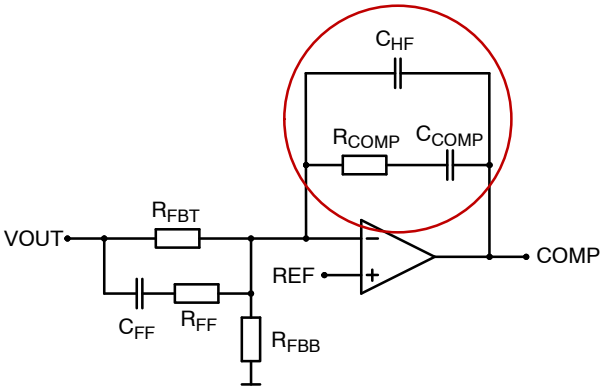



**Figure 45. Components for Modification**

$$R_{COMP,NEW} = G_{NEW} \cdot R_{FBT} = 0.11 \cdot 20\ k\Omega = 2.2\ k\Omega \quad \text{(eq. 22)}$$

With the new resistor value set at 2.2 kΩ, the gain will be −19.4 dB.

Adjusting $R_{COMP}$ will also affect the frequency of one zero and one pole. The red circle in Figure 45 highlights all components that must be modified.

The zero frequency is determined by $R_{COMP}$ and $C_{COMP}$. To maintain a zero frequency of 2.4 kHz with a new resistance of 2.2 kΩ, the value of $C_{COMP}$ needs to be adjusted to 33 nF (the next closest standard value).

$$C_{COMP,NEW} = \frac{1}{2 \cdot \pi \cdot \left(R_{COMP} \cdot f_{Z2}\right)} = \frac{1}{2 \cdot \pi \cdot (2.2\ k\Omega \cdot 2.4\ kHz)} = 30.1\ nF \quad \text{(eq. 23)}$$

The pole frequency is determined by $R_{COMP}$ and $C_{HF}$. Maintaining the pole at 130 kHz requires a capacitance of 560 pF, which is the nearest standard value.

$$C_{HF,NEW} = \frac{1}{2 \cdot \pi \cdot \left(R_{COMP} \cdot f_{P2}\right)} = \frac{1}{2 \cdot \pi \cdot (2.2\ k\Omega \cdot 130\ kHz)} = 556\ pF \quad \text{(eq. 24)}$$

### Quick Method

While the previous method provided detailed adjustments, the process can be streamlined. To increase the gain by a factor of 3.2, simply multiply the value of RCOMP by this factor, yielding 2.2 kΩ. For subsequent calculations, the factor is simplified to 3.

$$\text{Ratio} = \frac{R_{COMP,NEW}}{R_{COMP}} = \frac{2.2\ k\Omega}{680\ \Omega} = 3.2 \approx 3 \quad \text{(eq. 25)}$$

To maintain the frequencies of the pole and zero, the capacitors must be reduced by the same factor as the resistor is increased.

$$C_{COMP,NEW} = \frac{C_{COMP,OLD}}{3} = \frac{100\ nF}{3} \approx 33\ nF \quad \text{(eq. 26)}$$

$$C_{HF,NEW} = \frac{C_{HF,OLD}}{3} = \frac{1800\ pF}{3} \approx 560\ pF \quad \text{(eq. 27)}$$

The value of $C_{COMP}$ changes from 100 nF to 33 nF, and CHF changes from 1800 pF to 560 pF.

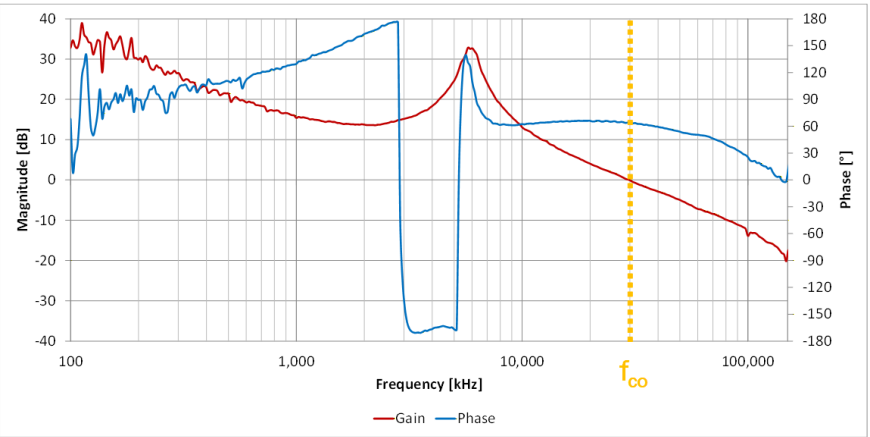



**Figure 46. Bode Plot of Optimized Compensation**

The optimized compensation results in a crossover frequency of 30.9 kHz, a phase margin of 64°, and a gain margin of −18 dB. Despite significantly increasing the bandwidth, the device still exhibits a substantial phase and gain margin.

This demonstrates a strong correlation between theoretical predictions and practical measurements, while also providing a straightforward method for optimizing compensation with minimal calculations.

## REVISION HISTORY

| Revision | Description of Changes | Date |
|---|---|---|
| 0 | Initial document release. | 1/16/2026 |



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