Using Cascode SiC JFETs in LLC Primary

AND90415/D

Abstract

Cascode SiC JFETs (CJFETs) combine beneficial characteristics such as high voltage blocking, low conduction loss, fast switching speed, and low gate charge (0–12 V gate drive), making them attractive for LLC resonant converters. However, their high turn-off dv/dt can excite sustained ringing, leading to voltage overshoot, EMI, and oscillation in the worst cases, especially when operating above the resonant frequency where primary switching current can be high (e.g., > 30 A for 750 V devices). This note provides top-level design guidance for CJFET when used in high switching frequency ZVS applications and demonstrates that a capacitor snubber (C-snubber) placed in parallel with the primary devices is a simple and effective way to control dv/dt and reduce switching loss, with quantified trade-offs in magnetizing current or dead time. Measured data show efficiency gains in high switching current LLC designs when a C-snubber is used in parallel with CJFET.

Benefits of Cascoded SiC JFETs in LLC Primary

CJFETs are well suited to the LLC primary due to below characteristics:

- High voltage rating: suitable for high voltage dc bus input applications such as those 400 V or 800 V used in data centers.
- Low Rds(on): Reduced conduction loss compared with conventional SiC and Si MOSFETs in the same voltage ratings.
- High switching speed: Small charges (stored in C_{oss}) to be removed to maintain ZVS at minimum dead time.

Figure 1 shows the $R_{ds(on)}$ comparison of TOLL packaged devices in similar voltage ratings but using different technologies. CJFET has much lower $R_{ds(on)}$ compared to other devices using different technologies while providing 100 V extra V_{ds} rating.

Figure 2 shows the typical C_{oss} of 650 V or 750 V rated power devices with similar $R_{ds(on)}$and same TO-247 package. In general, SiC devices have much lower C_{oss} than Si devices.

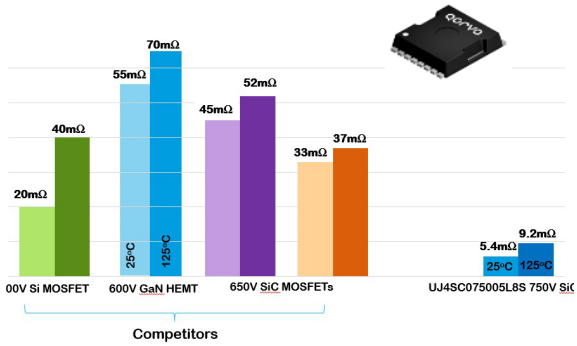

Figure 1. CJFET 's Best-in-class FOM $R_{ds(On)}$ x(Chip Area) Enables Lowest On-resistance in any Given Package

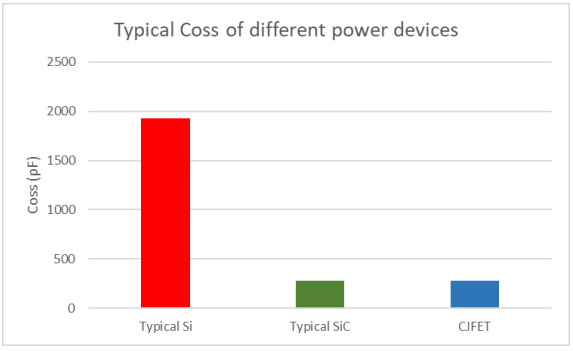

Figure 2. C_{oss} Among Different Devices in TO-247 Package, 650 V to 750 V Ratings, and Similar $R_{ds(on)}$'s

Controlling CJFET Turn-off dv/dt with External Cds

For CJFETs, increasing R_g reduces gate current as in the gate control of a regular MOSFET, but it is not effective at controlling V_{ds} slew rate (dv/dt) due to CJFET's very low C_{gd}. A device-parallelling (drain-to-source) snubber is more effective for turn-off dv/dt control. An RC snubber provides broad-band damping with a tradeoff of additional resistive loss for control of ringing, and a pure C snubber provides dv/dt control without power dissipation for ZVS applications like LLC.

Assuming negligible current flowing through the device conduction channel during fast turn-off transients, for a Half Bridge (HB) configuration, dv/dt is proportional to the instantaneous current being commutated (I_{sw}):

$$\frac{dv}{dt} \approx \frac{I_{SW}}{2\left(C_{oss(HV)} + C_{ds}\right)} \quad \text{(eq. 1)}$$

Where I_{sw} is the switching current and assumed to be magnetizing current peak (I_{m_pk}) in an LLC in this application note, is the average in the V_{ds} section where C_{oss} is relatively flat and the highest dv/dt is measured, as shown in Figure 3 for NTBT023N075CJ4 (TOLT package) as an example. Only this part of capacitance is used in the equation since it is the lowest average output capacitance to generate the measured highest dv/dt during the transient. Reading from Figure 3, $C_{oss(HV)}$ is approximately 160 pF.

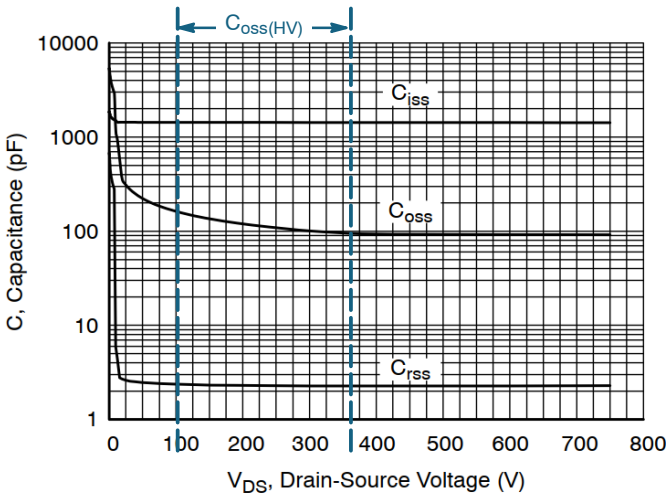

Figure 3. Definition of the Typical Capacitances of NTBT023N075CJ4 in the V_{ds} Section that Generating Highest dv/dt

Using NTBT023N075CJ4 working in 400 V dc bus as an example, the dv/dt can be estimated against switching currents based on eq 1. A family of curves without and with different external C_{ds}' is plotted in Figure 4 below. For designs with different switching current, these curves can be used to determine the C_{ds} needed to control dv/dt. For example, if this device is selected as the primary switch in a high switching frequency LLC converter and the magnetizing current peak I_{m_pk} is determined to be 10 A, the estimated dv/dt is approximately 31 V/ns. If this dv/dt is acceptable in considering the V_{ds} overshoot, oscillation tendency, and EMI, no external C_{ds} is necessary for normal operation. However, this decision needs to be made together with all the possible working conditions an LLC converter can operate in. Transient working conditions such as startup, load step changes, and fault protective conditions where high turn-off currents may exist. C_{ds} snubber is recommended to limit the dv/dt if those high current switching conditions cannot be ruled out during system design stage. In this example assuming a dv/dt of 20 V/ns or below is required, a C_{ds} of 100 pF or higher should be used.

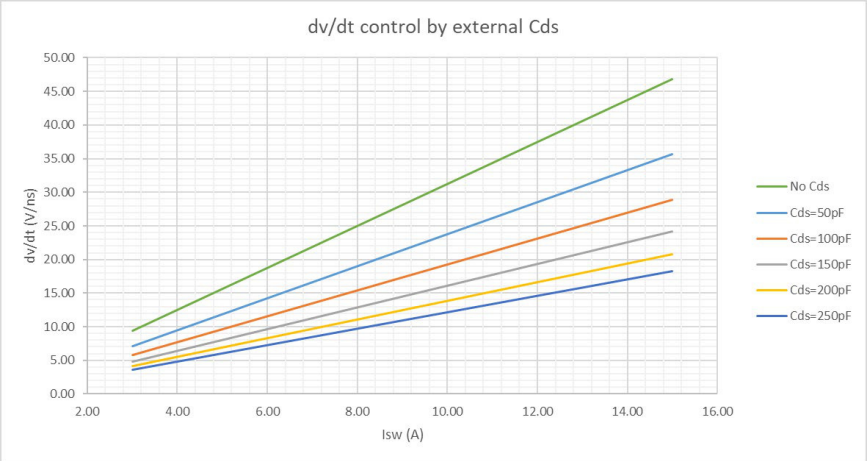

Figure 4. Turning Off dv/dt of NTBT023N075CJ4 and Controlling dv/dt by Using External Cds

Impact of External C_{ds} on Deadtime Requirements

To maintain the ZVS of a primary switch in LLC converter, the total capacitance at the switching node needs to be completely discharged before applying gate voltage to the turning on device. Assuming the switching current keeps constant during the turn-off transient, the minimum transition time T_{tr} required for ZVS is given in below equation:

$$T_{tr} \geq \frac{2\left(C_{oss(tr)} + C_{ds}\right) V_{ds}}{I_{SW}} \qquad \text{(eq. 2)}$$

Where $C_{oss(tr)}$ is the time related output capacitance of the device specified in a power device datasheet.

As can be seen in eq 2, the external C_{ds} increases the required minimum transition time. Again, using NTBT023N075CJ4 as an example, required minimum T_{tr}'s with and without external C_{ds} are plotted in Figure 5 according to eq 2. To maintain ZVS deadtime T_{dt} needs to be longer than this T_{tr}. Therefore, this plot gives the theoretical minimum of the required dead time T_{dt} for the PWM signals generated by gate controllers. In practical designs, a margin needs to be added to accommodate the time shifting tolerances at device gates due to unequal gate driving path delays, device gate threshold voltage differences from on and off gate voltages, unbalanced on/off resistances, etc. This margin is a system design decision that needs to be made with collective considerations of gate driving path component selections, on/off gate voltages, PCB layouts, etc.

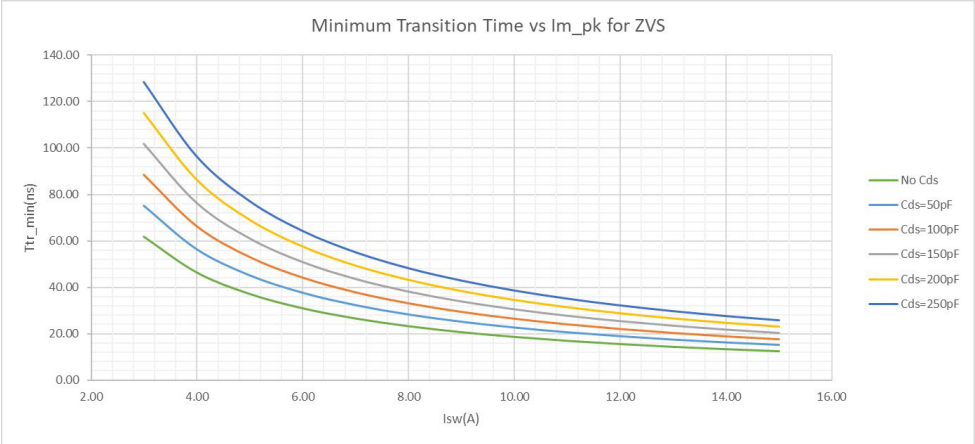

Figure 5. Minimum Dead Time Required to Maintain ZVS without and with Different External Cds

Use the same example as that used in previous section, when the switching current is 10 A and an external C_{ds} of 220 pF is used to control the dv/dt, a T_{tr} of approximately 35 ns is sufficient. To leave margin for the timing tolerances at the device gate, a deadtime T_{dt} of 75 ns is used in the test setup in this note.

Power Losses Reduction with External C_{ds}

In many applications the LLC converter needs to be operating at switching frequencies higher than their resonant frequencies. In those cases, switching devices need to turn off not only magnetizing currents but also load currents (reflected to the primary side). Since the turn-off dv/dt goes up with switching current as shown in Figure 5, an RC or pure C-snubber is recommended to limit the dv/dt for high-current turn-off events.

If a C-snubber is used in LLC converter and ZVS is maintained, it does not generate extra switching loss. On the contrary, it helps to reduce switching loss because the switching off transient current is deviated to the snubber. The stored energy in the snubber during turning off is returned to the bus before turning on the same switch, so the snubber capacitance does not generate extra power loss. This drain current deviation is explained by the tested waveforms in Figure 6.

During the turn-off transient, part of the load current (I_{Load} in the schematics) is deviated by both top and bottom snubbers C1 and C2 (I_{cs1} and I_{cs2}). Due to this current deviation, the current flowing into the device (I_{DUT}) is reduced. As a result, V–I overlapped area and the turn-off switching loss is reduced.

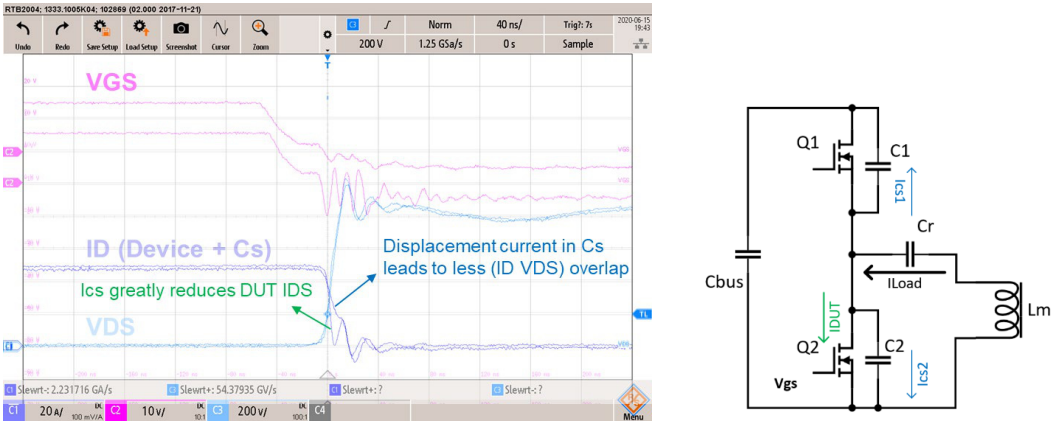

Figure 6. Waveform Comparison Shows Turn-off Current Deviations by Using Snubber

Test Result

To demonstrate the HF LLC design concepts and show the impacts of an external C_{ds} on the primary dv/dt and power losses, a hardware test setup is designed to exclude the contribution factors from an LLC converter's secondary side. This test setup schematic is shown in Figure 7. It is an HB resonant converter without loading, equivalent to an LLC converter working near or below its resonant frequency in terms of dead time requirements and switching losses in the primary side devices. Different inductances (Lm) are used to obtain different switching currents. This simulates different magnetizing inductances of the isolation transformer used in an LLC converter design. For those operating at frequencies higher than their resonant frequencies, the loading current effects on the primary switches can be included by increasing the magnetizing current peaks (I_{m_pk}) to a level beyond a normally designed range.

The gate drive voltages and on/off resistance for each device are tuned to ensure ZVS at the tested minimum switching current and 75 ns dead time. The gate drive circuit parameters in this test are listed below.

- Vgs = 0 V ~ 12 V
- Rgon = Rgoff = 5 Ω

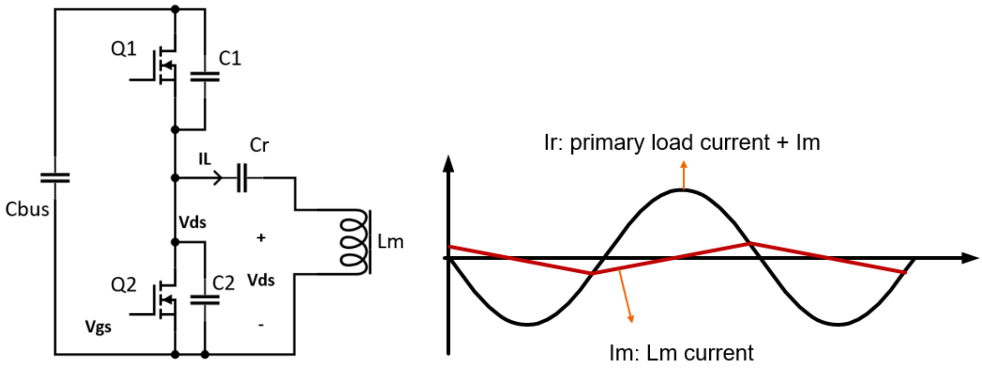

Figure 7. Hardware Simulation of an Unloaded LLC Converter. Only Lm Current is Considered in This Setup. There is No Load Current (Ir in the Simplified Waveform) in This Test

Typical CJFET operating waveforms are shown in Figure 8. These waveforms are captured when the dc input voltage is 400 V, dead time is set to 75 ns, and switching frequency is set to about 990 kHz. An inductance of 5 μH which sets the I_{m_pk} to 10 A is used. No external C_{ds} is used in this first test due to low switching currents. These waveforms show that the CJFET (NTBT023N075CJ4, TOLT package) can be used in LLC primary with a switching frequency at 1 MHz range. When the magnetizing current is designed to be around 10 A, ZVS is maintained with substantial margin.

Figure 9 is zoomed in at the turning off transient from Figure 8. The dv/dt of the V_{ds} is measured at 31.4 V/ns, very close to the estimated value given in Figure 4. With a design optimized in power loop inductances and under steady-state operations, this dv/dt should not cause switching transient issues.

With fixed switching frequency, each L_m generates a different switching current I_{sw} in this test. The total input power flowing into the circuit under test is measured for each I_{sw} and plotted in Figure 10. This total loss includes all losses in power circuit including inductance wire loss, PCB ESR loss, device losses (conduction and switching), but without loading current caused losses as in an LLC converter. As anticipated, the total loss goes up with switching current.

Majority of these losses are generated by the ESRs of the inductances used, which are measured in hundred milliohms range in this test. As in all the HF magnetic designs, winding ESRs are significant in 1 MHz frequency range. Its reduction for copper loss optimization has been a major challenge in all HF LLC designs.

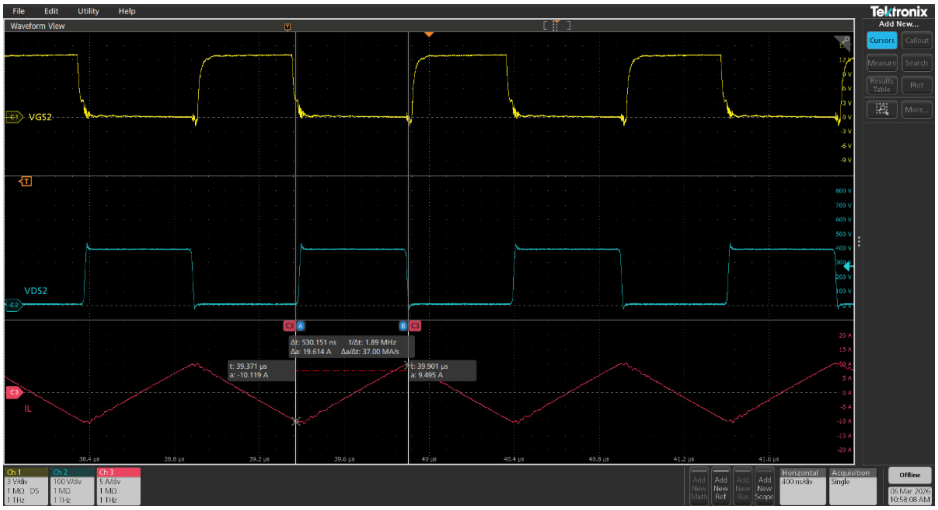

Figure 8. Typical Waveforms Taken from the Unloaded LLC Circuit, with Switching Current Isw set to 10 A. Fsw = 990 kHz, Tdt = 75 ns, and Vdc = 400 V

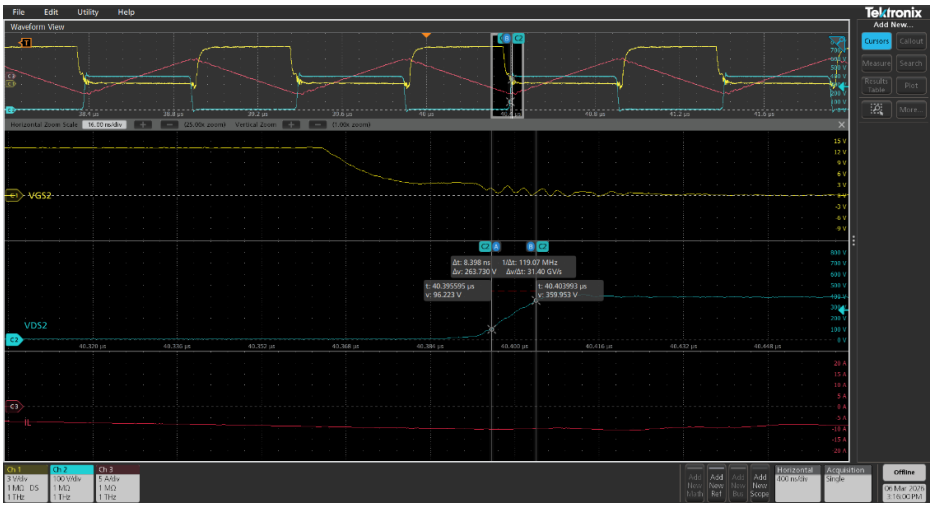

Figure 9. Zoomed-in Version of Figure 8 at Turning Off Transient

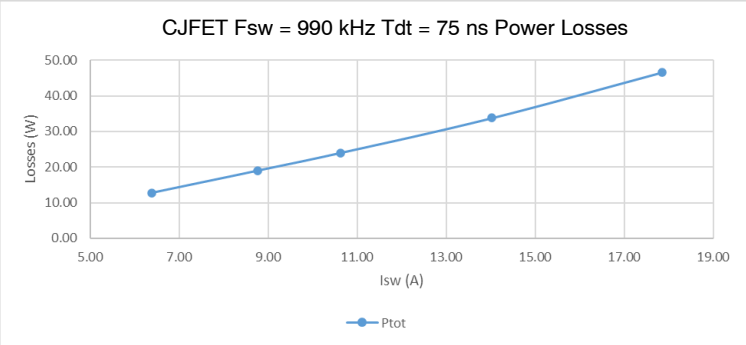

Figure 10. Total Power Losses at Different Switching Currents (I_{m_pk}, Magnetizing Current Peaks). Fsw = 990 kHz, Tdt = 75 ns, and Vdc = 400 V

Operations at 1 MHz range with an external C_{ds} is the next test. In this test a 220 pF capacitor is placed in parallel with each switch. A different inductor, 4 μH Litz wire air core inductor, is used in the resonant tank to generate a switching current of about 12 A. The key waveforms are shown in Figure 11. With a slightly bigger switching current, substantial dead time margin is achieved even with an external snubber capacitor used.

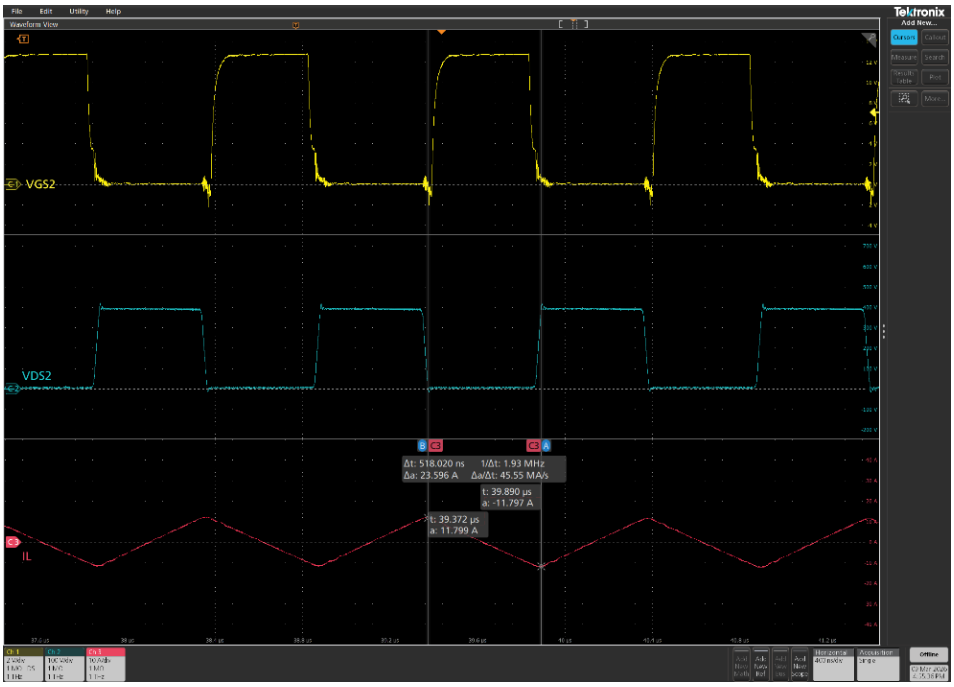

Figure 11. Waveforms when Operating at 1 MHz with a C-snubber of 220 pF in Parallel with CJFET, with Switching Current Isw set to 12 A. Fsw = 990 kHz, Tdt = 75 ns, and Vdc = 400 V

In the third test, the same 4 μH Litz wire inductor is used and the switching frequency is set to 400 kHz, but V_{dc} varies from 250 V to 425 V to obtain different switching currents. The total input power and switching node dv/dt are measured.

Figure 12 shows the dv/dt comparison with and without a 220 pF C_{ds} when switching at 400 kHz. The 220 pF C_{ds} reduces dv/dt by about half. This shows the turn-off dv/dt control effect by using snubber C_{ds}.

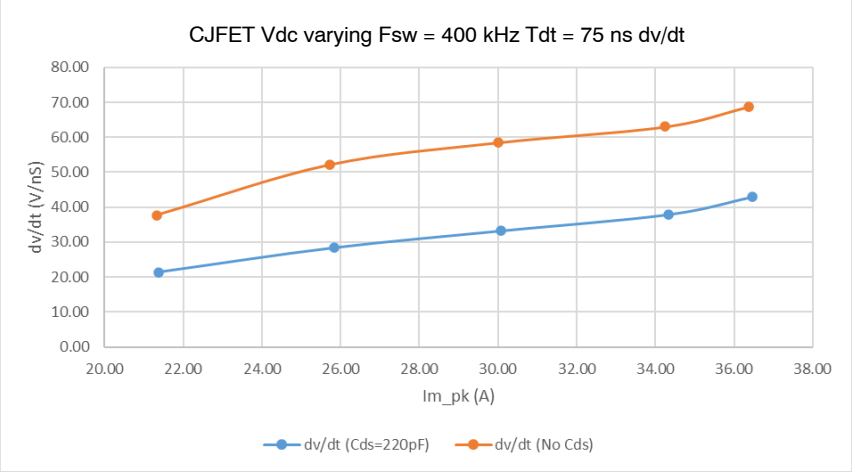

Figure 12. dv/dt Comparisons with and without an External Cds. Vdc = 400 V, Fsw = 400 kHz, and Tdt = 75 ns

Figure 13 shows the total power loss comparisons with and without a 220 pF C_{ds}. The total loss is reduced with the 220 pF C-snubber. This result matches circuit analysis in section 4. The difference is small when the switching current is small at around 20 A but becomes more evident when the switching current goes higher. At the high end of the switching currents of around 36 A, the loss difference goes to about 10 W.

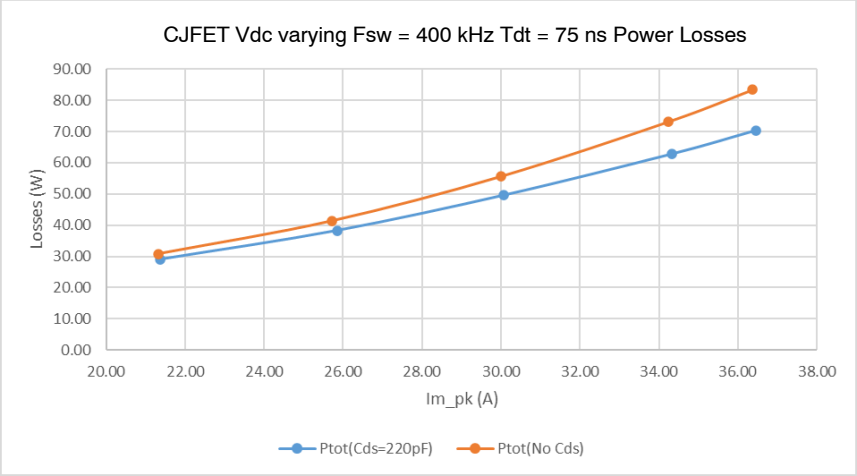

Figure 13. Total Power Losses with and without an External Cds. Vdc = 400 V, Fsw = 400 kHz, and Tdt = 75 ns

Conclusions

CJFETs provide high voltage capability, low conduction loss, and fast switching, making them excellent candidates for high voltage high frequency LLC primary stages.

For above-resonance operation (with higher switching currents), turn-off dv/dt can be excessive and trigger overshoot, oscillation, and EMI. A parallel C-snubber is a simple, effective, and low-dissipation method to control dv/dt and optimize total loss, with manageable trade-offs in dead time or switching current.

With proper component sizing and layout, the total system efficiency can be improved, while system robustness is enhanced.

References

[1] SiC Cascode JFET & Module User Guide, UM70114 – SiC Cascode JFET & Module User Guide.

[2] Choosing the Correct Semiconductor Technology for 800 V, AND90387 – Choosing the Correct Semiconductor Technology for 800 V.

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	4/22/2026

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:
Technical Library: www.onsemi.com/design/resources/technical−documentation
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