Bridging Voltage Domains: Enabling High-Performance ADAS Processors to Communicate with Automotive Peripherals Using the T30LAXT3V4T245

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Overview

Advanced driver-assistance systems (ADAS) are among the most computationally demanding automotive subsystems ever deployed in a production vehicle. Modern ADAS domain controllers rely on high-performance application processors and SoCs that are fabricated on deep-submicron CMOS nodes and operate at core I/O voltages as low as 0.9 V to 1.2 V. At the same time, the peripheral ecosystem surrounding these processors – including radar transceivers, camera serializers, LiDAR modules, safety microcontrollers (MCUs), and HMI displays-frequently operates at 3.3 V or higher I/O rails inherited from legacy automotive supply chains.

The resulting I/O voltage mismatch between the ADAS SoC and its peripheral devices is a critical hardware challenge. Without a reliable translation bridge, direct signal interconnect between a sub-1.2 V processor I/O and a 3.3 V peripheral input can cause logic-level violations, potential latch-up conditions, and erroneous behavior – any of which is unacceptable in a safety-critical system. Discrete resistor-divider approaches introduce propagation delay uncertainty and consume additional board area. An integrated, bidirectional level translator resolves these mismatches deterministically while preserving signal integrity and limiting power overhead.

onsemi's Treo level translation devices such as the **T30LAXT3V4T245** 4-bit configurable dual-supply transceiver addresses this need directly. With independent VCCA and VCCB supply rails each configurable from 0.9 V to 3.6 V, the device provides the voltage headroom to bridge any combination of modern low-voltage SoC I/O domains and the higher-voltage peripheral I/O environments common in automotive electronics. The block diagram in Figure 1 illustrates a representative ADAS domain controller architecture and highlights where the T30LAXT3V4T245 sits within the signal chain.

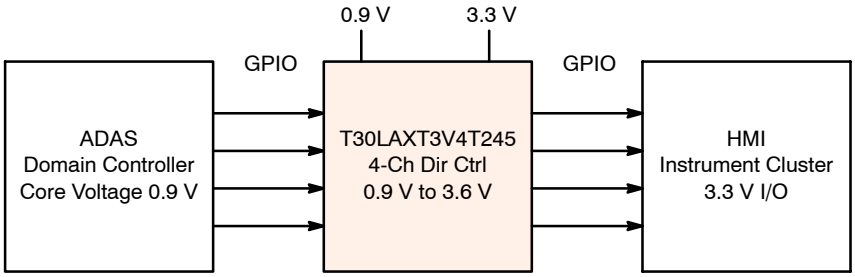

Figure 1. T30LAXT3V4T245 Voltage Level Translation in an ADAS Domain Controller

Voltage Level Translation in ADAS Systems

As CMOS process nodes continue to shrink toward 5 nm and below, processor core voltages and supported I/O levels fall in step. New-generation ADAS SoCs require I/O supplies from 0.9 V to as low as 0.7 V in future roadmap nodes. The I/O voltage mismatch between such processors and the broader peripheral ecosystem is therefore a systemic, not incidental, design challenge.

The T30LAXT3V4T245 is organized as two independent groups of 2-bit transceivers, each controlled by dedicated direction (1DIR/2DIR) and output-enable (1OE/2OE) pins. When nDIR is high, data flows from the A-port (SoC side, VCCA) to the B-port (peripheral side, VCCB); when nDIR is low, the direction reverses. The independent enable per group supports half-duplex bus protocols such as SPI and UART where transmit and receive must be gated separately. Both supply rails track independently, eliminating the need for power-sequencing constraints found in single-rail translators. The device also features partial power-off protection and 3-state behavior when either supply drops to ground, preventing back-drive or inadvertent logic assertion during power cycling – a critical requirement for ISO 26262 functional safety alignment.

Key Benefits for ADAS System Designers

The T30LAXT3V4T245 delivers several properties that are particularly valuable for ADAS domain controller designs.

- Wide dual-supply range (0.9 V–3.6 V on both VCCA and VCCB) accommodates current and next-generation

ADAS processor I/O levels without a device change, protecting the design against future node migrations.

- High-speed operation at up to 400 Mbps (≥1.8 V–3.3 V translation) and 200 Mbps (≥1.1 V translation) supports SPI sensor configuration buses, UART diagnostic links, and GPIO based control interfaces at automotive data rates.
- Balanced ±24 mA output drive at 3.0 V provides robust drive strength for 3.3 V peripheral buses with moderate capacitive loads, maintaining clean signal edges in the presence of PCB trace parasitics.
- Non-preferential VCC sequencing removes the requirement for power-supply sequencing logic between VCCA and VCCB, simplifying the power management architecture in multi-domain ADAS controllers.
- Partial power-off protection and 3-state outputs under power-down conditions prevent inadvertent signal injection onto live bus rails-an important attribute in systems that apply staggered supply sequencing for ISO 26262 diagnostic coverage.
- Compact UQFN16 package (1.8 mm × 2.6 mm) minimizes PCB footprint near the SoC, consistent with the space constraints of high-density ADAS domain controller PCBs.

Interface Mapping for ADAS Domain Controllers

Table 1 lists representative ADAS interfaces that benefit from the T30LAXT3V4T245, along with the voltage domains and achievable data rates from the device data sheet[1]. NOTE: VCCB tolerance at 5 V applies when the B-port supply is clamped below 3.6 V; for 5 V peripheral devices, an open-drain pull-up arrangement or a suitable higher-VCCB translator should be evaluated.

Table 1. T30LAXT3V4T245 ADAS INTERFACE VOLTAGE TRANSLATION SUMMARY

ADAS Interface	VCCA (SoC Side)	VCCB (Peripheral Side)	Max Data Rate	Bidirectional
SPI (Sensor config bus)	0.9 V – 1.2 V	3.3 V	400 Mbps	Yes
UART (Safety MCU diag.)	1.2 V – 1.8 V	3.3 V	200 Mbps	Yes
GPIO (Interrupt / Alert)	0.9 V – 1.8 V	3.3 V	400 Mbps	Yes

Design Recommendation

For ADAS domain controller designs that must bridge a low-voltage SoC I/O bus (0.9 V to 1.8 V) to 3.3 V peripherals across bidirectional interfaces including SPI, UART, and GPIO, the T30LAXT3V4T245 is the recommended **onsemi** solution. Its independent dual-group direction control makes it compatible with both full-duplex and half-duplex protocols. For unidirectional signal paths (e.g., clock-only outputs or sensor interrupt lines), the **T30LAXT3V4T244** 4-bit A-to-B-only level translator provides a lower-complexity option in the same CMOS process family.

For more information on **onsemi**'s level translation portfolio and automotive-qualified solutions, visit onsemi.com. The T30LMXT3V4T245 product page and data sheet are available at onsemi.com/T30LMXT3V4T245.

1. **onsemi**, T30LMXT3V4T245 Data sheet, Rev. 1, March 2026, https://www.onsemi.com/products/logic/voltage−level−translators/t30lmxt3v4t245

REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	9/11/2026

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