

NCV78902 in SEPIC Configuration

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Introduction

NCV78902 is a versatile device that, in addition to supporting a conventional boost topology, also enables operation in a SEPIC configuration.

A boost topology can generate only output voltages higher than the input battery voltage. Given the significant voltage fluctuations in automotive systems caused by events such as load dumps and engine cranking, the guaranteed minimum output voltage is typically above 20 V. However, certain applications, such as pre-regulation for linear LED drivers

used in rear lighting or cranking pulse filtering, may require a lower, well-regulated voltage. This need becomes even more pronounced in 48 V battery architectures. Achieving such output levels necessitates a change in topology.

A SEPIC topology provides the required flexibility, as it can maintain a stable output voltage either above or below the battery voltage.

With appropriate design considerations, summarized in this application note, the NCV78902 can be configured to operate as a two-phase SEPIC controller.

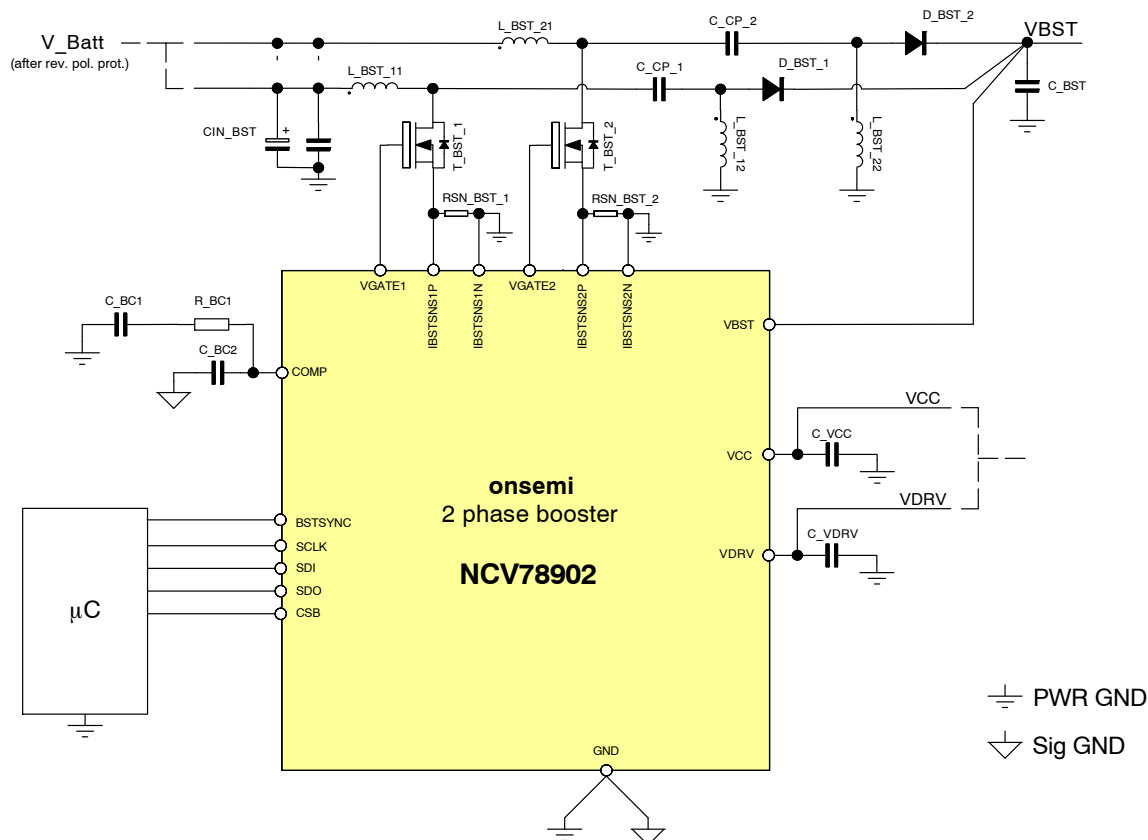


Figure 1. Typical Application Schematic – SEPIC Configuration

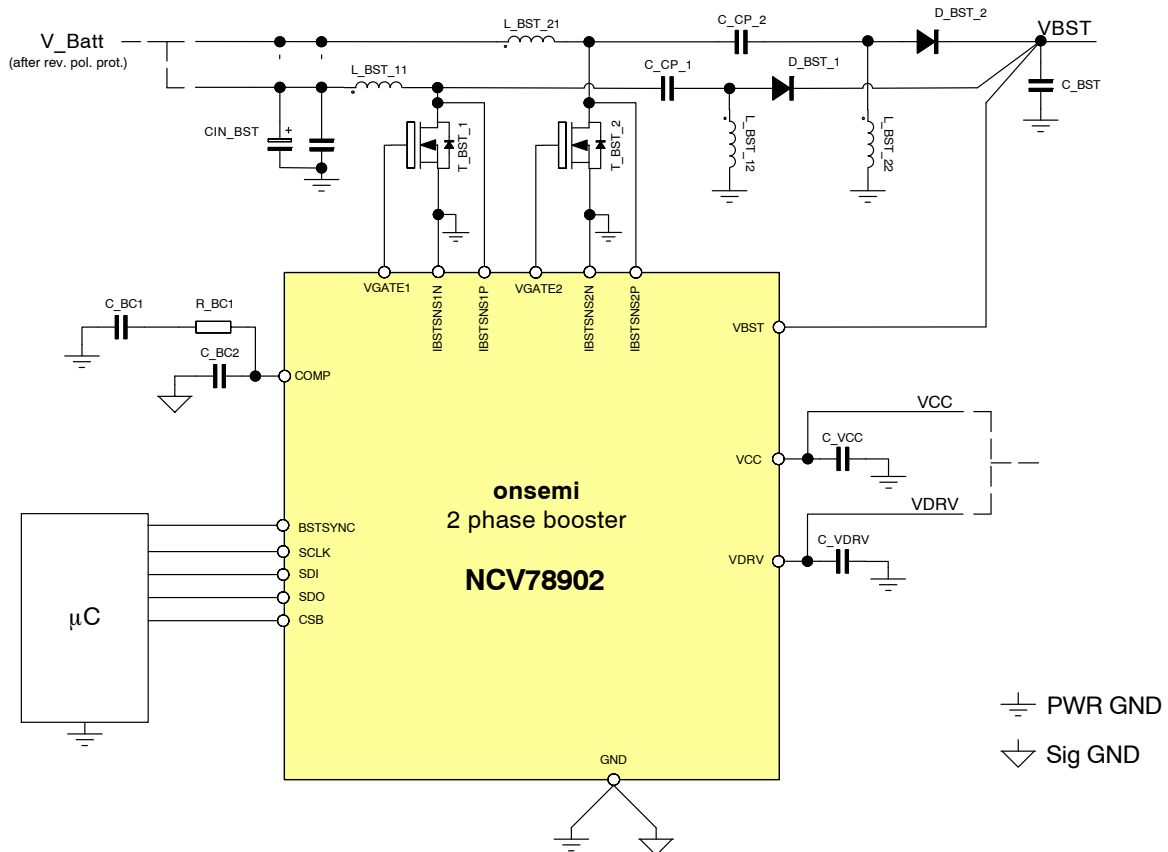


Figure 2. Typical Application Schematic – Shunt-less SEPIC Configuration

Boost-SEPIC Topology Differences

Boost topology inherently begins operation from the battery voltage, as its output cannot fall below the input level.

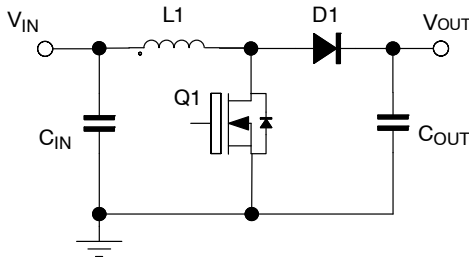


Figure 3. Booster Topology

SEPIC topology enables the true disconnection of the output, which means the converter starts from 0 V at power-up.

Unlike Booster topology, SEPIC consists of two power inductors. They can be implemented as two independent separate components, or it can be one component with two inductor windings coupled on one magnetic core.

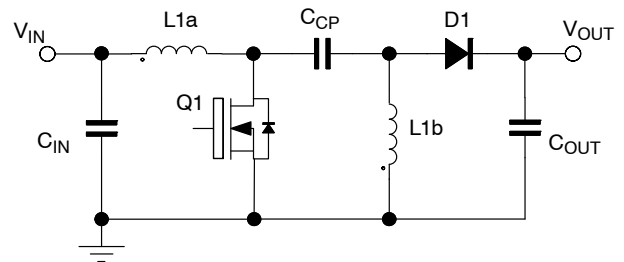


Figure 4. SEPIC Topology

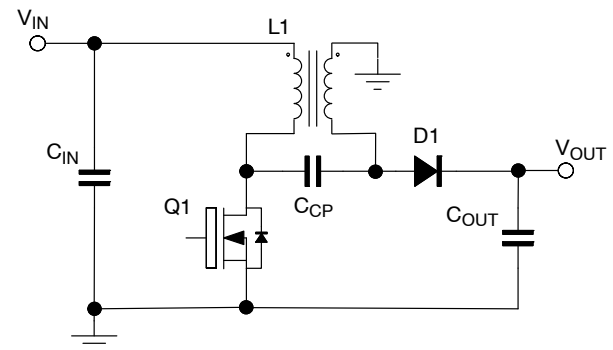


Figure 5. SEPIC Topology with Coupled Inductor

SEPIC Components Consideration

Inductor

The inductor value in a SEPIC converter should be selected based on the required current ripple under worst-case conditions, typically minimum input voltage, maximum output power, and the chosen switching frequency. A ripple current of 20–30% of the average inductor current is generally recommended to balance efficiency, transient response, and EMI performance.

The same selection methodology applies to both 12 V and 48 V automotive systems. However, because a 48 V system operates at lower input current for the same output power, a larger inductance is often required to maintain the same relative ripple current. When selecting the inductor, sufficient saturation current margin should be ensured for startup, fault, and transient conditions.

SEPIC power inductors can be implemented as two independent separate components, or it can be one component with two inductor windings coupled on one magnetic core. This solution results in a lower price, increased efficiency and reduced PCB area, and lower inductance is required for the same output current ripple.

On the LED Driver Evaluation Kit Daughter Board NCV78902R2DAGEVB (which can serve as a reference design) coupled inductor Würth Elektronik 74485540101 WE-CFWI with parameters 10 µH; 13 A; 13.9 mΩ is used.

Coupling Capacitor

The voltage rating of the SEPIC Coupling Capacitor must be greater than the maximum input voltage.

Its capacitance must be sufficient to keep input voltage ripple at lowest battery voltage at required limits:

$$C_{CP} \geq \frac{I_{OUT} \cdot D_{MAX}}{\Delta V_{C_{CP}} \cdot f_{SW}} \quad (\text{eq. 1})$$

Where

- C_{CP} is the coupling capacitor value,
- ΔV_{CCP} the practical guideline is to select 5% or 10% of the maximum input voltage $V_{IN(max)}$,
- I_{OUT} is the output current,
- D_{MAX} is the maximum duty cycle,
- f_{SW} is the SEPIC pwm clock frequency.

It is recommended to use a ceramic capacitor to keep the ESR losses as small as possible. On the LED Driver Evaluation Kit Daughter Board NCV78902R2DAGEVB (which can serve as a reference design) capacitor with parameters 10 µF; 100 V; X7S; 10% is used.

Output Capacitor

When MOSFET Q1 is conducting, the current through the output capacitor equals I_{OUT} since the capacitor is the only

element providing current to the output. When MOSFET Q1 is off the current through the C_{OUT} is the sum of the inductors L1a and L1b current minus the load current.

Assuming a linear relationship between the two sources of ripple we arrive that the output capacitor can be calculated as:

$$C_{OUT} \geq \frac{I_{OUT} \cdot D_{MAX}}{\Delta V_{C_{OUT}} \cdot f_{SW}} \quad (\text{eq. 2})$$

Where

- C_{OUT} is the output capacitor value,
- $\Delta V_{C_{OUT}}$ is the ripple across the output capacitor,
- I_{OUT} is the output current,
- D_{MAX} is the maximum duty cycle,
- f_{SW} is the SEPIC pwm clock frequency.

It is recommended to use a ceramic capacitor to keep the losses small.

Input Capacitor

The input capacitor sees moderately low RMS current thanks to the input inductor. The RMS current in the input capacitor is given by:

$$I_{CIN,RMS} = \frac{\Delta I_L}{\sqrt{12}} \quad (\text{eq. 3})$$

MOSFET

On SEPIC converter, the rated MOSFET drain voltage must be higher than:

$$V_{Q1,DS} \geq V_{IN(max)} + V_D + V_{OUT} \quad (\text{eq. 4})$$

Where

- $V_{IN(max)}$ is V_{CCP} – voltage over coupling capacitor corresponding to maximum input voltage,
- V_D is the voltage drop on diode,
- V_{OUT} is the output voltage.

Simplified less accurate equation for a quick calculation of MOSFET RMS current:

$$I_{Q1,RMS} = \frac{I_{IN}}{\sqrt{D_{MAX}}} \quad (\text{eq. 5})$$

Or in terms of the input and output voltages:

$$V_{Q1,RMS} = I_{OUT} \cdot \sqrt{\frac{(V_{IN(min)} + V_{OUT} + V_D) \cdot (V_{OUT} + V_D)}{V_{IN(min)}^2}} \quad (\text{eq. 6})$$

Diode

On SEPIC converter, the selected diode must be able to withstand reverse voltages equal to:

$$V_R \geq V_{IN} + V_{OUT} \quad (\text{eq. 7})$$

The average current that the diode must be able to withstand:

$$I_D = I_{IN} + I_{OUT} = \frac{I_{OUT}}{1 - D} \quad (\text{eq. 8})$$

And the peak current through the diode is equal to the peak current of MOSFET Q1 so the diode must be able to handle:

$$I_{D(\text{peak})} = I_{Q1, \text{peak}} = I_{L1a, \text{peak}} + I_{L1b, \text{peak}} \quad (\text{eq. 9})$$

NCV78902 in SEPIC Mode Considerations

NCV78902 incorporates built-in protection for output feedback failure. If the voltage at the booster feedback pin (VBST) drops below the BST_FBFAIL threshold (see Table 1), the device interprets this as a loss of feedback and the booster stage is disabled. The condition is reported through the BST_FBFAIL status flag (reg. 0x36).

Table 1. BOOSTER FEEDBACK FAIL DETECTION THRESHOLD

Symbol	Min	Typ	Max	Unit
BST_FBFAIL	1.15	1.21	1.27	V

Implementation and Masking of Booster Feedback Protection

To enable the use of SEPIC topology, the booster feedback protection BST_FBFAIL can be disabled through the BST_FBFAIL_MASK[2:0] register for a defined number of periods after startup, as specified in the following table:

Table 2. BOOSTER FEEDBACK FAILURE MASKING

BST_FBFAIL_MASK [2:0]	Mask Time – Periods {-}
0	Never
1	4
2	16
3	64
4	256
5	1024
6	4096
7	Always

During the masking time interval, the voltage at the output must rise above the BST_FBFAIL threshold (typ. 1.21 V). Several factors influence how quickly the output capacitor charges — and therefore how fast the output voltage increases:

- Input current limitation
- Output capacitor value
- Load conditions

If the masking time interval is set too short, the converter would fail to start because the output voltage will not reach 1.21 V in time. Conversely, an excessively long masking

period could, in principle, expose the system to risk (if feedback is lost and masked protection does not prevent uncontrolled rise of output voltage).

During the masking time interval, a modulo 4 division is applied to the clock signal, limiting the effective duty cycle to 25%. This constrains the maximum achievable output voltage in the event of an open feedback loop.

When the masking period ends, the BST_FBFAIL comparator is re-enabled. If its output remains active (the voltage at output is still below 1.21 V), the converter is stopped and the corresponding error flag is asserted. If the BST_FBFAIL comparator output is inactive, the converter starts normal operation.

Example of Feedback Failure Masking Settings

The time required to charge VBST pin above Feedback Fail Detection Threshold BST_FBFAIL is determined by the equation:

$$t_{\text{BST}} = \frac{C_{\text{OUT}} \cdot \Delta V_{\text{BST_FBFAIL}}}{I} \quad (\text{eq. 10})$$

Where

- t_{BST} is the time required to charge output capacitance above BST_FBFAIL threshold,
- C_{OUT} is the total capacitance at SEPIC output,
- $\Delta V_{\text{BST_FBFAIL}}$ is the BST_FBFAIL detection (typ. threshold 1.21 V),
- I is the current charging the output capacitance. For simplification, the half of the set current limitation $\text{BSTx_VLIM_THR}[7:0]/R_{\text{SENSE}}$ can be considered. Real current should be measured in application to get precise calculations. If the load becomes active immediately after start-up, its current consumption must also be taken into account and subtracted from the available charging current.

The BST_FBFAIL masking time is determined by:

$$t_{\text{MASK}} = \frac{\text{BST_FBFAIL_MASK}[2:0]}{f_{\text{sw}}} \quad (\text{eq. 11})$$

Where

- t_{MASK} is the booster feedback protection masking time,
- $\text{BST_FBFAIL_MASK}[2:0]$ is the number of masked periods,
- f_{sw} is the SEPIC pwm clock frequency.

The masking time must be set with sufficient margin to allow reliable start of SEPIC converter:

$$t_{\text{MASK}} > t_{\text{BST}} \quad (\text{eq. 12})$$

For NCV78902R2DAGEVB LED Driver Evaluation Kit Daughter Board settings BST_FBFAIL_MASK[2:0] = 2 or higher (meaning masking of 16 or more periods) should be selected to allow reliable start and grant proper functionality.

NCV78902 SEPIC Mode Limitations – Output Voltage Settings

The converter's output voltage is configured by means of BST_VSETPOINT[6:0] SPI register, which supports output voltages settings from 9.7 to 62 V as indicated in Table 3. Voltages lower than 9.7 V cannot be set.

Table 3. BOOSTER CONTROLLER – VOLTAGE REGULATION PARAMETERS

Characteristic	Symbol	Conditions	Min	Typ	Max	Unit
Booster Regulation Level	BST_REG_127			62		V
Booster Regulation Level	BST_REG_000			9.7		V
Booster Regulation Level Increase per Code	ΔBST_REG	Linear increase, 7 bits		0.412		V
Booster Regulation Level Error	BST_REGERRH	VBST_NOM > 25 V	–3		3	%
Booster Regulation Level Error	BST_REGERRL	VBST_NOM < 25 V	–4		4	%

Conclusion

The NCV78902 can be successfully configured to operate in a two-phase SEPIC topology by utilizing the BST_FBFAIL masking feature during startup.

SEPIC topology enables the converter to regulate output voltages independently of battery voltage variations, providing a robust solution for applications that require a stable output voltage both above and below the input supply.

This approach is particularly suitable for applications such as pre-regulators for linear LED drivers, rear-lighting systems, cranking pulse filtering, and other automotive power-conditioning functions where immunity to battery voltage fluctuations is required.



REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	10/15/2026



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