

Powering Next-Generation Image Sensors in AR Glasses and Smartphones

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INTRODUCTION

The continued evolution of computational photography, machine vision and augmented reality is placing increasingly demanding requirements on image-sensor power delivery. Modern imaging platforms combine higher sensor resolution, faster frame rates, complex on-sensor processing and high-speed data interfaces, while simultaneously targeting longer battery life and smaller form factors.

These requirements are particularly challenging in smartphones and AR glasses. Both platforms operate from a limited battery-energy budget and provide very little PCB area for power-management components. AR glasses introduce an additional thermal constraint because power dissipation must be minimized in a lightweight product located close to the user.

Image sensors also differ significantly from conventional static loads. Internal activity changes throughout exposure, pixel readout, image processing and data transmission. Consequently, sensor current consumption consists of repetitive transitions and bursts rather than constant DC current. The associated supply-current changes can occur much faster than the overall frame period and can produce significant voltage disturbances across the output impedance of the power-distribution network.

At the same time, system designers are reducing the voltage difference between upstream converters and sensor supply rails to maximize efficiency. This leaves an LDO with minimal operating headroom precisely when fast dynamic regulation is required. A suitable image-sensor power solution must therefore combine low dropout, fast transient response, low noise, high power-supply rejection and compact implementation.

This application note describes a practical power architecture based on the T30LMPSR131 and T30LMPSR165. The T30LMPSR131 is used for the low-voltage, high-current digital core domain, while the T30LMPSR165 addresses analog and auxiliary sensor rails requiring a compact, low-noise and fast-settling solution.

Image-Sensor Power Architecture

A modern CMOS image sensor typically uses several independent supply domains. Separating the domains allows the power architecture to address the electrical requirements of each internal function and reduces unwanted interaction between high-activity digital circuitry and noise-sensitive analog blocks.

Figure 1 shows a simplified power tree suitable for an image sensor used in an AR-glasses or smartphone platform.

Typical Image Sensor Power Tree

Reference architecture for AR glasses and smartphone imaging platforms

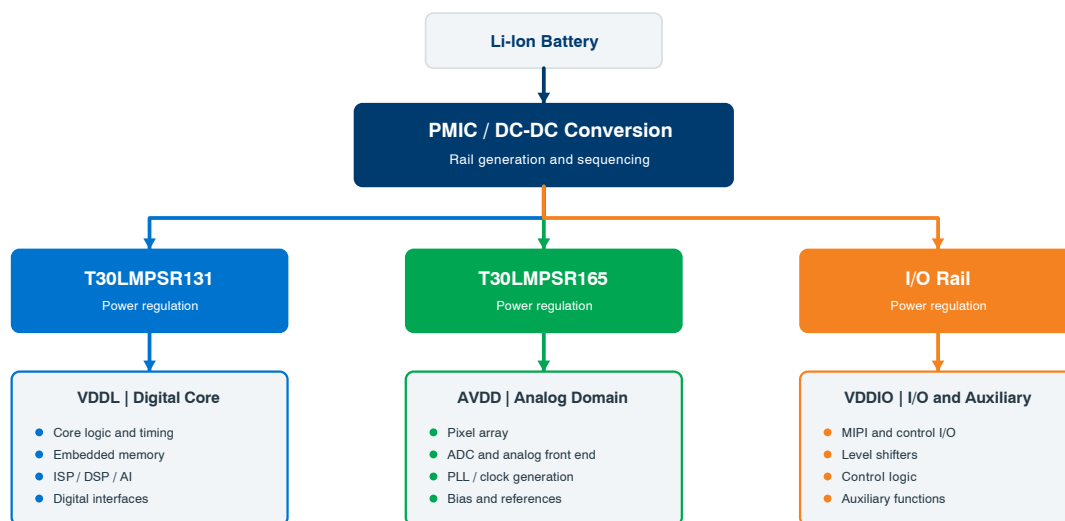


Figure 1. Simplified Image-Sensor Power Tree with Separate Digital, Analog and I/O Domains

The system battery supplies a main power-management IC containing DC-DC converters, sequencing logic and system-level control. The DC-DC converters efficiently generate intermediate supply rails, while downstream LDOs provide the final regulation required by the image sensor.

The digital core supply, identified as VDDL in Figure 1, powers the sensor core logic, embedded memory, image-signal processing functions and high-speed digital circuitry. This domain normally has the lowest output voltage and can exhibit the largest and fastest changes in load current. The T30LMPSR131 is positioned as the point-of-load regulator for this rail because it combines 1 A output capability, very low dropout and fast transient response. Its separate bias supply and NMOS pass architecture enable regulation of low-voltage rails while maintaining a small voltage difference between input and output. The device supports output voltages down to 0.5 V and is intended for space-constrained image-sensor and portable applications.

The analog supply, shown as AVDD, powers functions such as the pixel array, analog front end, ADC, PLL and internal reference circuits. Although this domain may require less current than the digital core, analog performance is more sensitive to supply ripple, broadband noise and transient disturbances. The T30LMPSR165 is

placed on this rail to provide a compact post-regulation stage with low dropout, fast settling, high PSRR and low output noise. The device supports output currents up to 300 mA and is designed to operate with a small effective output capacitance.

The VDDIO rail supplies MIPI interfaces, control interfaces, level shifters and auxiliary sensor functions. Depending on the sensor and PMIC architecture, the I/O rail may be supplied directly from the PMIC or through an additional discrete regulator. Figure 1 intentionally keeps this rail generic because its current, voltage and noise requirements depend strongly on the selected image sensor.

The architecture combines the conversion efficiency of switching regulators with the rail quality and dynamic regulation of point-of-load LDOs. The upstream DC-DC converter performs the major voltage conversion, while the final LDO isolates the sensor from upstream ripple and regulates the voltage locally, close to the load.

Understanding the Individual Supply Domains

The functional partitioning of a representative CMOS image sensor is shown in Figure 2. The diagram connects each sensor domain with the corresponding power-rail requirement.

Modern CMOS Image Sensor Supply Domains

Functional partitioning and electrical requirements of the main rails

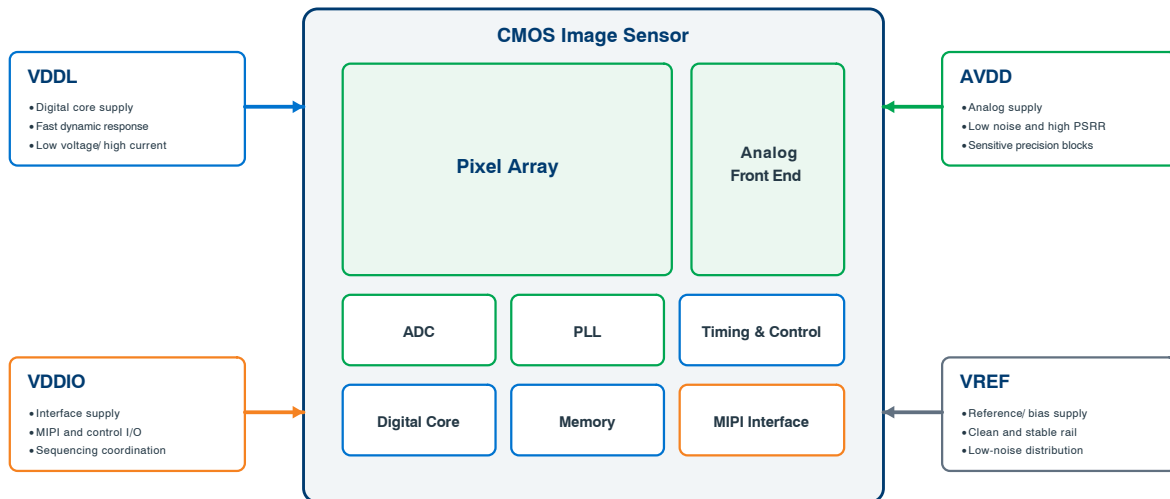


Figure 2. Functional Blocks and Supply Domains of a Representative CMOS Image Sensor

VDDL Digital Core Supply

The VDDL domain supplies digital logic, timing circuits, embedded memory and image-processing functions. Its average current depends on the sensor operating mode, resolution, frame rate and amount of on-chip processing. More importantly, the instantaneous current may change rapidly as individual processing blocks are activated and deactivated.

During a current increase, the local output capacitor initially supplies the additional load. The regulator control loop must then increase pass-device current and restore the output voltage. The magnitude of the resulting voltage deviation is determined by the effective output capacitance, capacitor parasitics, PCB interconnect impedance and the regulator's closed-loop output impedance.

As the core voltage decreases, the permitted voltage deviation generally becomes more critical because the same absolute disturbance represents a larger fraction of the nominal supply. Operation at low voltage also reduces the available margin between the normal operating range and the sensor's minimum acceptable supply voltage.

The T30LMPSR131 is therefore assigned to the VDDL rail. Its combination of high output-current capability, low output-voltage support and ultra-low dropout allows the upstream PMIC rail to be located close to the required sensor-core voltage. This reduces voltage loss across the LDO while preserving point-of-load regulation.

AVDD Analog Supply

The AVDD domain supplies the pixel array, sensitive analog signal path, ADC, PLL and related precision circuitry. Noise or ripple present on this rail can couple into the signal chain or modulate internal references and clock-related functions.

The analog rail therefore requires more than low DC error. The regulator must suppress disturbances generated by upstream DC-DC converters and must maintain a stable output during transitions between sensor operating states. Low output noise and high PSRR are particularly valuable when the LDO is used as a post-regulator after a switching converter.

The T30LMPSR165 provides this combination in a compact implementation. The device offers a typical dropout of 26 mV at 300 mA, a typical settling time of 0.8 μ s for a 0 to 300 mA load step, typical PSRR of 50 dB at 100 kHz, typical output noise of 16 μ VRMS and stable operation with 1 μ F effective output capacitance. Its small WLCSP package and limited external-component requirement are especially beneficial in compact camera modules and AR-glasses designs.

VDDIO and Auxiliary Supplies

The VDDIO domain supplies high-speed data and control interfaces, including MIPI and other sensor communication functions. The I/O rail may also supply level shifters or other auxiliary circuitry.

Although Figure 2 presents VDDIO as a separate rail, the implementation depends on the sensor. In some designs, VDDIO may be supplied directly by the PMIC. In others, additional filtering or point-of-load regulation may be required to prevent interface activity from coupling into the analog or digital core domains.

Power sequencing must also be considered. The sensor manufacturer's requirements define the permitted order and timing of VDDL, AVDD, VDDIO and reference supplies. The final regulator selection must therefore account not only for steady-state voltage and current, but also for enable thresholds, startup slew rate, active discharge behavior and interactions between individual rails.

VREF Reference Supply

Figure 2 also shows a separate VREF domain. Where the sensor provides a dedicated reference supply, this rail feeds internal voltage references and bias circuits that directly affect analog accuracy. Its current is typically low, but noise and ripple requirements can be as strict as, or stricter than, those of AVDD. Depending on the sensor, VREF may be derived from the AVDD regulator through additional filtering or supplied by a dedicated low-noise regulator. The sensor manufacturer's requirements determine the appropriate implementation.

Power-Delivery Challenges in AR Glasses

Figure 3 summarizes the main power-delivery constraints of an AR-glasses imaging subsystem and connects these constraints with the desired electrical outcomes.

Power Challenges in AR Glasses

Design constraints and corresponding power-delivery objectives

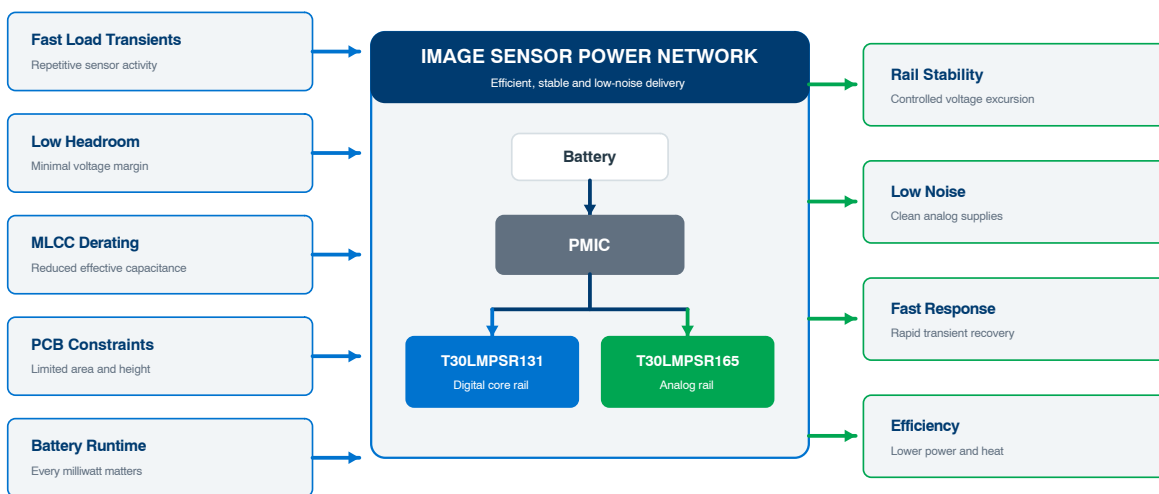


Figure 3. Key AR-Glasses Constraints and Corresponding System-Level Design Objectives

Fast and Repetitive Load Transients

Image sensors generate load profiles containing multiple operating phases. Current consumption may change during sensor initialization, exposure, pixel readout, analog-to-digital conversion, internal processing and MIPI data transmission.

Unlike a single load step commonly used for datasheet characterization, a real sensor profile may contain a sequence of pulses with different amplitudes, edge rates and durations. The regulator may not fully return to its previous steady-state condition before the next event occurs. Consequently, regulator performance should be evaluated using the actual repetitive load profile in addition to conventional load-step testing.

A regulator with inadequate transient response can produce excessive undershoot when sensor current increases and overshoot when the load is removed. Repetitive disturbances may also create a periodic ripple pattern correlated with frame activity.

Minimal Voltage Headroom

Reducing the voltage difference between the upstream converter and the LDO output improves power efficiency because less power is dissipated across the LDO:

$$P_{LDO} = (V_{IN} - V_{OUT}) \times I_{OUT} \quad (\text{eq. 1})$$

However, low-headroom operation moves the LDO closer to dropout. Conventional LDOs may exhibit increased output impedance, reduced PSRR and slower recovery as the available control margin across the pass device decreases.

This is particularly relevant to low-voltage digital core rails. An LDO may demonstrate good transient response with several hundred millivolts of headroom yet respond differently when the headroom is reduced to the level required by the final power architecture. Measurements should therefore reproduce the intended input voltage, output voltage and bias conditions.

Effective Capacitance and MLCC Derating

Output capacitance is another important part of transient performance. Small multilayer ceramic capacitors can lose a significant portion of nominal capacitance due to applied DC bias, temperature and component tolerance. The capacitance printed on the component is therefore not necessarily the capacitance available in the application.

The regulator should be evaluated using effective capacitance under actual operating conditions. This is particularly important for miniature capacitors used in smartphones, camera modules and AR glasses, where high-capacitance components are often selected in very small case sizes.

The T30LMPSR131 documentation defines the capacitance requirement in terms of effective capacitance and explicitly accounts for derating factors. The T30LMPSR165 is designed to remain stable with a

minimum effective output capacitance and recommends X5R or X7R ceramic capacitors.

PCB Area and Thermal Constraints

The mechanical design of AR glasses places strict limits on component area and profile. Power components must coexist with cameras, displays, processors, wireless connectivity, sensors and battery-management circuitry in a lightweight enclosure.

A smaller regulator package alone does not guarantee a smaller total solution. Required input and output capacitors, routing constraints and thermal considerations must also be included. An LDO that maintains dynamic performance with modest effective capacitance can reduce the area occupied by external components and make placement close to the sensor supply pins easier.

Power dissipation must also be minimized. Any loss in the LDO contributes to local heating, which is particularly undesirable in a compact wearable product. Ultra-low-dropout operation helps reduce this loss by allowing a smaller input-to-output voltage difference.

Desired Outcomes

The right side of Figure 3 identifies four primary outcomes:

- Stable supply rails during dynamic sensor activity
- Low noise for sensitive analog circuitry
- Fast recovery following load changes
- High efficiency with low power dissipation

These requirements are interdependent. Increasing upstream voltage headroom may improve regulation but reduce efficiency. Adding output capacitance may reduce transient deviation but increase board area. The preferred solution achieves the required rail stability through regulator performance rather than excessive voltage or capacitance margin.

Digital Core Regulation with the T30LMPSR131

The T30LMPSR131 is intended for low-voltage, high-current applications in which very low dropout and fast dynamic response are required simultaneously. The device uses an NMOS pass transistor and a separate bias supply, allowing the regulated input rail to operate close to the output voltage while the control circuitry is powered from a higher bias voltage.

This architecture is particularly suitable for the VDDL domain shown in Figures 1 and 2. The regulator can supply up to 1 A and supports fixed output voltages from 0.5 V to 1.8 V in 25 mV steps, with a typical dropout of 25 mV at 1 A. The device also provides typical output noise of 7.5 μ V_{RMS}, typical PSRR of 78 dB at 1 kHz and 40 dB at 100 kHz, and 1.2 V logic-level enable compatibility appropriate for modern portable platforms.

The principal system benefit is the ability to reduce the output voltage of the upstream converter while retaining a locally regulated sensor rail. This reduces power dissipated by the LDO and can improve overall battery efficiency. It also reduces the need to reserve excessive voltage margin solely to support transient performance.

Measurement with the Actual Sensor Load Profile

The value of the regulator should be demonstrated using the actual sensor current profile rather than only a synthetic rectangular load step.

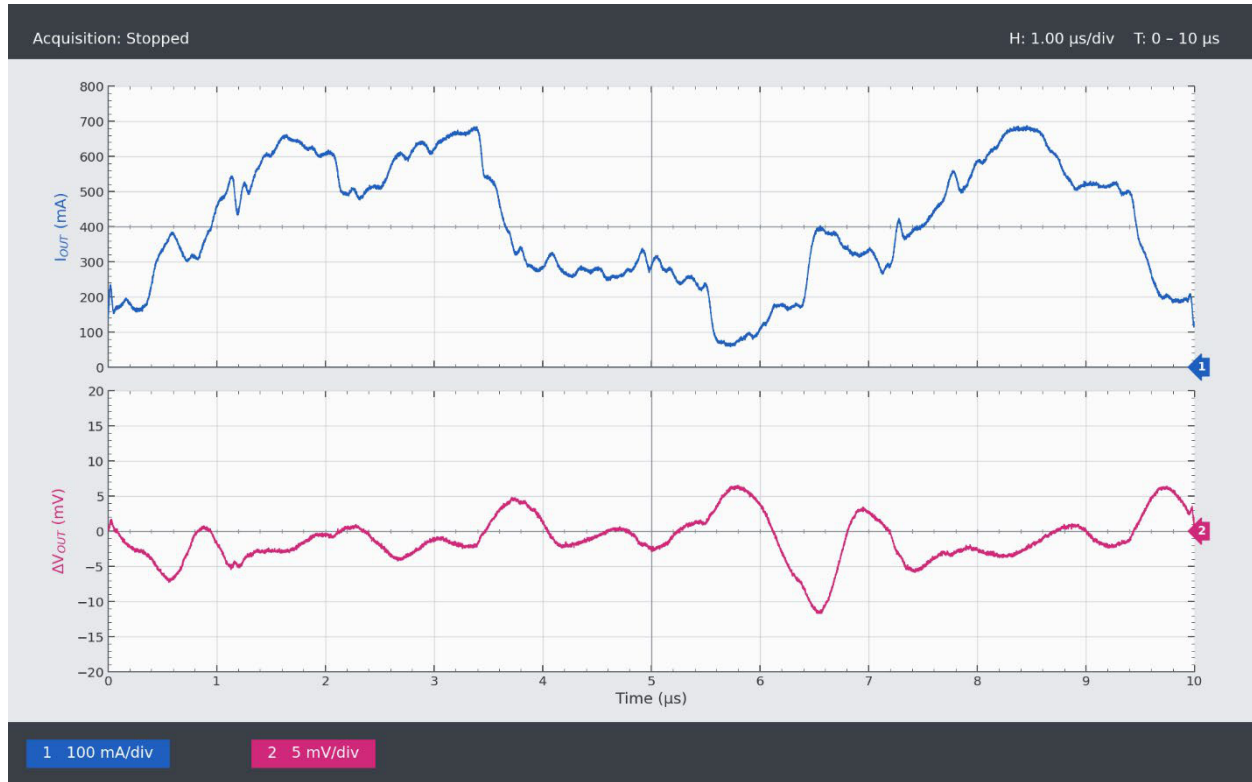


Figure 4. Measured T30LMPSR131 Response to a Representative Image-Sensor Digital-Core Load Profile

Figure 4 shows the T30LMPSR131 response to the measured sensor load profile. The waveform contains repetitive current transitions associated with normal sensor activity rather than a single synthetic load step. Under the stated low-headroom operating conditions, the output remains within the required voltage limits throughout the activity cycle. The measured peak undershoot is 12 mV, the peak overshoot is 6 mV.

Analog-Rail Regulation with the T30LMPSR165

The T30LMPSR165 addresses analog and auxiliary rails where output current is lower but solution size, noise, PSRR and transient settling remain important.

The device supports output currents up to 300 mA and is designed for very fast transient response: a 0 to 300 mA load step with 100 ns rise time produces a typical undershoot of

30 mV and settles within 0.8 μ s. The device operates with 1 μ F effective output capacitance and is available in a compact 0.64 mm $\times$ 0.64 mm WLCSP package. These properties make the device suitable for the AVDD domain shown in Figures 1 and 2.

High PSRR helps attenuate disturbances from the upstream switching converter. Low output noise supports sensitive sensor circuitry, while rapid transient recovery maintains the analog supply when the sensor changes operating state.

The small output-capacitance requirement is also important at the system level. It allows the LDO and its local bypass capacitor to be placed close to the image sensor, reducing interconnect impedance and limiting the area of the sensitive analog supply loop.

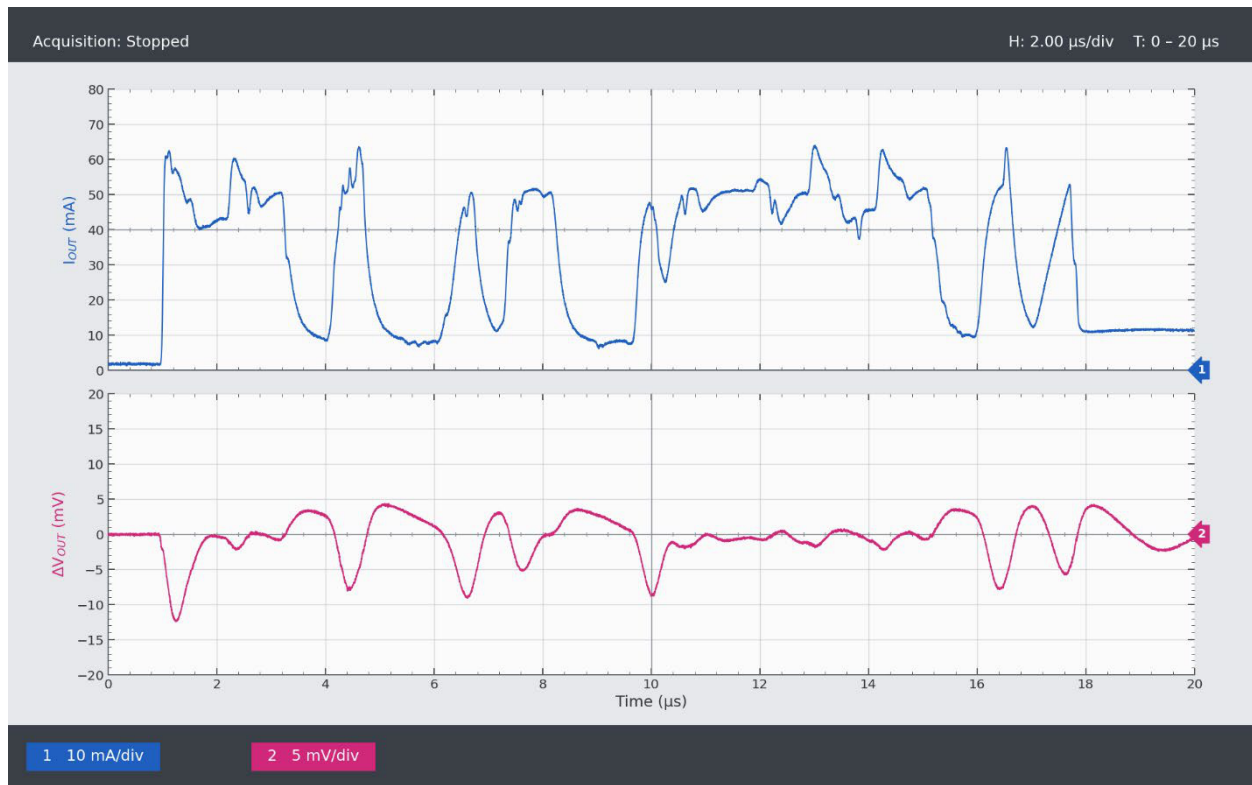


Figure 5. Measured T30LMPSR165 Response to a Representative Image-Sensor Digital-Rail Load Profile

Figure 5 shows the response of the T30LMPSR165 to the measured analog-rail current profile. The regulator maintains a controlled output-voltage deviation during repetitive sensor activity while operating with an effective output capacitance of 1 μ F. The measured peak undershoot is 12 mV and the peak overshoot is 4 mV. This tight

regulation range keeps the analog rail stable and helps preserve analog signal-chain integrity.

System-Level Benefits

Figure 6 summarizes how the regulator characteristics translate into benefits at the imaging-system level.

System-Level Benefits

Complementary LDO attributes for next-generation imaging systems

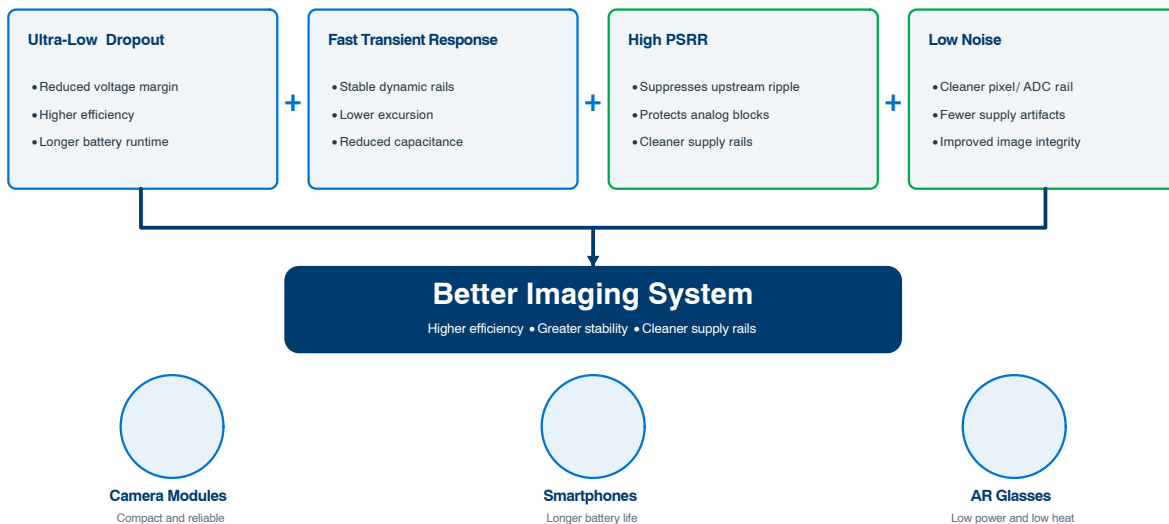


Figure 6. System-Level Value Created by Low Dropout, Fast Response, High PSRR and Low Noise

Ultra-low dropout allows the intermediate PMIC voltage to be reduced, limiting LDO power dissipation and improving battery utilization. Fast transient response maintains rail stability during rapid and repetitive sensor activity. High PSRR attenuates disturbances from upstream switching stages, while low output noise provides a clean supply for analog and pixel-related circuitry.

These characteristics should not be considered independently. Their combined effect determines whether the image sensor can operate from an efficient, compact and robust power tree.

For camera modules, the principal benefits are compact implementation and stable operation across multiple sensor modes. In smartphones, reduced voltage margin and power dissipation contribute to longer battery life and support increasingly complex computational-imaging workloads. In AR glasses, high efficiency and compact implementation help address the combined constraints of battery runtime, thermal performance, weight and available PCB area.

The T30LMPSR131 and T30LMPSR165 address complementary parts of the image-sensor power tree. The T30LMPSR131 provides the current capability and low-headroom regulation required by the digital core, while the T30LMPSR165 provides a small, low-noise and fast-settling solution for analog or auxiliary rails.

CONCLUSION

Modern image sensors present a demanding combination of rapid load changes, low operating voltages, strict noise requirements and limited implementation area. These challenges are intensified in battery-powered smartphones and AR glasses, where efficiency and thermal performance are critical system parameters.

A partitioned power architecture allows each image-sensor domain to be supplied according to its specific electrical requirements. The T30LMPSR131 supports low-voltage, high-current digital core rails through its 1 A capability, NMOS architecture, separate bias supply and ultra-low-dropout operation. The T30LMPSR165 complements this device on analog and auxiliary rails by combining fast transient response, high PSRR, low noise and operation with small effective output capacitance.

When combined with realistic load-profile testing, this architecture demonstrates how regulator selection affects more than an individual supply specification. Low dropout improves efficiency, fast response preserves voltage margin, high PSRR and low noise protect sensitive sensor circuitry, and compact implementation reduces total solution area.

Together, the T30LMPSR131 and T30LMPSR165 provide a practical foundation for efficient and robust image-sensor power delivery in next-generation smartphones, AR glasses and advanced camera systems.



REVISION HISTORY

Revision	Description of Changes	Date
0	Initial document release.	10/22/2026



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