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Latch-up Considerations for ESD Protection Devices on High Speed Serial Interface Applications

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APPLICATION NOTE

Introduction

As process geometries of chipsets that drive today's high speed serial interfaces become smaller and consequently more sensitive to transients such as ESD, the challenge to provide adequate protection for these chipsets is growing. A type of device that exhibits a negative resistance on a portion of their current−voltage characteristic is one solution to overcome the protection challenge. However, when using such a snap-back device, the effect of data line latch−up must be considered. This application note will discuss the effects of a latch−up condition and their applicability to snap-back protection devices. The note will also explain the relevant portions of certain high speed serial interfaces such as HDMI 1.4, USB 2.0, and USB 3.0 with respect to latch-up by analyzing potential latch−up conditions in each case. Based on the analysis, recommendations and design specifications for the protection device will be presented for each case in order to guarantee latch−up free applications. The below recommendations for each case will be discussed in relation to ON Semiconductor's ESD8000 series technology.

Latch−Up Effects

A latch−up condition may be initiated by a transient (such as ESD, conducted or radiated EMI, or surge) bringing the protection device into conduction. Latch−up is said to occur if the device remains in an on state, after the transient has passed. The latch−up state can be maintained in a snapback device if the power source on the protection can supply enough voltage and current to maintain the protection device's on state.

Latch−up conditions are not desirable because of two main reasons. One being that the conduction current may be excessive, thus causing damage to the protection device, the application circuit, or both from the resulting power dissipation. The other being that the voltage across the protection device in conduction may be too low to allow the application circuit node to reach its normally intended voltage.

Latch−Up Free Design: General Approach

Figure 1 shows the typical current−voltage characteristic of a snap−back protection device (such as a silicon controlled rectifier or SCR for example). The parameters of interest as shown on Figure 1 are: the breakdown voltage (V_{BR}), break−over voltage (V_{BO}), snap−back voltage (V_{SB}), and both the holding current (I_H) and holding voltage (V_H).

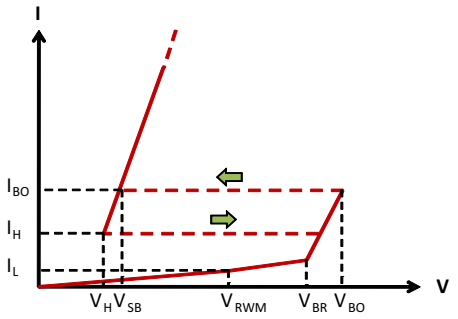

Figure 1. Typical Snap−back Protection Device Current−Voltage Characteristic

Several parameters of the protection device can be acted upon to prevent a latch−up condition. The protection device snap−back voltage (V_{SB}) can be designed to be higher than the maximum operating voltage, V_{SS} or V_{RWM}, of the application line. In this case, every point of the current−voltage characteristic is above the maximum operating voltage, for currents above the leakage level I_L. This is representative of standard Zener diode protection devices for example which do not exhibit snap−back characteristics. Another key parameter that can be designed to prevent a latch−up condition is the holding current, I_H. The holding current can be designed to be higher than the maximum steady−state current I_{SSMAX} the application circuit can supply. While these serve as guidelines that will guarantee latch−up free designs under all circumstances, they can be overly conservative. A load−line analysis of the application circuit can provide more refined guidelines, which will allow a better tuning of the protection device characteristics.

Latch−Up Free Design: Load−Line Approach

The load-line analysis of the application circuit assumes that its behavior is linear, and that the source can be

represented by a voltage source in series with a source resistor, connected to the protection device. Let the voltage be V_{DD} and the source resistance be R_S. Figure 2 shows a schematic representation of this model.

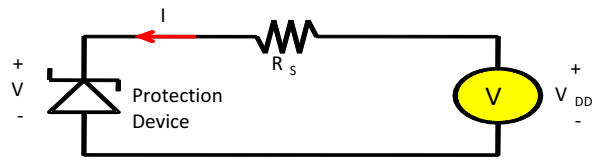

Figure 2. Schematic Representation of the Load−Line Analysis Circuit

The maximum voltage possible across the protection device assuming it is an open circuit is therefore V_{DD}. Alternatively, if the protection device is a short circuit, the maximum current is now $I_{SSMAX} = V_{DD}/R_S$. In the current−voltage plane, a line (the load−line) linking these two points A = (V = 0, I = I_{SSMAX}) and B = (V = V_{DD}, I = 0) can be drawn. Any point located on this load−line is a possible stable operating point of the application circuit. Figure 3 shows a graphical representation of this load−line. If the protection device's snapback I−V curve crosses the load line, latch−up is possible. If the protection device's I−V curve does not cross the load line, latch−up cannot occur.

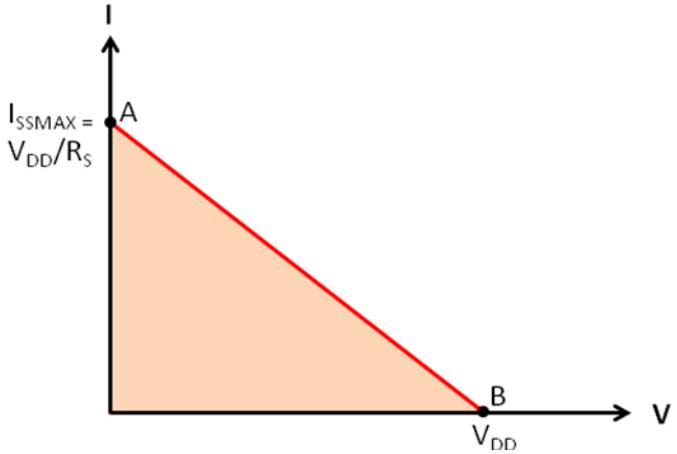

Figure 3. Graphical Representation of the Load−line

To determine the operating point(s) of the circuit including the protection device, the intersections of the load line and the current−voltage characteristic of the protection device must be determined. Figure 4 shows two possible cases.

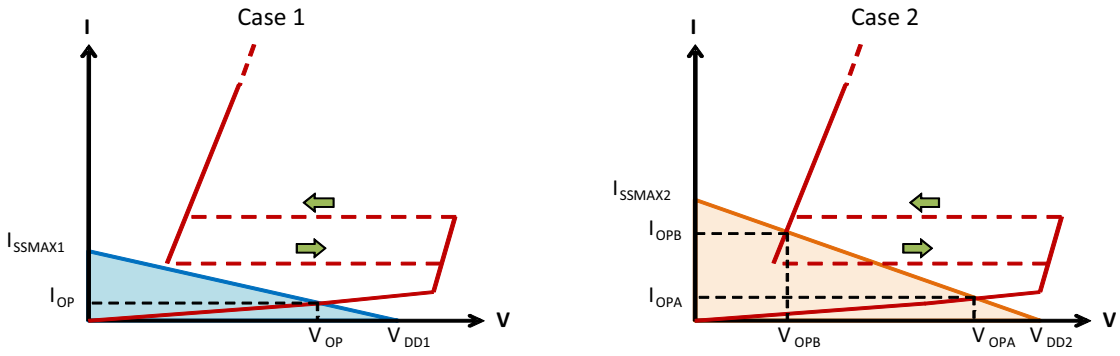

Figure 4. Graphical Solution of the Operating Point(s) for Two Load−line Cases

In case 1, the load−line intersects the current−voltage characteristic of the device in one unique point (V_{OP}, I_{OP}). This is the only stable operating point of the circuit and the system is therefore latch−up free. Note than I_{SSMAX1} is higher than I_H in this case. In case 2, the load−line intersects the current−voltage characteristic of the protection device in two points (V_{OPA}, I_{OPA}) and (V_{OPB}, I_{OPB}). Therefore in this case, the potential for latch−up exists if the system settles at (V_{OPB}, I_{OPB}) after a transient. In the following sections, this load−line analysis method will be used to determine snap−back protection device requirements to provide a latch−up free system for three applications: HDMI 1.4, USB 2.0, and USB 3.0 interfaces.

ESD8000 Series Technology

ON Semiconductor's 8000 series of ESD protection devices utilizes a deep snap−back, SCR type structure. By using this technology, the potential for a latch−up condition was taken into account and the below recommendations to design a latch−up free device were implemented. The main parts in the series that service the three main interfaces discussed above, shown in Table 1, were designed with parameters to guarantee latch−up free designs in USB 3.0/2.0 and HDMI 1.4/1.3 interfaces respectively. System level ESD testing was performed on all devices to verify that no latch−up conditions occurred.

Table 1. SUMMARY OF SCR PARAMETERS FOR ESD8000 SERIES DEVICES

ON Semiconductor's ESD8000 Series Devices	V_{BR} (Min) (V)	I_H (Min) (mA)	V_H (Min) (V)
ESD8004	5.50	20.00	1.00
ESD8006	5.50	20.00	1.00
ESD8008	5.50	20.00	1.00
ESD8040	5.50	–	–

HDMI 1.4 Application

HDMI 1.4 interface builds on the existing 1.3a specification by adding support for 3D video, higher resolutions, shared network connections between 1.4 compatible devices, etc… There has been no information that states a change in the data signal's electrical characteristics and it is assumed to be the same as HDMI 1.3a specification. The HDMI data−carrying lines use a Transient−Minimized Differential Signal (TMDS) signaling method. The HDMI 1.4 cable interface contains three TMDS data pairs with separate shields, one TMDS clock pair with shield, a 5 V power supply line, a GND line, and four additional (low speed) auxiliary signal lines. The focus of this analysis is the requirements for protecting the more challenging high speed data lines (TMDS lines), which are connected to a highly sensitive high speed transceiver chip requiring advanced ESD protection devices.

Figure 5 shows a conceptual schematic for one TMDS signal pair with schematic representations of the Transmitter and Receiver circuits. This figure is taken from the HDMI 1.3a specification.

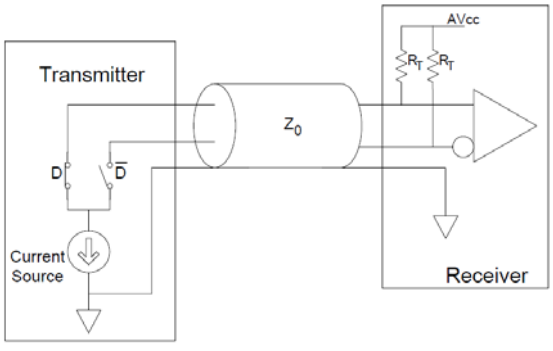

Figure 5. Schematic Representation of One TMDS Differential Data−line

In this schematic, a protection device would be inserted at the connector site on either or both sides of the transmission line Z_0. Given that the current source and signaling switches (D and D_ gates) sub−circuit is in parallel to the protection device, the worst case scenario is when the signaling switch is open and the full A_{Vcc} voltage is across the protection device. In this case, the current source and signal switch sub−circuit does not affect the loading of the A_{Vcc} source. The load−line characteristics are therefore, a voltage source of value A_{Vcc} and a source resistance of R_T. According to the 1.3a specification, values for A_{Vcc} and R_T are 3.3 V ±5% and 50 Ω ±10% respectively. For the purpose of the load−line analysis, the worst case scenario is when A_{Vcc} is at its maximum limit, 3.465 V, and R_T is at its minimum limit, 45Ω. This results in a load−line with V_{DD} = 3.465 V and I_{SSMAX} = 77 mA (3.465 V/45 Ω).

Assuming that the protection device is an idealized SCR, with a V_{BO} greater than V_{DD} and a V_H = 1 V for all currents, I > I_H (equivalent to an SCR dynamic resistance in the conduction region of zero). Using an idealized SCR presents the worst case scenario as a real SCR will typically have a V_H greater than 1 V and the dynamic resistance will be greater than zero. Figure 6 shows a graphical representation of the load−line analysis for the ideal SCR in the HDMI TMDS line protection case.

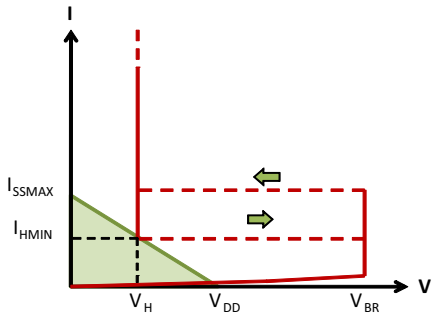

Figure 6. Graphical Representation of the Load−line Analysis in the HDMI Case with an Ideal SCR

As can be seen on the graph, the latch−up free condition is when I_H is above the intersection of the HDMI load−line and the vertical, V_H = 1 V line. This corresponds to a minimum value for I_H given by:

$$I_{HMIN} = \frac{V_{DD} - V_H}{V_{DD}} I_{SSMAX} \quad \text{(eq. 1)}$$

Given the values for V_{DD}, V_H, and I_{SSMAX} for HDMI, the resulting I_{HMIN} value is 54.78 mA. A protection SCR device with $V_{BR} > V_{DD}$, $I_H > I_{HMIN}$, and $V_H > 1$ V at I_H will satisfy the latch−up free condition for the HDMI TMDS line protection application.

USB 2.0 Application

The USB 2.0 interface uses a single differential pair to carry data encoded as a NRZI signal. In addition to the data pair, the USB 2.0 connection includes a 5 V power line and a GND line. The USB 2.0 specification includes the capability of transmission of data at three different speeds: High−Speed (HS) at 480 Mbps, Full−Speed (FS) at 12Mbps and Low−Speed (LS) at 1.5 Mbps. Therefore, the transceiver architecture includes various drivers and terminations to accommodate these various modes of operation, depending on the speed of the transmission being supported by the USB device connected. Figure 7 shows a schematic representation of the USB 2.0 transceiver circuit.

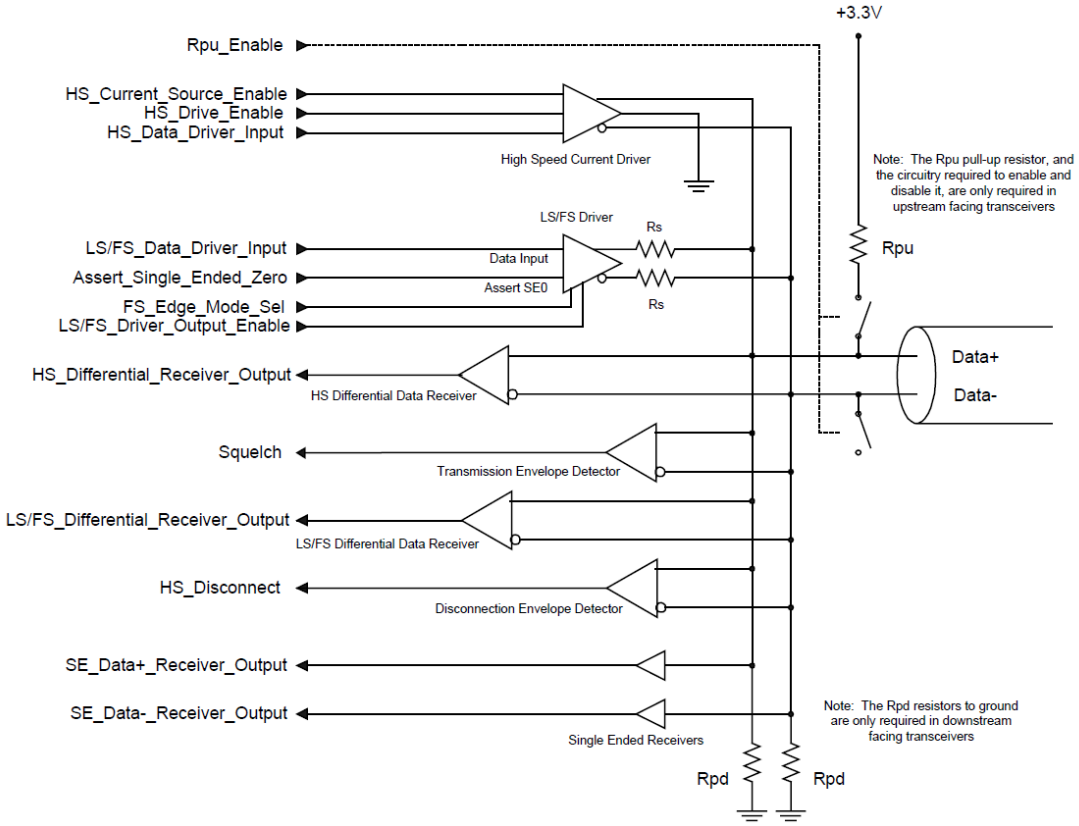

Figure 7. Schematic Representation of the USB 2.0 Transceiver Circuit

For the purpose of the load−line analysis, we can omit all the devices that have inputs connected to the data−lines since they are high−impedance elements. However, we must distinguish between LS/FS and HS operating modes due to the fact that they present distinctly different circuit configurations with different voltage and current levels.

LS/FS Mode Load−Line Analysis

In LS/FS mode, the HS current driver is disabled and acts as high impedance therefore it can be omitted from the schematic representation. The only difference in terms of signaling levels between LS and FS modes is whether the pull−up resistor, R_{pu}, is connected (LS) or disconnected (FS) to the D+ line. Therefore, the D+ line operating in LS mode is the worst case for determining the SCR parameters for protection. Table 2 gives the circuit element values, taken from the USB 2.0 specification, of interest in this evaluation for USB 2.0 in LS mode.

Table 2. USB 2.0 LS MODE TRANSCEIVER CIRCUIT ELEMENT VALUES

USB 2.0 Circuit Element	Min	Max	Worst Case
R_{pu}	1.425 kΩ	1.575 kΩ	1.425 kΩ
R_{pd}	14.250 kΩ	15.750 kΩ	15.750 kΩ
DC Termination Voltage for R_{pu}	3.0 V	3.6 V	3.6 V
R_S (HS mode)	40.500 Ω	49.500 Ω	–
R_S (LS mode)	28 Ω	44 Ω	28 Ω
Driver Source Voltage	2.8 V	3.6 V	3.6 V

In this configuration, the LS/FS driver sources a max voltage of 3.6 V with the output impedance of the driver being given in Table 1. For the purpose of the load−line analysis, we can replace the LS/FS driver with a 3.6 V voltage source connected to the D+ line via a 28 Ω resistor. Figure 8 shows the equivalent schematic of the LS circuit connected to the D+ line and its simplified equivalent source for the load−line analysis.

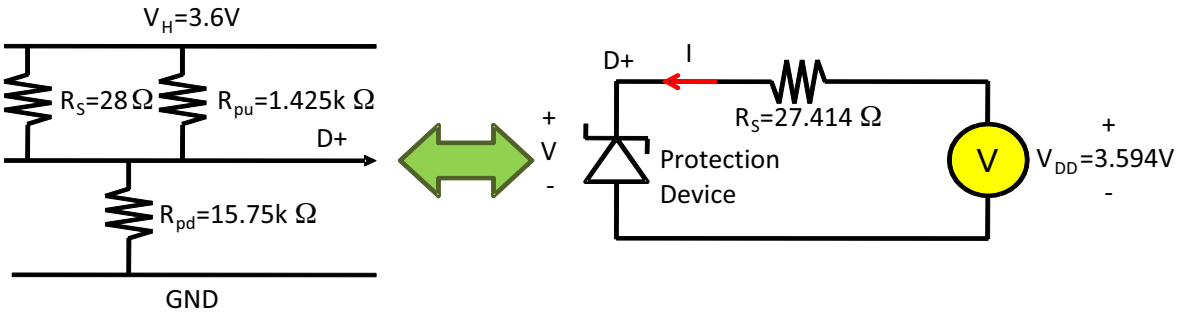

Figure 8. Equivalent Schematic and Load−line Source for USB 2.0 LS Mode Transceiver

From this analysis, it follows that the load−line representation of the USB 2.0 LS/FS driver in the current−voltage plane is a line between points (I_{SSMAX} = 131.1 mA, V = 0) and (I = 0, V_{DD} = 3 V). Equation 1, given earlier, defines the minimum holding current for the ideal SCR. Given the numbers for the USB 2.0 LS/FS driver in LS mode, the corresponding I_{HMIN} value in this case is 94.6 mA. A protection SCR device with V_{BR} > 3.594 V, I_H > 94.6 mA and V_H > 1 V at I_H will satisfy the latch−up free condition for the USB 2.0 LS−mode line protection application.

HS Mode Load−Line Analysis

In HS mode, the LS/FS driver asserts zero volts on both outputs and the output impedances, Rs, on each output act as termination for the signal lines. The HS driver is operated as a current source which is switched between channels D+ and D− to generate the differential signals. Both D+ and D− lines are equivalent when the USB 2.0 transceiver is operated in HS mode. Pull down resistors, R_{pd}, are also present on each line. This full circuit is present on each end of the USB cable. Per the USB 2.0 specification, the current source in the HS driver has a nominal value of 17.78 mA ±10%. The left side of Figure 9 shows the equivalent schematic for the HS circuit during a high state with the maximum forced current of 19.558 mA. This current must be shared by the four parallel resistors and the protection device. The four parallel resistors can of course be represented by a single 24.67 Ω resistor, R. The total current, I_S, is the sum of the current between resistors and the protection device current, I_P, where V is the voltage across the resistors and protection device.

$$I_S = \frac{V}{R} + Ip \qquad \text{(eq. 2)}$$

Or

$$I_p = I_S - \frac{V}{R} \qquad \text{(eq. 3)}$$

This equation shows the HS circuit with a protection element to have an effective load line as shown in Figure 10. Alternatively the constant current and resistor combination can be viewed as a voltage source with source impedance equal to resistor R as shown on the right side of Figure 9.

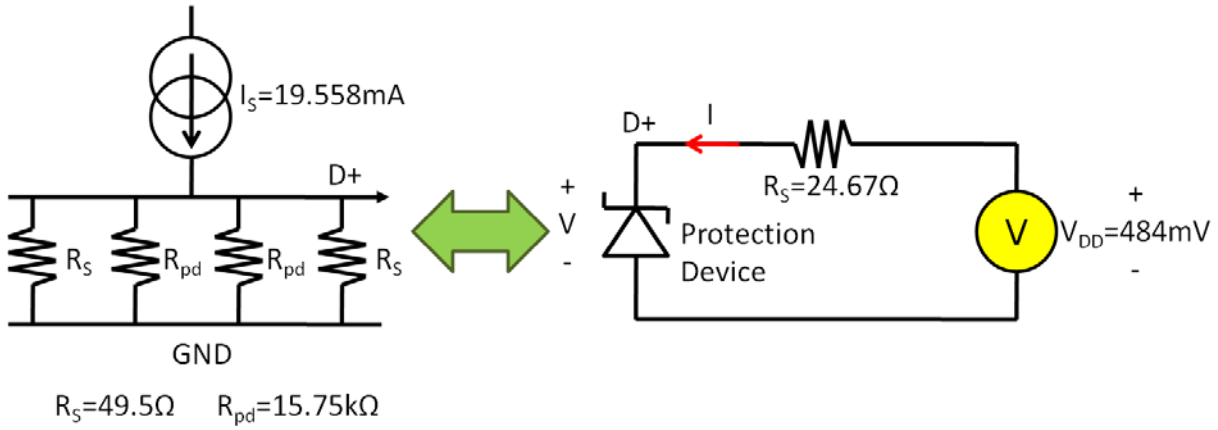

Figure 9. Equivalent Schematic and Load−line Source for USB 2.0 HS Mode Transceiver

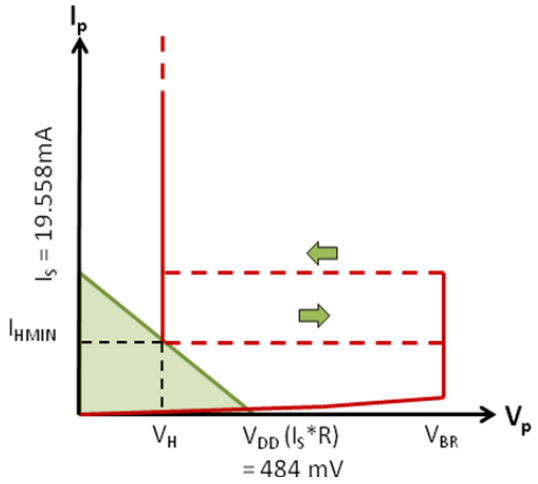

Figure 10. Equivalent Load Line for HS USB 2.0

USB 3.0 Application

The USB 3.0 interface uses three differential pairs to carry data, a 5 V power line, and a GND line. The first differential pair adheres to the USB 2.0 specification for which its latch−up considerations have been addressed in the previous section. The other two differential pairs are called SuperSpeed (SS) data links and are described in the USB 3.0 specification. Each pair is capable of data transmission at a 5 Gbps rate with one pair dedicated to a transmit link, SSTX, and the second pair dedicated to a receive link, SSRX. Figure 11 shows a diagram of the SS connection between two USB 3.0 devices.

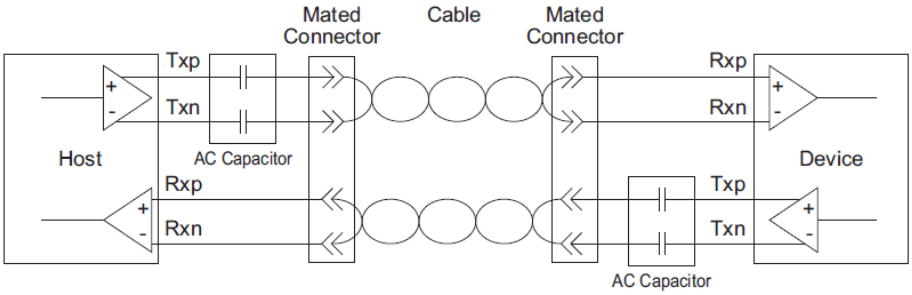

Figure 11. Diagram of the SS Connection Between Two USB 3.0 Devices

Figure 12 shows a sample waveform of a typical differential signal on a SS pair. The differential voltage is denoted as V_{DIFF} = Txp − Txn and the common mode voltage is denoted as V_{CM} = (Txp + Txn)/2.

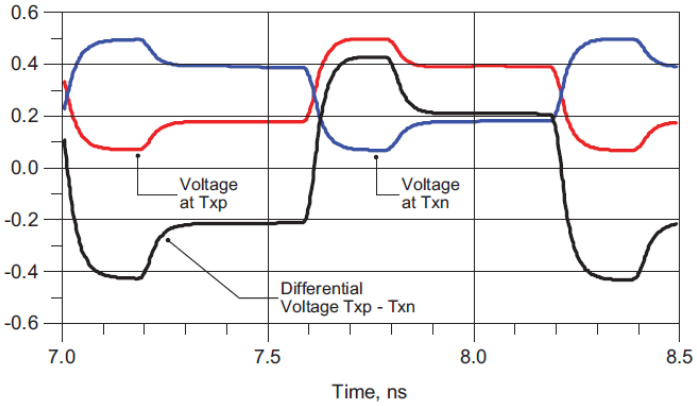

Figure 12. Sample Waveforms on a USB 3.0 SS Pair

Note that as shown on Figure 10, the data−lines are AC−coupled via coupling capacitors, and that the common−mode voltage is different on either side of the capacitors.

In order to evaluate the potential for latch−up in the USB 3.0 SS application, three cases must be examined:

1. The protection device is located between the transmitter and the AC coupling capacitor.
2. The protection device is located between the AC coupling capacitor and the connector.
3. The protection device is located between the connector and the receiver.

Case 1 shall be evaluated first. The voltage at the transmitter is composed of V_{DIFF} + V_{CM} and the USB 3.0 specification only calls for a normative value for V_{DIFF}. Informative specifications for V_{CM} and other transmitter electrical parameters are given. V_{DIFF} maximum value is defined as 1.2 V peak−to−peak, or 0.6 V amplitude, and V_{CM} is defined as a maximum value of 2.2 V at the connector side of the AC coupling capacitors. Since there is no mention of the V_{CM} at the transmitter side of the capacitors we can assume it will be the same. Additionally, a maximum short−circuit current of 60 mA is specified for the transmitter. Given these values, the maximum voltage present on the line is V_{CM} + 0.5 * V_{DIFF} = 2.8 V and the maximum current is 60 mA. For the purpose of the load−line analysis, this corresponds to a load−line between points (I_{SSMAX} = 60 mA, V = 0) and (I = 0, V_{DD} = 2.8 V). Equation 1, given earlier, defines the minimum holding current for the ideal SCR. Given the numbers in this case, the corresponding I_{HMIN} value is 38.6 mA. A protection SCR device with V_{BR} > 2.8 V, I_H > 38.6 mA and V_H > 1 V at I_H will satisfy the latch−up free condition for case 1 of the USB 3.0 SS line.

In evaluating case 2, there is no substantially different information compared to case 1 except that V_{CM} is explicitly defined at the connector side of the AC coupling capacitor. Therefore the maximum voltage present at either one of these nodes is the same as in case 1, or V_{DD} = 2.8 V. However, the difference in case 2 is that because of the coupling capacitors, no DC current can flow from the transmitter through the capacitors and into the protection device. In the USB 3.0 specification, there is no mention of a DC biasing circuit connected to the transmission lines at the connector side. Since a latch−up condition must be created by a DC current flowing into the device, I_{SSMAX} is zero in this case and latch−up is inherently impossible.

Case 3 is similar to case 2. Since the USB 3.0 specification does not mention DC biasing circuits connected to the Rxn or Rxp lines, it can be assumed that there is no possible DC current flowing into these nodes and therefore latch−up is impossible in this configuration.

As a conclusion, only one protection configuration in USB 3.0 is subject to a potential latch−up condition, where the protection device is connected at Txn and Txp nodes immediately between the transmitter chip and the AC coupling capacitors. Incidentally, this is also the least likely configuration to be used in practice because 1) protection is generally placed immediately after the connector 2) the receiver is more likely to be sensitive and 3) the outputs of a transmitter are less sensitive to transients than receiver inputs.

Summary of Latch−Up Requirements for HDMI 1.4, USB 2.0 and 3.0

This section will provide a summary table of the latch−up free requirements for hypothetical SCR−type protection devices used in three potential high−speed applications. It is important to note that the preceding analyses all assume worst case scenarios where the transmitters output the maximum specified voltage constantly into a latched−up device. In practice, a transient condition on the line bringing a protection device into conduction state may temporarily cause a latch−up condition where the transmitter maintains the device in conduction (if it does not satisfy the above determined parameters). However, since data transmission

on the interface will be impeded, it is likely that the transmitters will turn off in relatively short order and reset, which will end the latch−up condition. Only a DC biasing network which may never turn−off based on data transmission protocol could cause a permanent (and thus un−recoverable) latch−up condition.

The analyses shown in this document are repeated, with the difference that transmitter dynamic sources are omitted from the analysis and only DC biasing networks are included. In these cases, one finds that the latch−up free design conditions are less stringent, as described in the following Table 3.

Table 3. SUMMARY OF SCR REQUIREMENTS FOR LATCH−UP FREE APPLICATIONS WITH DYNAMIC SOURCES OMITTED

Application	V_{BR} (Min) (V)	I_H (Min) (mA)	V_H (Min) (V)	ON Semiconductor ESD8000 Series Recommended PN
HDMI 1.4/1.3 TMDS	3.465	54.78	1.0	ESD8040
USB 2.0 LS/FS	3.301	1.76	1.0	ESD8004
USB 2.0 HS	0.482	N/A	1.0	ESD8004
USB 3.0 SS	2.800	N/A	1.0	ESD8004, ESD8006

Conclusion

This application note provides a method to determine safe design parameters for SCR−based protection devices which provide a latch−up free application. From an analysis of the high−speed data lines in three common applications, latch−up conditions must be considered and steps must be taken to avoid latch−up. The ESD8000 series of devices were designed with latch−up considerations in mind and can guarantee that no latch−up conditions can occur due to the device staying in conduction after the transient ESD event.

References

1. −, “High−Definition Multimedia Interface Specification, Version 1.3a”, HDMI Licensing, LLC, 2006.
2. −, “Universal Serial Bus Specification, Version 2.0”, USB Implementers Forum, 2000.
3. −, “Universal Serial Bus 3.0 Specification, Revision 1.0”, USB Implementers Forum, 2008.

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