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NB3H5150 Crystal Oscillator Selector Guide and PCB Layout Guidelines for Best Phase Jitter Performance

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APPLICATION NOTE

Introduction

The goal of this application note is to assist the system design engineers in selecting the appropriate crystal oscillator required for the lowest phase jitter performance for the NB3H5150 device.

The NB3H5150 is a high performance, PLL−based clock generator that accepts a 25 MHz input reference provided by either a crystal or an external crystal oscillator. This reference clock is followed by a PLL that multiplies the reference frequency by the appropriate amount to generate up to four pin−strap selectable or I2C−programmable clock output frequencies of interest.

Today's systems require extremely low jitter timing references to meet end application requirements.

Only the highest performing Clock Generator/Multiplier IC's can provide the necessary low jitter performance for end application requirements.

Phase jitter is derived from an integration of phase noise over a specified bandwidth. For example, many systems specify a jitter integration bandwidth of 12 kHz to 20 MHz. This is because phase noise performance at offsets lower than 10 kHz are dominated primarily by the on−chip crystal oscillator, while the devices' LVPECL / LVCMOS outputs largely set the noise floor for offset frequencies greater than 10 MHz. The remaining intermediate frequencies' phase noise performance is determined by the device's integrated VCO and associated PLL components.

Using an External Crystal Oscillator Signal as the Clock Source

The NB3H5150 can accept an externally generated 25 MHz clock source as the input via a crystal oscillator. The crystal oscillator's output is fed into the NB3H5150 as the input reference to the PLL. Some, but not all crystal oscillators can provide low phase noise and good frequency accuracy that can be used in high performance end applications.

If an external 25 MHz oscillator or other clock sources are used, follow the instructions of Table 2 in the NB3H5150 datasheet.

Table 1. CRYSTAL INPUT INTERFACE AND REFMODE TRUTH TABLE

Input Mode Crystal / External Clock	REFMODE	CLK_XTAL1	CLKb_XTAL2
Crystal	LOW	Use a Crystal	Use a Crystal
Any Differential Input	HIGH	Overdrive with True Input	Overdrive with Complementary Input
Single−Ended Input	HIGH	Overdrive	Connect to Ground

NOTE: REFMODE pin = High will select an external clock reference input.
The single−ended crystal oscillator output can be fed into the CLK_XTAL1 pin;
The differential crystal oscillator outputs can be fed into the CLK_XTAL1 and CLKb_XTAL2 pins.

Phase Noise Performance of the NB3H5150

The quality of the crystal oscillator (or other single−ended) reference input will have a significant effect on the phase jitter performance of the NB3H5150.

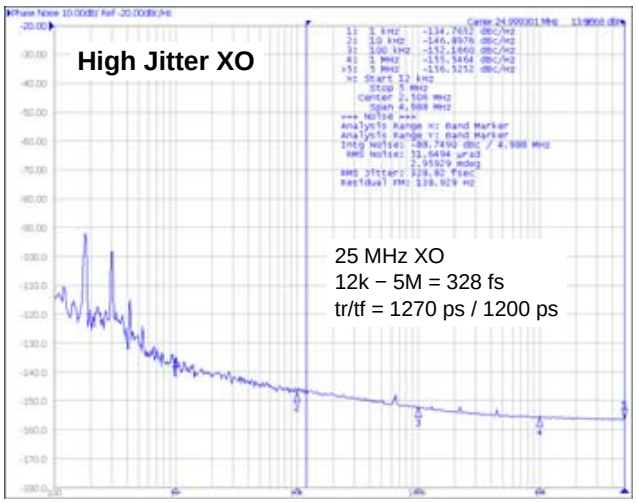
As will be shown, the output phase jitter of the NB3H5150 is dependent on the reference input phase jitter, and proper PCB layout.

In general, a Low Phase Jitter reference input will result in a Low Phase Jitter output from the NB3H5150.

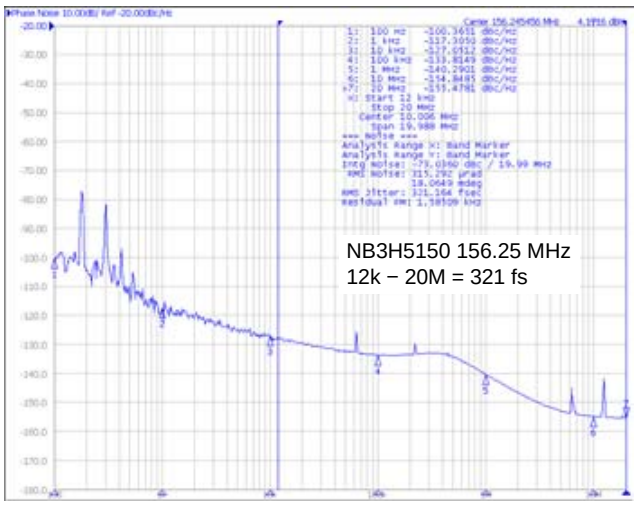
The following Figures compare the output phase jitter performance of the NB3H5150 using a low, average and high phase noise crystal oscillator as measured with a Phase Noise Analyzer.

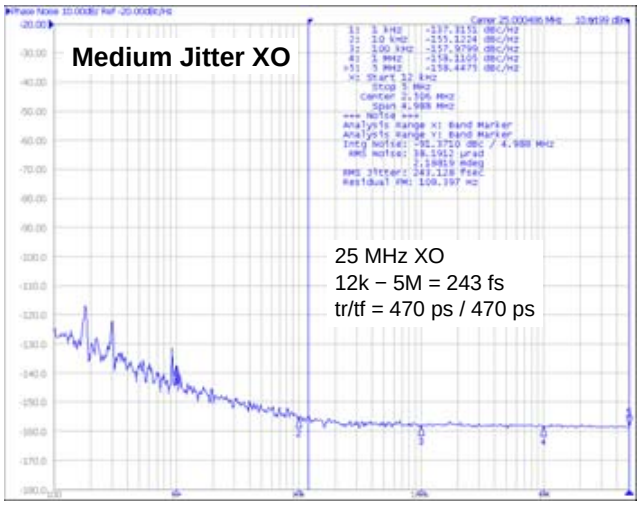
NB3H5150 Phase Jitter Performance (Using Three 25 Mhz Crystal Oscillators)

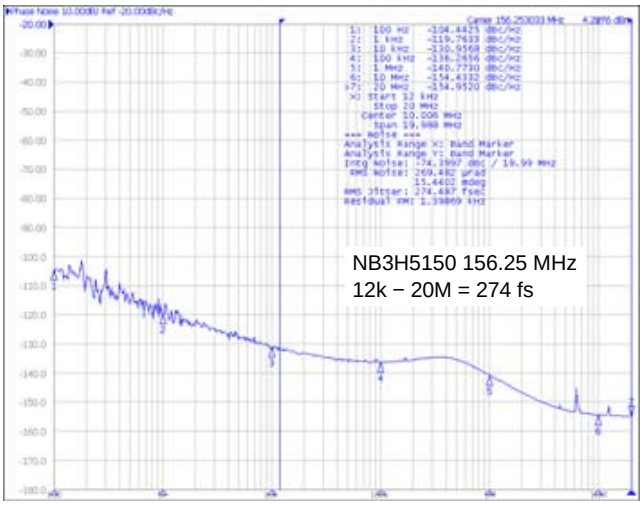
25 MHz Crystal Oscillator
RMS Phase Jitter 12k − 5M

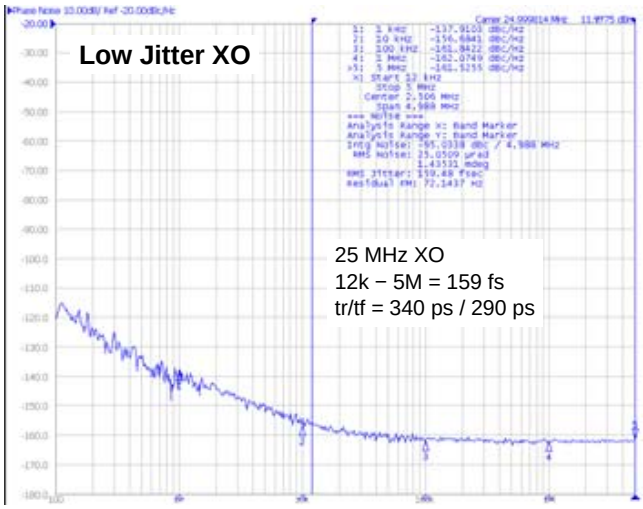


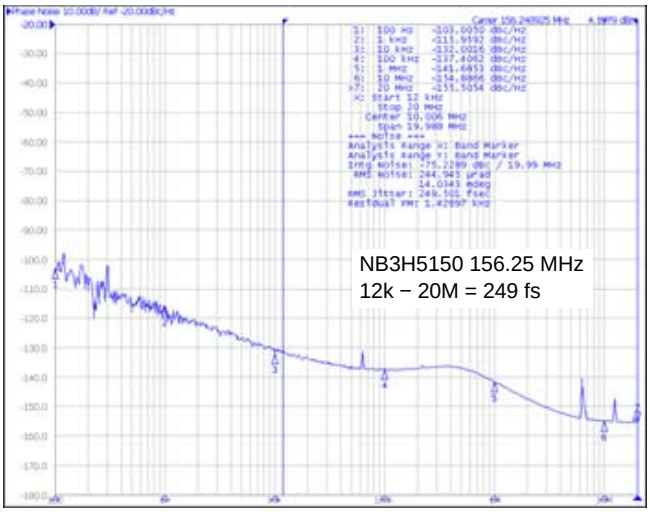
156.25 MHz NB3H5150
RMS Phase Jitter 12k − 20M











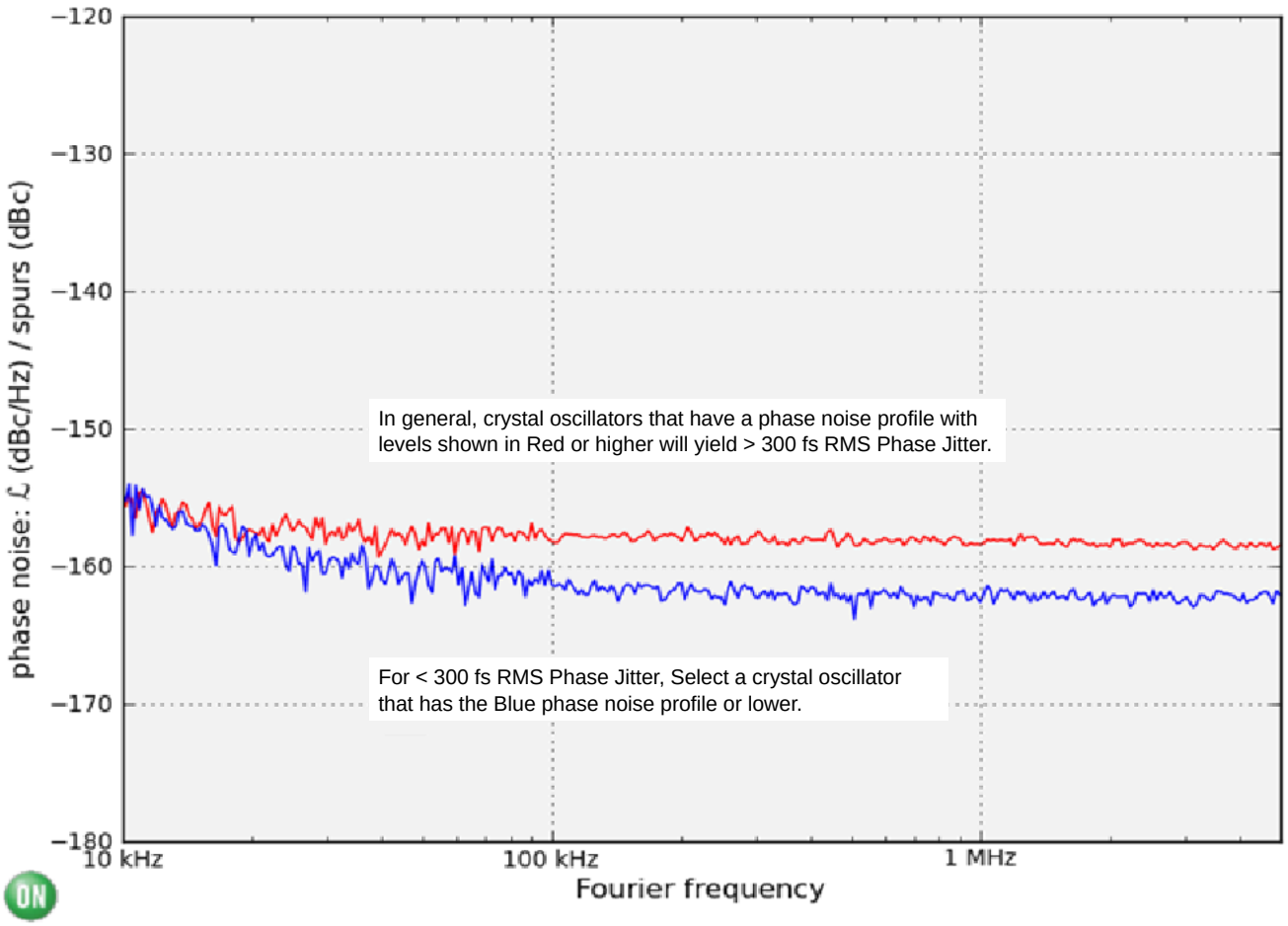


Figure 1. External Crystal Oscillator Frequency = 25 MHz

	Crystal Oscillator Phase Noise (dBc/Hz) @				Measured XO Phase Jitter (fs) 12k−5M Spurs Norm	Measured NB3H5150 Phase Jitter (fs) 12k−20M Spurs Norm	XO tr / tf (ps)	XO Duty Cycle (%)
	10k	100k	1M	5M				
Low Jitter XO	−155	−161	−162	−162	159	249	340 / 290	49.27
Medium Jitter XO	−155	−158	−158	−158	243	274	470 / 470	50.48
High Jitter XO	−146	−152	−155	−156	328	321	1270 / 1200	49.77

Recommendations and Requirements for Selecting a 25 MHz Crystal Oscillator

Crystal Oscillator Selection Guide

Use a 25 MHz crystal oscillator that complies with all of the following parameters simultaneously:

1. **The 25 MHz XO must have Low Phase Jitter** (see phase noise profile Figure above)
2. Fast output edges; **tr / tf < 1 ns**
3. Must be 50% Output Duty Cycle (XOs are typically 50%)

Ultimately, there is a performance advantage using a very low noise crystal oscillator.

In order to achieve < 300 fs RMS phase jitter performance from the NB3H5150, the below crystal oscillator parameters are recommended:

Parameter	Minimum	Typical	Maximum	Units
Frequency		25.000		MHz
Phase Noise Integration Range: 12 kHz to 20 MHz		220	300	fs RMS
Rise & Fall Time: 20% − 80%			500	ps
Duty Cycle	45	50	55	%
Output Levels VOH VOL	 VDD – 0.8 0		 VDD 0.6	V
Overall Frequency Stability	−50		+50	ppm

NOTE: Requirements of the above−mentioned parameters for crystal oscillator were derived from empirical data analysis.

Below is a list of ON Semiconductor recommended 25 MHz Crystal Oscillators that will allow NB3H5150 to supply sub 300 fs phase jitter performance.

Table 2.
RECOMMENDED 25 MHz CRYSTAL OSCILLATORS

XO Mfgr	Orderable Part Number
Abracon	ASFLMX−25.000MHZ−5ABH
NDK	2725T 25.000625MHz ENE 3223A
NDK	2725T−25.000000M−NSA6293E
HOSONIC	D35B25.0000WNS
HOSONIC	D36A25.00065NS
Taitien	CEFCGJ 25.000
Epson Toyocom	TCO−7106X1A425.000000MHz

Crystal Recommendations

In order to achieve < 300 fs RMS phase jitter performance from the NB3H5150, the below crystal parameters are recommended:

Table 3.
RECOMMENDED CRYSTAL SPECIFICATIONS

Crystal	Fundamental AT−Cut
Frequency	25 MHz
Load Capacitance	16 pF − 20 pF
Shunt Capacitance, C0	7 pF Max
Equivalent Series Resistance	50 Ω Max
Initial Accuracy at 25°C	±20 ppm
Temperature Stability	±30 ppm
Aging	±20 ppm
C0/C1 Ratio	250 Max
Crystal max Drive Level	100 μW

NOTE: Requirements of the above−mentioned crystal parameters were derived from empirical data analysis.

Below is a list of ON Semiconductor recommended 25 MHz Crystals that will allow NB3H5150 to supply sub 300 fs phase jitter performance.

Table 4. RECOMMENDED 25 MHz CRYSTALS

XO Mfgr	Orderable Part Number
Abracon	ABL−25.000MHZ−B2F
CTS	MP250B−E
Seiko Epson	FA−238−25.0000MA3DX−C0

PCB Layout Guidelines and Optimization for Reduced Phase Jitter

A PLL is sensitive to board−level noise, so special care must be taken in the design of PCB layout.

Proper PCB layout practices are fundamental in attaining good noise immunity and critical in achieving low phase jitter from the NB3H5150.

PCB Device Input Layout

Crystal Layout

Install the crystal and load capacitors as close to the CLK_XTAL1 and CLKb_XTAL2 pins as possible.

Minimize capacitive coupling between crystal pads / leads and other metal on the PCB.

Ensure that the ground under the crystal is the same ground used for the tuning Cload capacitors.

Crystal Input Interface

Figure 2 shows the NB3H5150 crystal interface using a typical 18 pF parallel resonant crystal. The crystal loading capacitance for the NB3H5150 would use C31 = 18 pF and C32 = 18 pF as nominal values. The frequency accuracy and duty cycle skew can be fine−tuned by adjusting the C31 and C32 values. For example, increasing the C31 and C32 values will reduce the crystal frequency. C31 and C32 values can be optimized and adjusted for various board layouts.

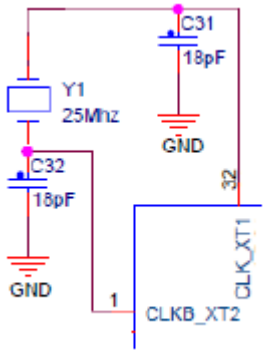


Figure 2. Crystal Input Interface

Crystal Oscillator Input Interfaces – Single−Ended and Differential

The CLK_XTAL1 pin can directly accept a single−ended LVCMOS signal and connect the CLK_XTAL2 pin to GND. A general LVCMOS interface diagram is shown in Figure 3 and a general Differential interface in Figure 4.

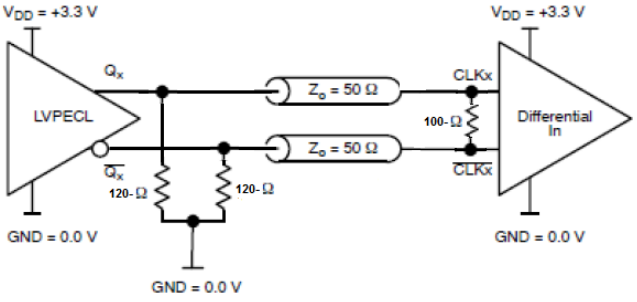


Figure 5. Typical LVPECL Output Loading and Termination

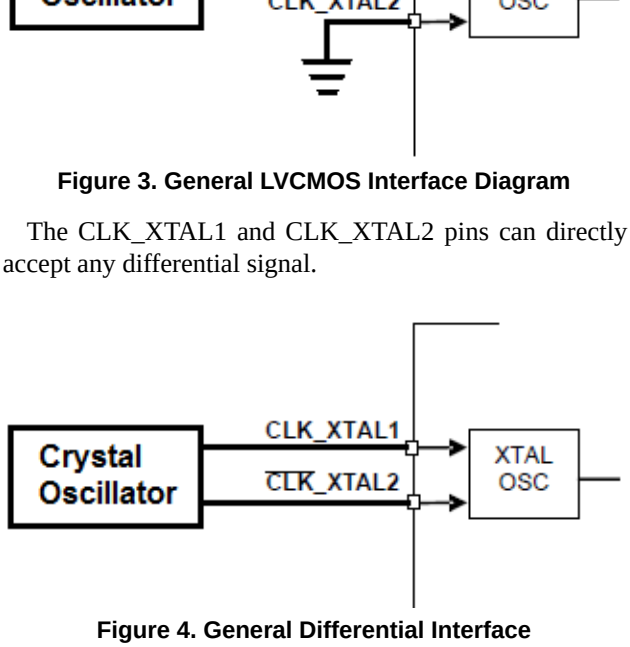


Figure 3. General LVCMOS Interface Diagram

The CLK_XTAL1 and CLK_XTAL2 pins can directly accept any differential signal.

Figure 4. General Differential Interface

PCB Output Layout

Do not use multiple signal layers for the clock output signals.

Avoid the use of vias in the routing of the clock transmission lines. Vias add unwanted inductance to the trace and can cause impedance changes and reflections.

Route the high−frequency traces far from other dynamic circuits to minimize noise coupling.

The differential LVPECL clock outputs must have equal length traces to minimize clock skew, and must be DC loaded and AC terminated equally.

It is recommended that the ground plane underneath the NB3H5150 device and its CLKnA/B output metal runs be solid and uninterrupted to maintain 50−Ω trace impedance.

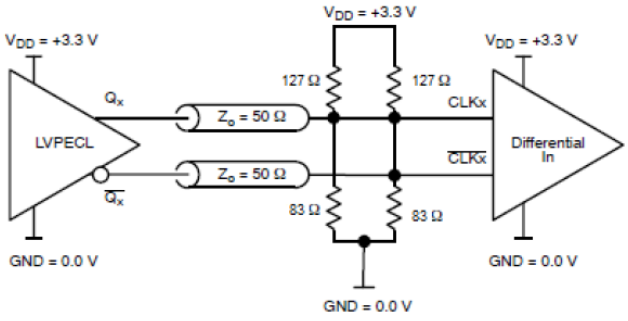


Figure 6. Optional LVPECL Output Loading and Termination

For the LVCMOS clock outputs, place a 33−ohm series termination resistor near the NB3H5150 package pin to match the impedance of the 50−Ω transmission line to minimize reflection. Metal traces from the clock outputs should be as short as possible to minimize reflections and ringing.

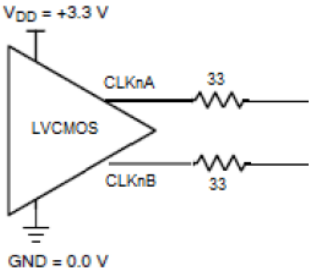


Figure 7. Typical LVCMOS Output Series Termination

Power Supply Filtering Techniques: Isolating Analog and Digital Power Supplies for NB3H5150 PLL−Based Devices

Figure 8 is the recommended power supply decoupling circuit configuration. It is recommended to put 0.1 μF decoupling capacitors on each VDD pin. In addition to the 0.1 μF capacitors, it is also recommended to put a 10 μF decoupling capacitor near the VDD pins to stabilize the power supply. A ferrite bead is also recommended for isolating the main power supply of the NB3H5150 and other power supplies on the system board.

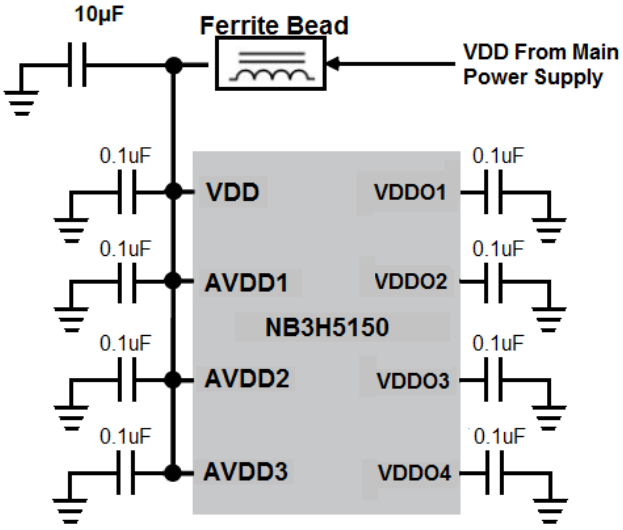


Figure 8. General Recommended Power Supply Decoupling Circuit Diagram

Noise is a common cause of system problems and the power supply pins are vulnerable to random and deterministic noise.

In PLL−based systems, power supply noise is a major cause of jitter. Therefore, bypassing is essential to optimum high speed circuit performance.

To achieve best jitter performance from the NB3H5150, power supply isolation is required.

The NB3H5150 provides separate power supply pins (VDD, AVDD1−3, VDDO1−4) to help isolate any high switching noise from coupling into the internal PLL.

Reducing the power supply noise can be accomplished by observing the following recommendations:

In order to achieve the best possible filtering, it is recommended that placement of the filter components be on the device side of the PCB as close to the power pins as possible.

The 0.1 μF capacitors in each VDDOn power pin filter must be placed on the device side.

If space is limited, the other components can be placed on the bottom side of the PCB.

Power supply filter recommendations are a general guideline to be used for reducing external noise from coupling into the NB3H5150. Figure 10 is a recommended power supply filter scheme for the NB3H5150.

Keep power and ground planes close together. This reduces power−supply noise.

Decoupling Capacitors

To minimize coupling on the power and ground rails due to fluctuations, it is recommended that each power supply have a dedicated filter.

To filter the high−frequency noise at the device, all power supply decoupling capacitors should be attached as close as possible to each VDD and GND pair.

For decoupling, high quality, surface−mount ceramic chip capacitors are recommended for their low lead inductance, and low−ESR.

Typically, 0.1 μF capacitors should be connected between each VDD power pin and ground.

Ferrite Beads

To filter power supply noise, use a non−resonant, surface−mount ferrite bead large enough to handle the current in series with the power supply.

The ferrite bead prevents high−frequency noise coming from the VDD source from reaching the device power supply pins. Any low frequency noise is filtered by a 10 μF and 0.1 μF capacitors after the ferrite bead.

Inserting a surface mount ferrite bead between the four VDDOn clock generators's output power supplies and the main PCB power plane will provide high−frequency noise isolation and effectively eliminate this problem.

Ferrite beads neither enhance nor degrade the performance of a clock generator; they merely provide noise isolation.

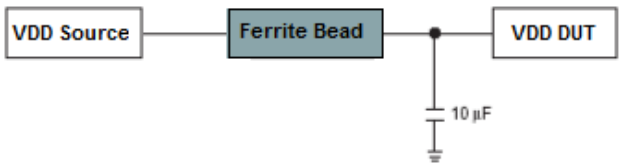
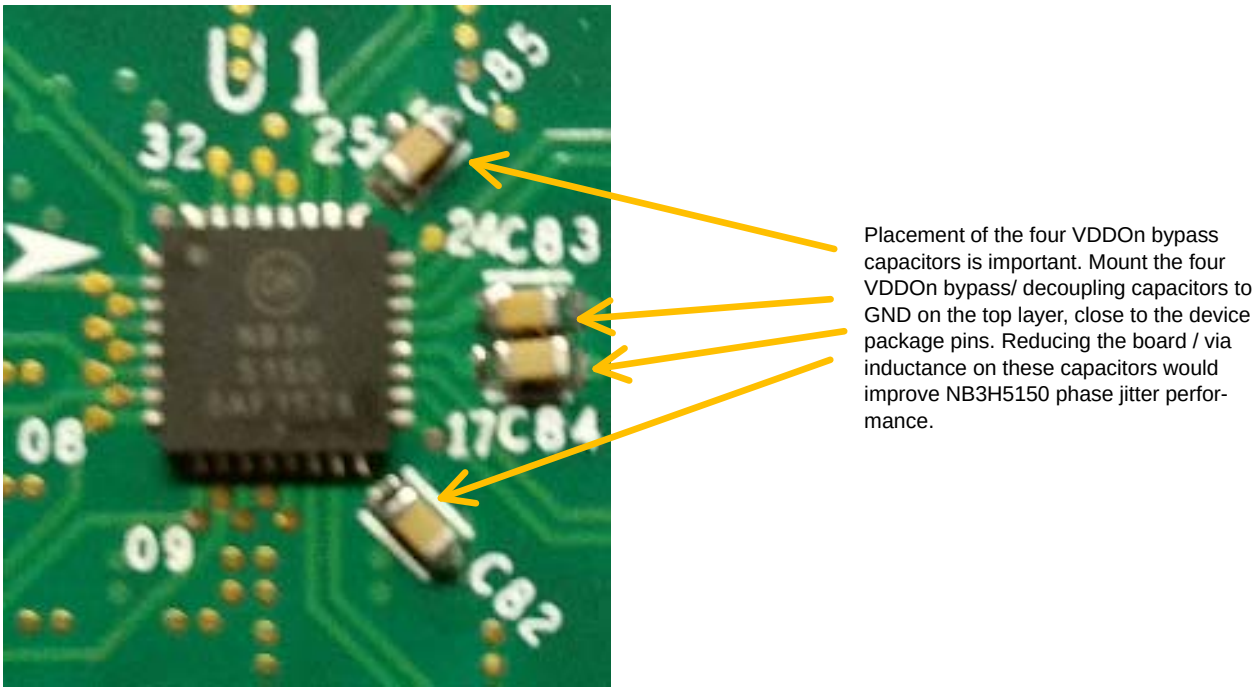


Figure 9. Power Supply Noise Filtering Example

The figure and schematic below are a recommended power supply filtering / decoupling layout scheme and ground noise reduction techniques through the use of bypass capacitors and ferrite beads for VDD, AVDDn and VDDOn.



NB3H5150 Recommended Power Supply Decoupling Circuit Schematic

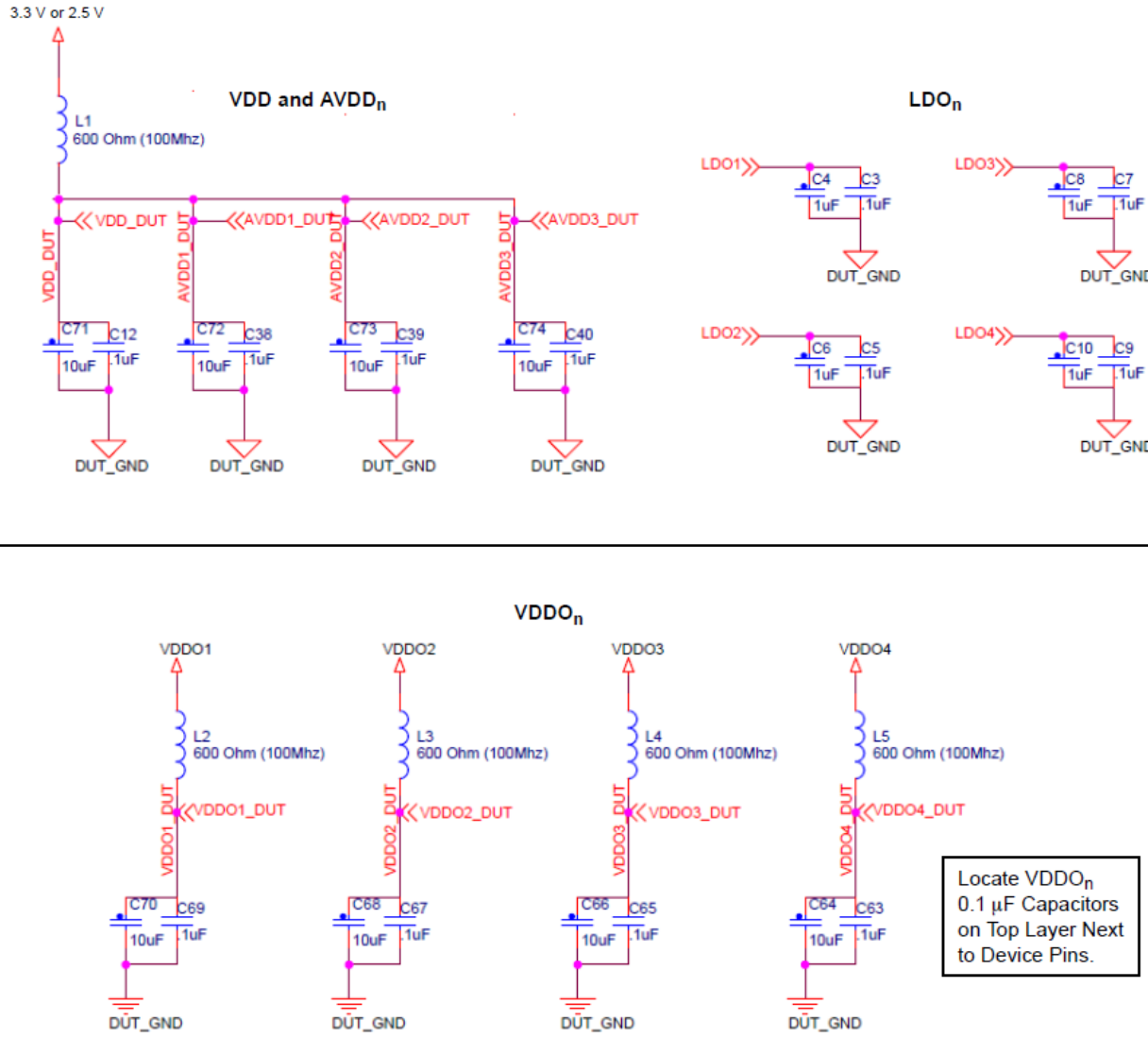


Figure 10. NB3H5150 Power Supply Filter Schemes

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