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Lessons Learned from using LV8907UW in a BLDC Motor Application

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APPLICATION NOTE

Abstract

Tuning tips and tricks for key parameters are described. This device has flexibility for various motors with the use of internal registers and external components. In this note, it is shown how to determine the register and component values to match motors mechanical parameters.

Risks and their mitigation proposals are also shown in this note.

Parameter Tuning:

- Decoupling Capacitors
- Charge Pump Capacitors
- Resistor and Capacitor Values for a Power FET Gate
- Lead Angle

Risks and Their Mitigation:

- Parameter Dependency on the Rotor Speed
- Loss of Commutation Synchronization and Over Current

PARAMETER TUNING

Decoupling capacitors

The Node VS:

10 μF 50 V and 0.1 μF 50 V (multilayer ceramic capacitor) are recommended. This node is affected by the fly back with PWM switching.

The Node V3RO:

4.7 μF 50 V is recommended. It is required to make the regulator stable.

The Node VCC:

4.7 μF 50 V is recommended. It is required to make the regulator stable. If the internal regulator is not used, the capacitor is not required, but the circuit must be inactivated by the register VCEN = 0 in OTP.

Charge Pump Capacitors

Calculate using the following tables. The tables show an example of the case of the NVD5803NT4G, which is used in the evaluation board, the input capacitance C_{iss} is 3220 pF.

Table 1. FOR OUTPUT CAPACITOR CCHP/CVGL CALCULATION

Item	Parameter	Symbol	Value	Unit	Description
FET	Input capacitance	C_{iss}	3220	pF	parameter of MOSFET's input capacitance
Capacitor	Minimum value of output capacitor	C_{gmin}	0.161	μF	Capacity value to limit voltage fluctuation within 2% when charged to C_{iss}. Calculate 50 times C_{iss}. $C_{gmin} = C_{iss} \times 50$
Result	Recommended value of output capacitor	C_{grec}	0.40	μF	$C_{gmin} \times 2.5$

Table 2. FOR TRANSFER CAPACITOR CP1/CP2 CALCULATION

Item	Parameter	Symbol	Value	Unit	Description
MOSFET	Input capacitance	C_{iss}	3220	pF	MOSFET's input capacitance
LV8907	MOSFET gate drive voltage	V_G	12	V	Drive voltage for MOSFET gate
	Drive PWM frequency	f_{pwm}	20	kHz	MOSFET's gate charge frequency
	Charge pump frequency	f_{cp}	50	kHz	
	Current capability in charge pump (MOSFET's drive current + IC consumption current)	I_{cp}	3.55	mA	Calculate the current required for the charge pump $I_{cp} = (C_{iss} \times V_G \times f_{pwm}) \times 2 + I_{dc}$ MOSFET's drive current: $C_{iss} \times V_G \times f_{pwm} \times 2$MOSFET Icconsumption current: I_{dc} = 2 mA
	Voltage drop inside IC	V_{dic}	0.96	V	Calculate the voltage drop inside the IC $V_{dic} = I_{cp} \times 2.5 \times$ Ricma The DC current is calculated in Icp. In actual charge pump operation, it is operating at 50% duty. Assuming that the ratio of current generation to all the switches in the IC is 40%, the current needs 2.5 times (100% / 40%). For this reason, it is necessary to calculate the current value at 2.5 times. Total internal resistance value in charge pump block: Ricmax = 108 Ω
Capacitor	Allowable Charge Pump Voltage Drop	V_{drop}	4.50	V	Allowable voltage drop when CHP voltage = V_S + 6.5 V at V_S = 5.5 V (Full function operation minimum). $V_{CHP} = V_S + V_{GL} - V_{drop} > V_S$ + 6.5 V $V_{GL} = V_S \times 2 - V_{drop} > 6.5$ V = 5.5 V × 2 – $V_{drop} > 6.5$ V $V_{drop} < 11$ V – 6.5 V = 4.5 V
	Allowable transfer capacitor Voltage Drop	V_{dct}	1.77	V	Calculate the voltage drop allowed at the transfer capacitor $(V_{drop} - V_{dic}) / 2$ The voltage drop value allowed by the transfer capacitor can be calculated by $V_{drop} - V_{dic}$. Since it is a configuration of two stages of capacitors, obtain an allowable voltage drop per piece. (× 1/2)
	Minimum value of transfer capacitor	C_{tmin}	0.04	μF	Calculate the capacitance value at which V_{dct} occurs when I_{cp} current is consumed $C_{tmin} = I_{cp} / (V_{dct} \times f_{cp})$ Charge pump frequency: f_{cp} = 50 kHz
Result	Recommended value of transfer capacitor	C_{trec}	0.10	μF	$C_{trec} = C_{tmin} \times 2.5$

Resistor and Capacitor Values for a Power FET Gate

Figure 1 shows an example topology between LV8907UW gate driver output and power FETs.

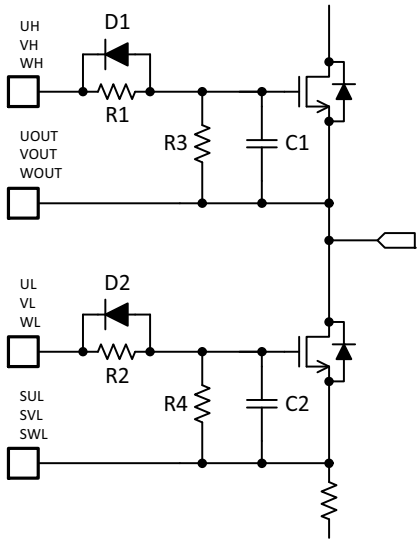

Figure 1. Gate Circuit

The resistor and capacitor network is used in:

- Limiting the gate driver current
- Controlling the switching slew rate
- Avoiding floating gate
- Avoiding shoot through

The tuning method is as shown below:

Step 1. Get the input capacitance C_{iss} of the power FET from its catalog or SPICE model. In case of NVD5803NT4G, which is used in the evaluation board, the input capacitance C_{iss} is 3220 [pF]. This capacitance will be referred to the time constant of the gate switching pulse.

Step 2. Determine R1/R2 and C1/C2:
The resistance must be higher than 29 Ω, because:
– the driver capability is 400 mA peak,
– the driver on-resistance is 6 Ω minimum,
– the driver voltage 14 V maximum.
This determines the time constant of the gate switching pulse. Higher slew rates give lower switching loss. However, slower slew rates produce less electrical noise. Based on these characteristics of the slew rates, appropriate target value should be defined before calculating the component parameters. For example, if the internal fixed PWM frequency of 19.5 kHz is selected, and we choose to use approximately 90% of the 1 μs rising time then the time constant τ can be simply calculated from a step response of the CR circuit

$$1 - e^{-\frac{1\,\mu}{\tau}} = 0.9$$

$$\tau = -\frac{1\,\mu}{2.3} = 0.43\,\mu$$

C1 = C2 = 1000 pF
C_{iss} = 3220 pF
R1 = R2 = 100 Ω
τ = 0.422 μ
It is closed to the target 0.43 . It is assumed that the falling time is same.

Step 3. Determine the dead time:
LV8907UW has capability of the dead time adjustment with the register FDTI[4:0], by which both of the high and low side FET is turned off. The falling time of the gate is 1 μs. To have the margin against the component variation, the dead time should be longer than the falling time.
If needed, the diodes D1 and D2 make the discharge time shorter than the charge time to secure the dead time.

A steep step voltage at the output node could make a spike at the power FET gate node, going through the gate capacitance C_{GD} for low side and C_{GS} for high side. Figure 2 shows the case of low side. It has a possibility of shoot through. To avoid this, higher capacitance of C1/C2 can be helpful. It reduce the impedance between gate and source.

The lower slew rate at the other side FET give the smaller spike as well.

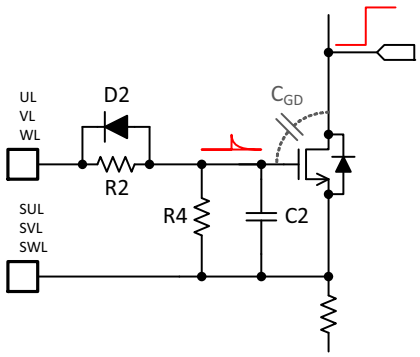

Figure 2. Spike in the Low Side Gate

Lead Angle

Usually, a lead angle adjustment is required to tune the power efficiency by compensation of the coil current (equivalent to torque) phase delay versus BEMF (equivalent to rotor angle). In this application note another effect of the lead angle is mentioned.

In LV8907, the coil current is turned off to observe the BEMF. At this moment, a large fly back pulse is generated and the BEMF due to rotor rotation may be unstable. To

minimize the fly back, the coil current prior to turning off should be minimized. The lead angle adjustment function may be useful for this purpose.

Figure 3 shows an example waveform without the lead angle adjustment. The yellow line is the coil current. At the point of turning off high current flows. Since current cannot change instantaneously in an inductive circuit a large flyback voltage pulse is generated. Figure 4 shows the case of the adjusted lead angle. The current (yellow line) shows a smaller change in amplitude at the point of turning off generating much less electrical stress and switching noise.

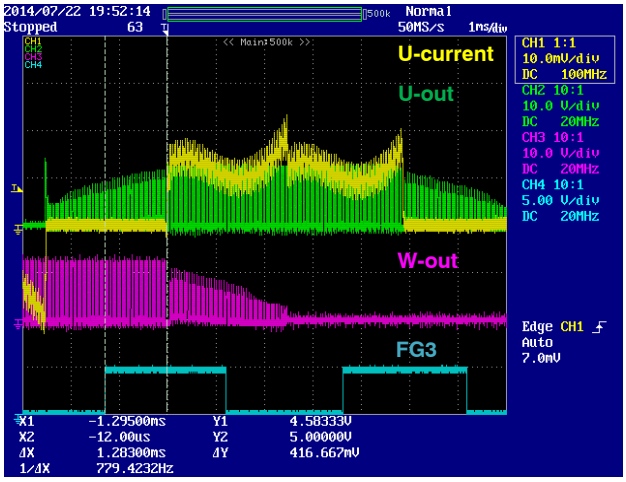

Figure 3. Without Lead Angle Adjustment

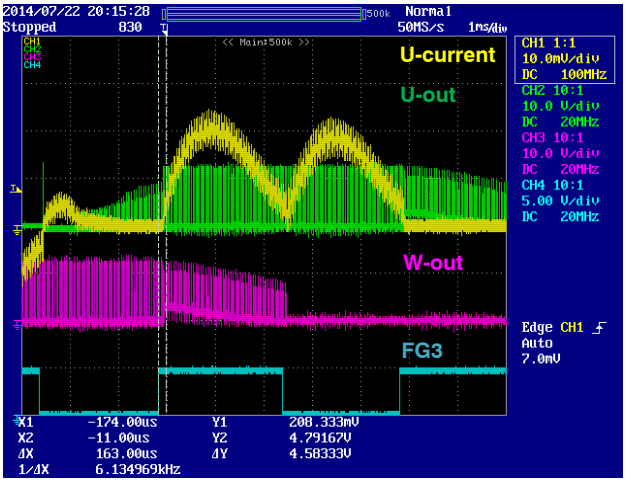

Figure 4. With Lead Angle Adjustment

RISKS AND THEIR MITIGATION

Dynamic Parameter Change Based on the Rotor Speed

The parameters below are adjustable with LV8907UW register settings. Since they have a rotation speed dependency it is better to tweak these parameters based on the rotor speed. But once a register setting is written into the OTP memory the parameters cannot be changed by LV8907UW itself. Therefore, there is a risk that the following parameters cannot be tuned best for all of the required rotational speed range.

- Wave shaping (120/150 degree drive) for acoustic noise reduction.
- PI gain for the on-chip closed loop speed control.
- Lead angle for torque improvement and electrical noise reduction.

It is possible to change many parameters dynamically with register changes while running without changing the OTP contents. This allows a default operation (Limp Home) to be in the OTP and still allows dynamic runtime control for advanced systems.

The following table shows an example of dynamic parameter control, but many parameters can be modified as the rotor speed changes to optimize the drive of a particular motor over a wide speed range.

Table 3. DYNAMIC PARAMETER CONTROL

RPM	Wave shaping	PI gain	Lead angle
Lower	Trapezoidal	Lower	Lower
Higher	Pseudo-sinusoidal	Higher	Higher

Loss of Commutation Synchronization and Over Current

Risk

The loss of commutation synchronization can be caused by the following cases:

- The connection(s) between the driver and the motor are momentarily disconnected and then reconnected such as a loose or worn connector.
- The PWM duty cycle is changed drastically.
- The rotor speed is changed (acceleration, deceleration, or reverse) drastically by an external force.

LV8907UW doesn't always detect this loss of commutation synchronization and keeps trying to apply current to the motor windings based on a false BEMF zero cross detection. When the BEMF voltage polarity is inverted against the applied driving voltage, over current of the motor coil will occur. Therefore, there is the risk of physical damage caused by this unexpected over current.

Detection

When the commutation synchronization is lost, a BEMF zero crossing cannot be found within the detection window, or a false detection is generated. It can be estimated with the FG (tachometer) pulse period by external monitoring. The condition to determine the loss of commutation synchronization is:

- The rotation speed recognized from FG pulse period is much higher or much lower than the physical rotor speed.
- The FG pulse period difference from the previous cycle is much larger than the possible physical rotor rate of change.

Figure 5 shows example waveform in the case that the commutation synchronization is lost. The coil current (Orange plot) shows abnormally high currents. FG pulse period changes drastically.

Mitigation

The connections between the controller and the motor must be insured, and it is always maintained.

The difference of PWM duty cycle change within short time must be limited.

The FG pulse must be monitored. When the loss of commutation synchronization is detected by the abnormal FG pulse train described above, LV8907UW must be restarted. By setting the rotation enable pin, EN, to a logical low state, the driver output is deactivated to halt the over current situation. After this deactivation, the pin EN should be set logical high to restart. The LV8907UW will enter its normal startup sequence and regain synchronization. To enable this resynchronization of LV8907UW, the register bit named FRREN must be set 0. (See datasheet for detail).

Figure 5 also shows example waveform of resynchronization by toggling EN pin. The EN pin should be set low immediately when incoherent FG pulse detected in an actual application.

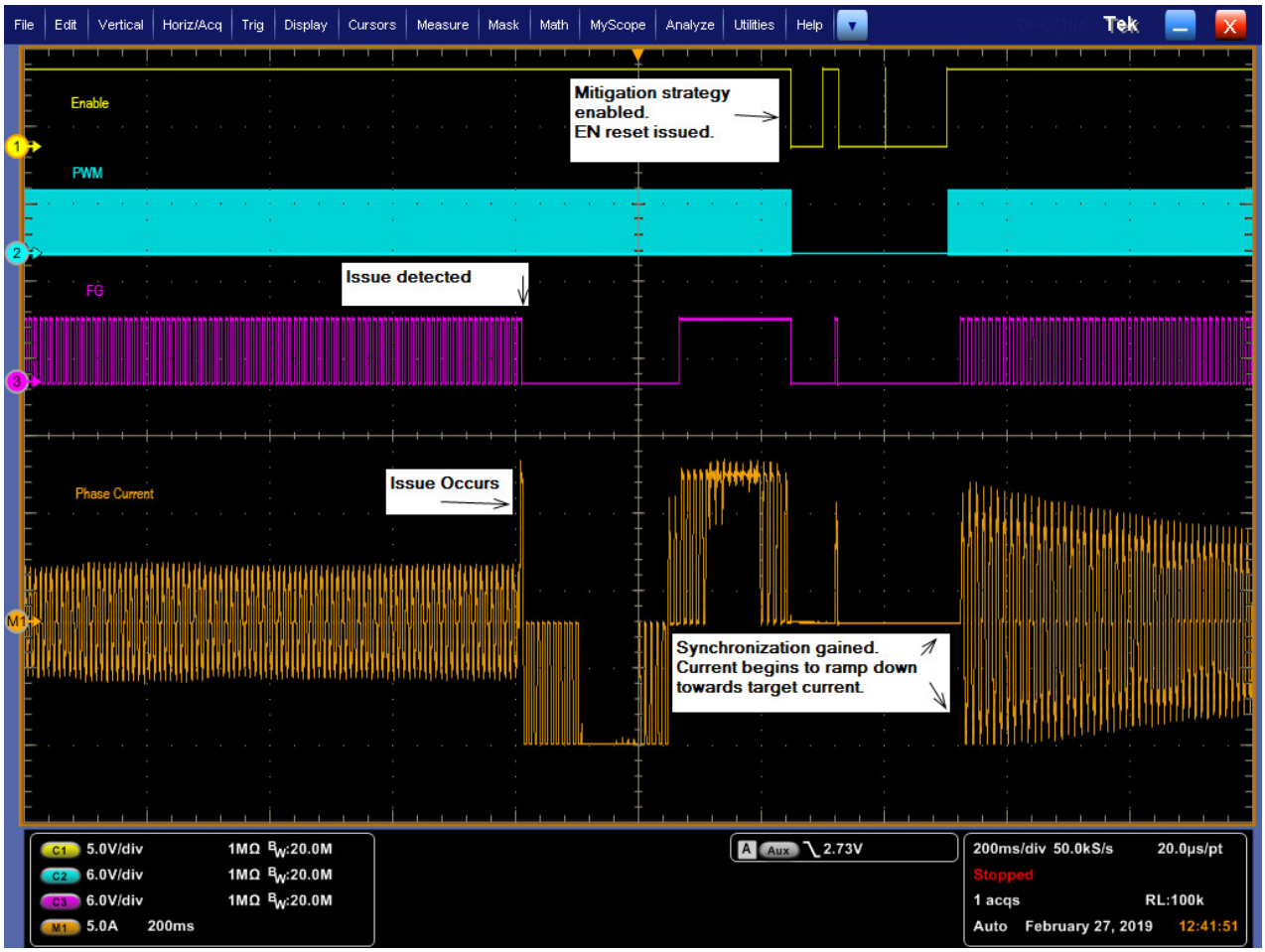

Figure 5. Example Waveform

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