

# NPN - 2N6515, 2N6517; PNP - 2N6520

## High Voltage Transistors

### NPN and PNP

#### Features

- Voltage and Current are Negative for PNP Transistors
- These are Pb-Free Devices\*

#### MAXIMUM RATINGS

| Rating   | Symbol         | Value       | Unit                       |
|--|----------------|-------------|----------------------------|
| Collector – Emitter Voltage<br>2N6515<br>2N6517, 2N6520                                | $V_{CEO}$      | 250<br>350  | Vdc                        |
| Collector – Base Voltage<br>2N6515<br>2N6517, 2N6520                                   | $V_{CBO}$      | 250<br>350  | Vdc                        |
| Emitter – Base Voltage<br>2N6515, 2N6517<br>2N6520                                     | $V_{EBO}$      | 6.0<br>5.0  | Vdc                        |
| Base Current   | $I_B$          | 250         | mA <sub>dc</sub>           |
| Collector Current – Continuous   | $I_C$          | 500         | mA <sub>dc</sub>           |
| Total Device Dissipation @ $T_A = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 625<br>5.0  | mW<br>mW/ $^\circ\text{C}$ |
| Total Device Dissipation @ $T_C = 25^\circ\text{C}$<br>Derate above $25^\circ\text{C}$ | $P_D$          | 1.5<br>12   | W<br>mW/ $^\circ\text{C}$  |
| Operating and Storage Junction<br>Temperature Range                                    | $T_J, T_{stg}$ | -55 to +150 | $^\circ\text{C}$           |

#### THERMAL CHARACTERISTICS

| Characteristic                          | Symbol          | Max  | Unit               |
|---|-----------------|------|--------------------|
| Thermal Resistance, Junction-to-Ambient | $R_{\theta JA}$ | 200  | $^\circ\text{C/W}$ |
| Thermal Resistance, Junction-to-Case    | $R_{\theta JC}$ | 83.3 | $^\circ\text{C/W}$ |

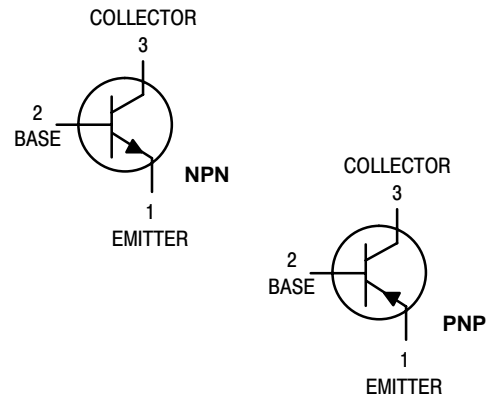
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

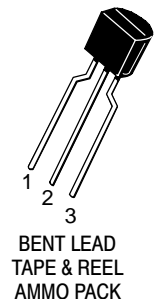
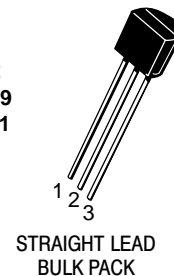


ON Semiconductor®

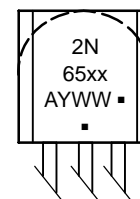
<http://onsemi.com>



TO-92  
CASE 29  
STYLE 1



#### MARKING DIAGRAM



xx = 15, 17, or 20  
A = Assembly Location  
Y = Year  
WW = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

# NPN – 2N6515, 2N6517; PNP – 2N6520

## ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C unless otherwise noted)

| Characteristic   | Symbol               | Min        | Max      | Unit             |
|--|----------------------|------------|----------|------------------|
| <b>OFF CHARACTERISTICS</b>   |                      |            |          |                  |
| Collector–Emitter Breakdown Voltage (Note 1)<br>(I <sub>C</sub> = 1.0 mA <sub>dc</sub> , I <sub>B</sub> = 0)   | V <sub>(BR)CEO</sub> | 250<br>350 | –<br>–   | V <sub>dc</sub>  |
| Collector–Base Breakdown Voltage<br>(I <sub>C</sub> = 100 μA <sub>dc</sub> , I <sub>E</sub> = 0)   | V <sub>(BR)CBO</sub> | 250<br>350 | –<br>–   | V <sub>dc</sub>  |
| Emitter–Base Breakdown Voltage<br>(I <sub>E</sub> = 10 μA <sub>dc</sub> , I <sub>C</sub> = 0)  | V <sub>(BR)EBO</sub> | 6.0<br>5.0 | –<br>–   | V <sub>dc</sub>  |
| Collector Cutoff Current<br>(V <sub>CB</sub> = 150 V <sub>dc</sub> , I <sub>E</sub> = 0)<br>(V <sub>CB</sub> = 250 V <sub>dc</sub> , I <sub>E</sub> = 0) | I <sub>CBO</sub>     | –<br>–     | 50<br>50 | nA <sub>dc</sub> |
| Emitter Cutoff Current<br>(V <sub>EB</sub> = 5.0 V <sub>dc</sub> , I <sub>C</sub> = 0)<br>(V <sub>EB</sub> = 4.0 V <sub>dc</sub> , I <sub>C</sub> = 0)   | I <sub>EBO</sub>     | –<br>–     | 50<br>50 | nA <sub>dc</sub> |

## ON CHARACTERISTICS (Note 1)

|  |                      |                  |                             |                 |
|--|----------------------|------------------|-----------------------------|-----------------|
| DC Current Gain<br>(I <sub>C</sub> = 1.0 mA <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> )   | h <sub>FE</sub>      | 35<br>20         | –<br>–                      | –               |
| (I <sub>C</sub> = 10 mA <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> )   |                      | 50<br>30         | –<br>–                      |                 |
| (I <sub>C</sub> = 30 mA <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> )   |                      | 50<br>30         | 300<br>200                  |                 |
| (I <sub>C</sub> = 50 mA <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> )   |                      | 45<br>20         | 220<br>200                  |                 |
| (I <sub>C</sub> = 100 mA <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> )  |                      | 25<br>15         | –<br>–                      |                 |
| Collector–Emitter Saturation Voltage<br>(I <sub>C</sub> = 10 mA <sub>dc</sub> , I <sub>B</sub> = 1.0 mA <sub>dc</sub> )<br>(I <sub>C</sub> = 20 mA <sub>dc</sub> , I <sub>B</sub> = 2.0 mA <sub>dc</sub> )<br>(I <sub>C</sub> = 30 mA <sub>dc</sub> , I <sub>B</sub> = 3.0 mA <sub>dc</sub> )<br>(I <sub>C</sub> = 50 mA <sub>dc</sub> , I <sub>B</sub> = 5.0 mA <sub>dc</sub> ) | V <sub>CE(sat)</sub> | –<br>–<br>–<br>– | 0.30<br>0.35<br>0.50<br>1.0 | V <sub>dc</sub> |
| Base–Emitter Saturation Voltage<br>(I <sub>C</sub> = 10 mA <sub>dc</sub> , I <sub>B</sub> = 1.0 mA <sub>dc</sub> )<br>(I <sub>C</sub> = 20 mA <sub>dc</sub> , I <sub>B</sub> = 2.0 mA <sub>dc</sub> )<br>(I <sub>C</sub> = 30 mA <sub>dc</sub> , I <sub>B</sub> = 3.0 mA <sub>dc</sub> )   | V <sub>BE(sat)</sub> | –<br>–<br>–      | 0.75<br>0.85<br>0.90        | V <sub>dc</sub> |
| Base–Emitter On Voltage<br>(I <sub>C</sub> = 100 mA <sub>dc</sub> , V <sub>CE</sub> = 10 V <sub>dc</sub> )   | V <sub>BE(on)</sub>  | –                | 2.0                         | V <sub>dc</sub> |

## SMALL–SIGNAL CHARACTERISTICS

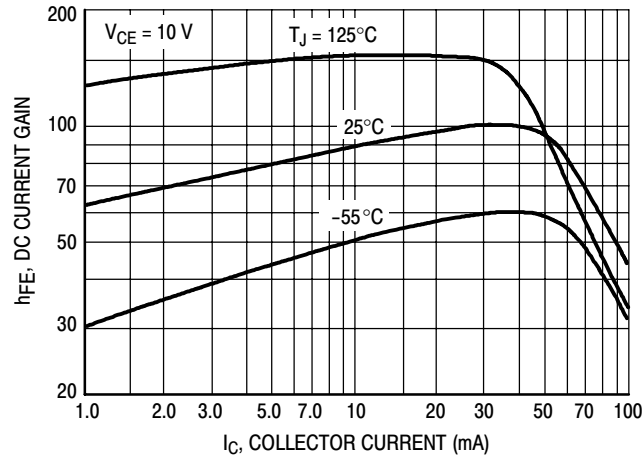
|   |                 |        |           |     |
|---|-----------------|--------|-----------|-----|
| Current–Gain – Bandwidth Product (Note 1)<br>(I <sub>C</sub> = 10 mA <sub>dc</sub> , V <sub>CE</sub> = 20 V <sub>dc</sub> , f = 20 MHz) | f <sub>T</sub>  | 40     | 200       | MHz |
| Collector–Base Capacitance<br>(V <sub>CB</sub> = 20 V <sub>dc</sub> , I <sub>E</sub> = 0, f = 1.0 MHz)                                  | C <sub>cb</sub> | –      | 6.0       | pF  |
| Emitter–Base Capacitance<br>(V <sub>EB</sub> = 0.5 V <sub>dc</sub> , I <sub>C</sub> = 0, f = 1.0 MHz)                                   | C <sub>eb</sub> | –<br>– | 80<br>100 | pF  |

## SWITCHING CHARACTERISTICS

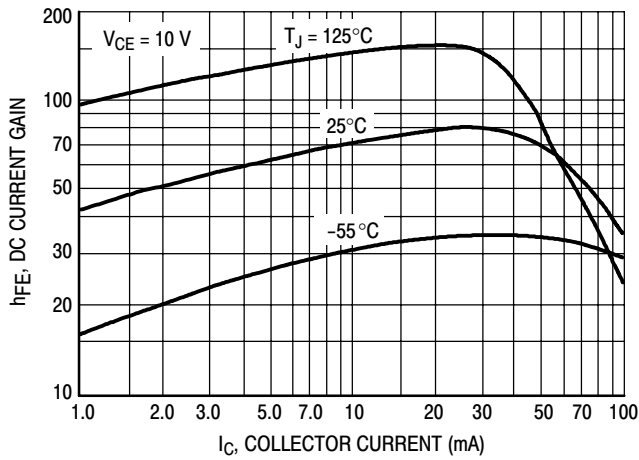
|  |                  |   |     |    |
|--|------------------|---|-----|----|
| Turn–On Time<br>(V <sub>CC</sub> = 100 V <sub>dc</sub> , V <sub>BE(off)</sub> = 2.0 V <sub>dc</sub> , I <sub>C</sub> = 50 mA <sub>dc</sub> , I <sub>B1</sub> = 10 mA <sub>dc</sub> ) | t <sub>on</sub>  | – | 200 | μs |
| Turn–Off Time<br>(V <sub>CC</sub> = 100 V <sub>dc</sub> , I <sub>C</sub> = 50 mA <sub>dc</sub> , I <sub>B1</sub> = I <sub>B2</sub> = 10 mA <sub>dc</sub> )                           | t <sub>off</sub> | – | 3.5 | μs |

1. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%.

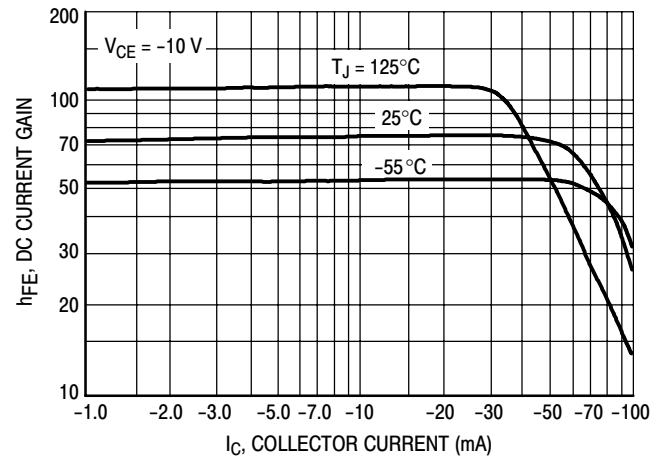
# NPN – 2N6515, 2N6517; PNP – 2N6520



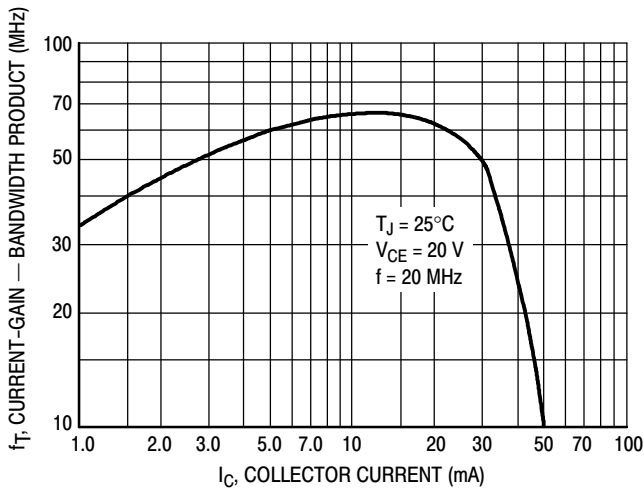
**Figure 1. DC Current Gain  
NPN 2N6515**



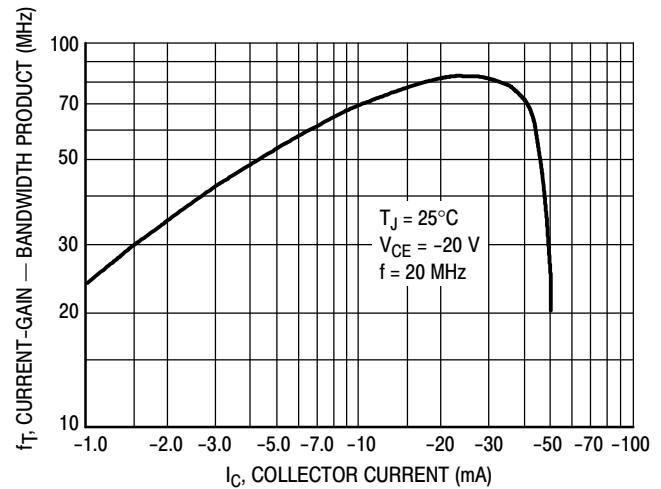
**Figure 2. DC Current Gain  
NPN 2N6517**



**Figure 3. DC Current Gain  
PNP 2N6520**

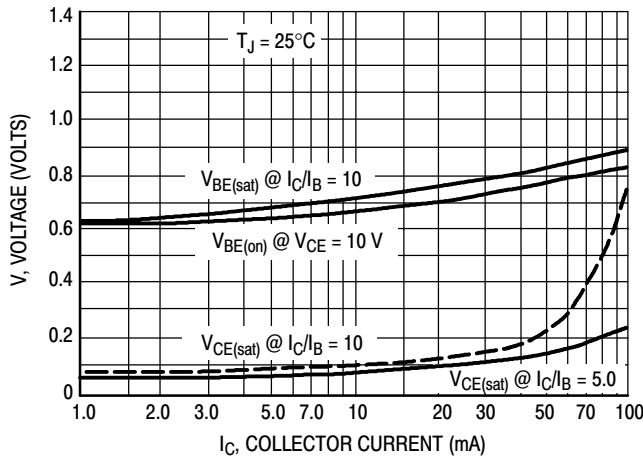


**Figure 4. Current-Gain – Bandwidth Product  
NPN 2N6515, 2N6517**

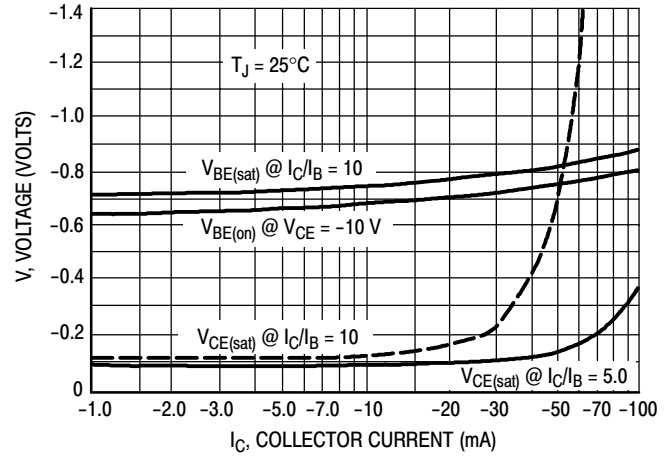


**Figure 5. Current-Gain – Bandwidth Product  
PNP 2N6520**

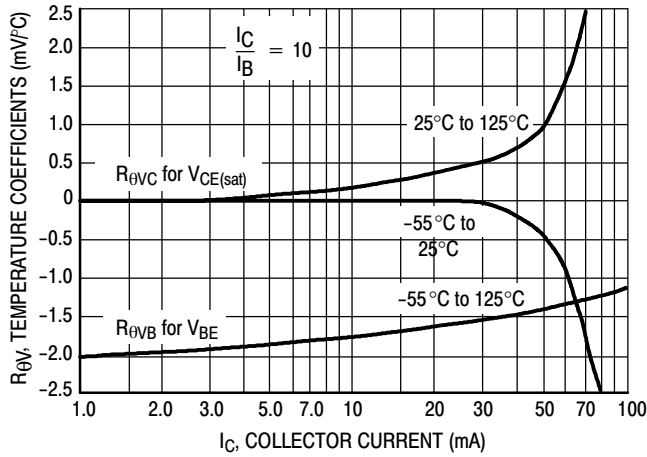
# NPN – 2N6515, 2N6517; PNP – 2N6520



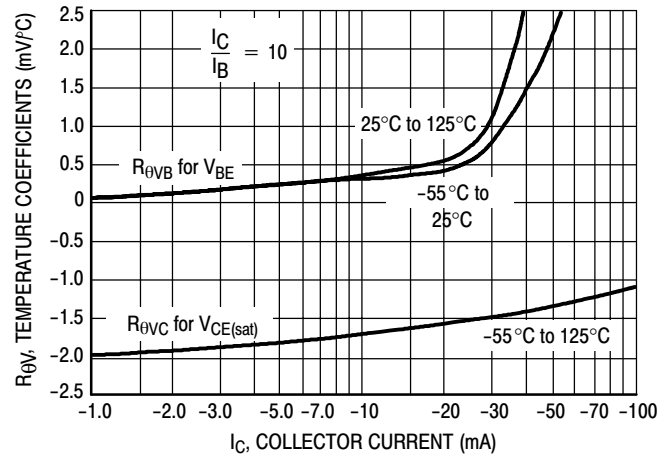
**Figure 6. "On" Voltages  
NPN 2N6515, 2N6517**



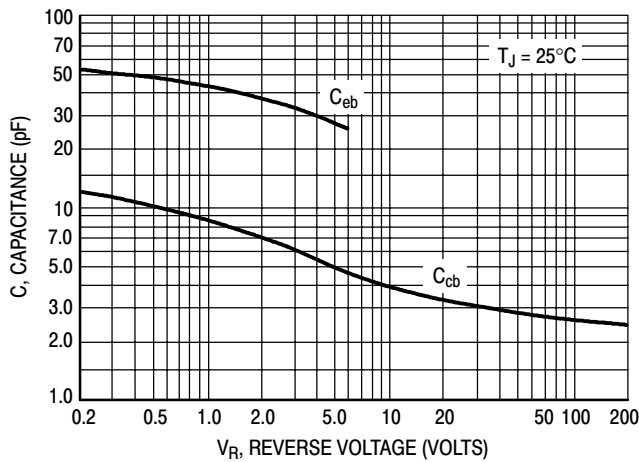
**Figure 7. "On" Voltages  
PNP 2N6520**



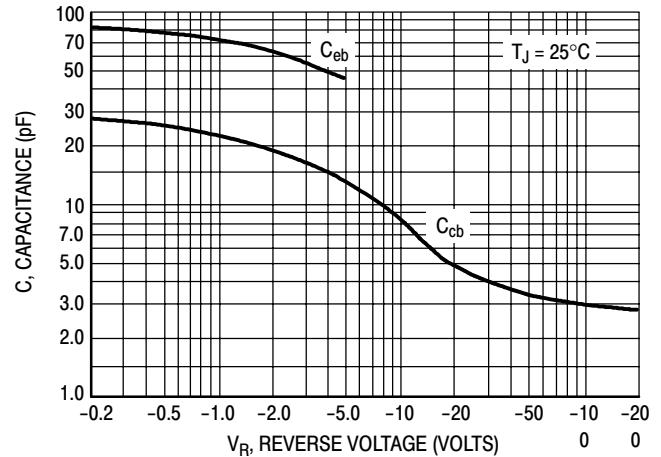
**Figure 8. Temperature Coefficients  
NPN 2N6515, 2N6517**



**Figure 9. Temperature Coefficients  
PNP 2N6520**

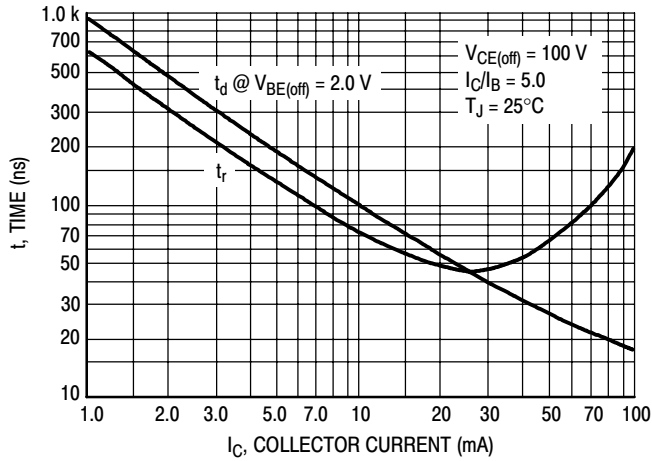


**Figure 10. Capacitance  
NPN 2N6515, 2N6517**

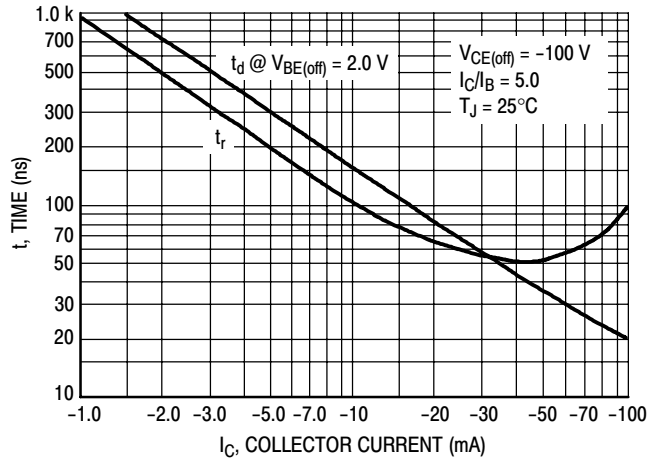


**Figure 11. Capacitance  
PNP 2N6520**

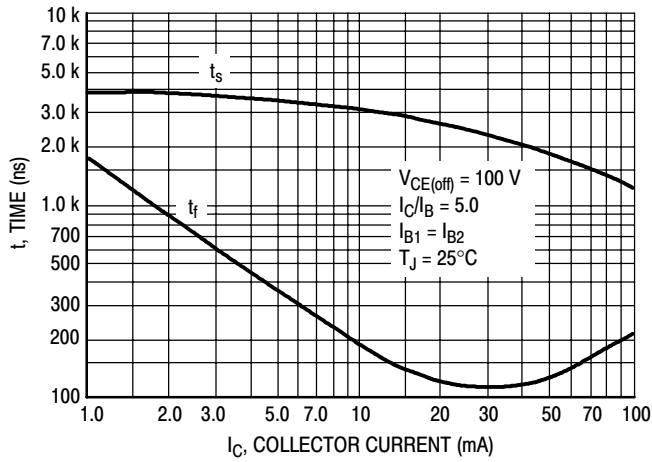
# NPN – 2N6515, 2N6517; PNP – 2N6520



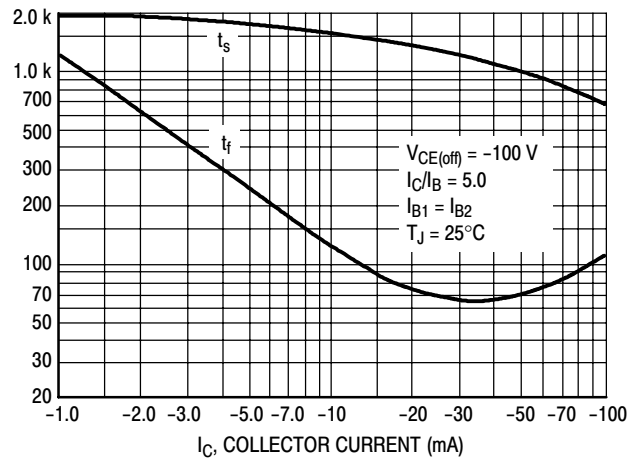
**Figure 12. Turn-On Time**  
NPN 2N6515, 2N6517



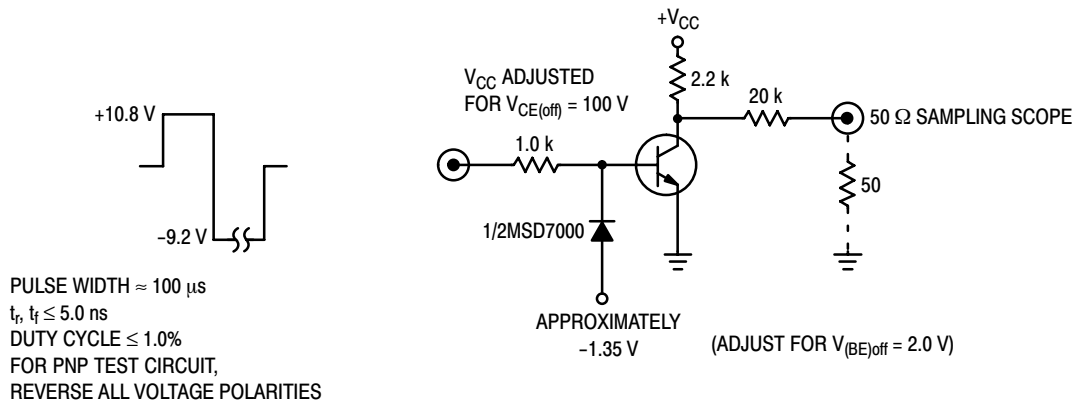
**Figure 13. Turn-On Time**  
PNP 2N6520



**Figure 14. Turn-Off Time**  
NPN 2N6515, 2N6517



**Figure 15. Turn-Off Time**  
PNP 2N6520



**Figure 16. Switching Time Test Circuit**

## NPN – 2N6515, 2N6517; PNP – 2N6520

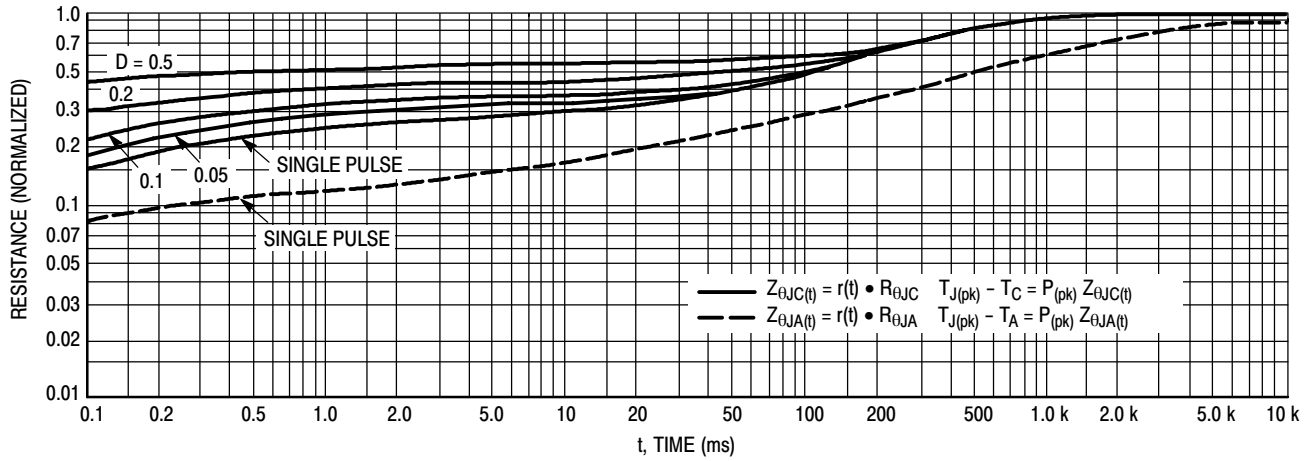


Figure 17. Thermal Response

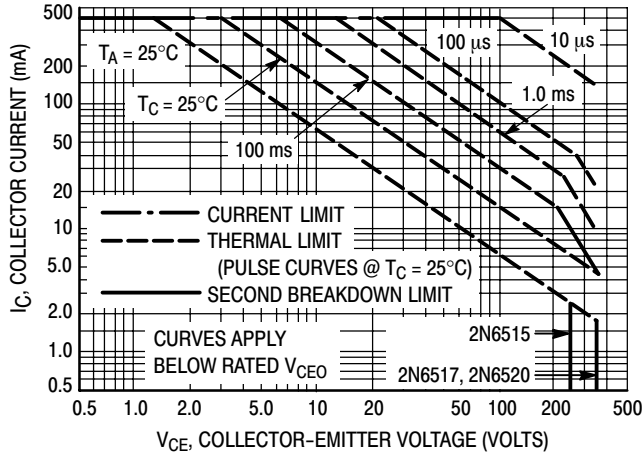
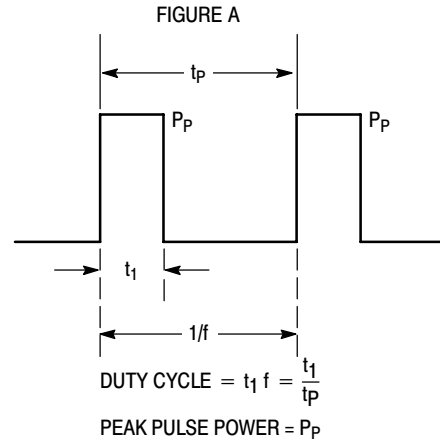


Figure 18. Active Region Safe Operating Area



Design Note: Use of Transient Thermal Resistance Data

### ORDERING INFORMATION

| Device      | Package            | Shipping†        |
|-------------|--------------------|------------------|
| 2N6515RLRMG | TO-92<br>(Pb-Free) | 2000 Ammo Pack   |
| 2N6517G     | TO-92<br>(Pb-Free) | 5000 Unit / Bulk |
| 2N6517RLRPG | TO-92<br>(Pb-Free) | 2000 Ammo Pack   |
| 2N6520RLRAG | TO-92<br>(Pb-Free) | 2000 Tape & Reel |

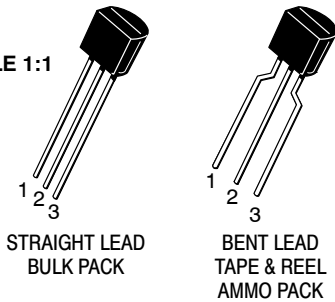
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS

ON Semiconductor®

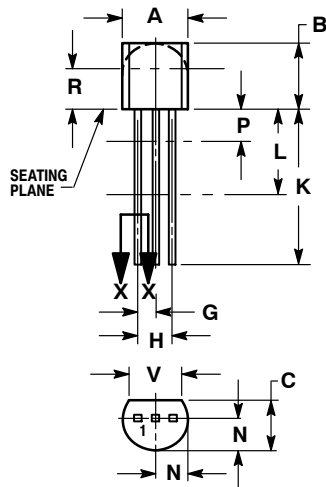
ON

SCALE 1:1

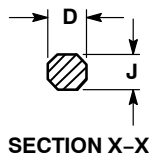


TO-92 (TO-226)  
CASE 29-11  
ISSUE AM

DATE 09 MAR 2007



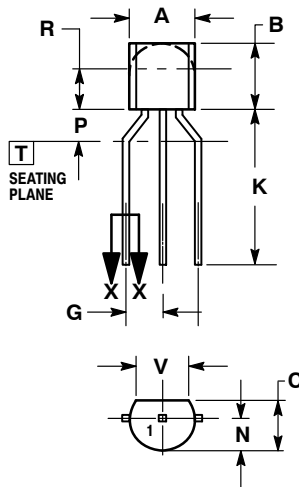
STRAIGHT LEAD  
BULK PACK



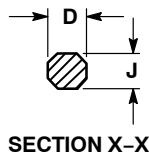
NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| DIM | INCHES |       | MILLIMETERS |       |
|-----|--------|-------|-------------|-------|
|     | MIN    | MAX   | MIN         | MAX   |
| A   | 0.175  | 0.205 | 4.45        | 5.20  |
| B   | 0.170  | 0.210 | 4.32        | 5.33  |
| C   | 0.125  | 0.165 | 3.18        | 4.19  |
| D   | 0.016  | 0.021 | 0.407       | 0.533 |
| G   | 0.045  | 0.055 | 1.15        | 1.39  |
| H   | 0.095  | 0.105 | 2.42        | 2.66  |
| J   | 0.015  | 0.020 | 0.39        | 0.50  |
| K   | 0.500  | ---   | 12.70       | ---   |
| L   | 0.250  | ---   | 6.35        | ---   |
| N   | 0.080  | 0.105 | 2.04        | 2.66  |
| P   | ---    | 0.100 | ---         | 2.54  |
| R   | 0.115  | ---   | 2.93        | ---   |
| V   | 0.135  | ---   | 3.43        | ---   |



BENT LEAD  
TAPE & REEL  
AMMO PACK



NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. CONTOUR OF PACKAGE BEYOND DIMENSION R IS UNCONTROLLED.
4. LEAD DIMENSION IS UNCONTROLLED IN P AND BEYOND DIMENSION K MINIMUM.

| DIM | MILLIMETERS |      |
|-----|-------------|------|
|     | MIN         | MAX  |
| A   | 4.45        | 5.20 |
| B   | 4.32        | 5.33 |
| C   | 3.18        | 4.19 |
| D   | 0.40        | 0.54 |
| G   | 2.40        | 2.80 |
| J   | 0.39        | 0.50 |
| K   | 12.70       | ---  |
| N   | 2.04        | 2.66 |
| P   | 1.50        | 4.00 |
| R   | 2.93        | ---  |
| V   | 3.43        | ---  |

STYLES ON PAGE 2

|                  |                           |  |
|------------------|---------------------------|--|
| DOCUMENT NUMBER: | 98ASB42022B               | Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red. |
| STATUS:          | ON SEMICONDUCTOR STANDARD |  |
| NEW STANDARD:    |                           |  |
| DESCRIPTION:     | TO-92 (TO-226)            |  |
|                  |                           | PAGE 1 OF 3  |

**TO-92 (TO-226)**  
**CASE 29-11**  
**ISSUE AM**


DATE 09 MAR 2007

|   |  |  |   |   |
|---|--|--|---|---|
| STYLE 1:<br>PIN 1. EMITTER<br>2. BASE<br>3. COLLECTOR         | STYLE 2:<br>PIN 1. BASE<br>2. EMITTER<br>3. COLLECTOR                | STYLE 3:<br>PIN 1. ANODE<br>2. ANODE<br>3. CATHODE           | STYLE 4:<br>PIN 1. CATHODE<br>2. CATHODE<br>3. ANODE            | STYLE 5:<br>PIN 1. DRAIN<br>2. SOURCE<br>3. GATE            |
| STYLE 6:<br>PIN 1. GATE<br>2. SOURCE & SUBSTRATE<br>3. DRAIN  | STYLE 7:<br>PIN 1. SOURCE<br>2. DRAIN<br>3. GATE                     | STYLE 8:<br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE & SUBSTRATE | STYLE 9:<br>PIN 1. BASE 1<br>2. EMITTER<br>3. BASE 2            | STYLE 10:<br>PIN 1. CATHODE<br>2. GATE<br>3. ANODE          |
| STYLE 11:<br>PIN 1. ANODE<br>2. CATHODE & ANODE<br>3. CATHODE | STYLE 12:<br>PIN 1. MAIN TERMINAL 1<br>2. GATE<br>3. MAIN TERMINAL 2 | STYLE 13:<br>PIN 1. ANODE 1<br>2. GATE<br>3. CATHODE 2       | STYLE 14:<br>PIN 1. EMITTER<br>2. COLLECTOR<br>3. BASE          | STYLE 15:<br>PIN 1. ANODE 1<br>2. CATHODE<br>3. ANODE 2     |
| STYLE 16:<br>PIN 1. ANODE<br>2. GATE<br>3. CATHODE            | STYLE 17:<br>PIN 1. COLLECTOR<br>2. BASE<br>3. EMITTER               | STYLE 18:<br>PIN 1. ANODE<br>2. CATHODE<br>3. NOT CONNECTED  | STYLE 19:<br>PIN 1. GATE<br>2. ANODE<br>3. CATHODE              | STYLE 20:<br>PIN 1. NOT CONNECTED<br>2. CATHODE<br>3. ANODE |
| STYLE 21:<br>PIN 1. COLLECTOR<br>2. EMITTER<br>3. BASE        | STYLE 22:<br>PIN 1. SOURCE<br>2. GATE<br>3. DRAIN                    | STYLE 23:<br>PIN 1. GATE<br>2. SOURCE<br>3. DRAIN            | STYLE 24:<br>PIN 1. EMITTER<br>2. COLLECTOR/ANODE<br>3. CATHODE | STYLE 25:<br>PIN 1. MT 1<br>2. GATE<br>3. MT 2              |
| STYLE 26:<br>PIN 1. $V_{CC}$<br>2. GROUND 2<br>3. OUTPUT      | STYLE 27:<br>PIN 1. MT<br>2. SUBSTRATE<br>3. MT                      | STYLE 28:<br>PIN 1. CATHODE<br>2. ANODE<br>3. GATE           | STYLE 29:<br>PIN 1. NOT CONNECTED<br>2. ANODE<br>3. CATHODE     | STYLE 30:<br>PIN 1. DRAIN<br>2. GATE<br>3. SOURCE           |
| STYLE 31:<br>PIN 1. GATE<br>2. DRAIN<br>3. SOURCE             | STYLE 32:<br>PIN 1. BASE<br>2. COLLECTOR<br>3. EMITTER               | STYLE 33:<br>PIN 1. RETURN<br>2. INPUT<br>3. OUTPUT          | STYLE 34:<br>PIN 1. INPUT<br>2. GROUND<br>3. LOGIC              | STYLE 35:<br>PIN 1. GATE<br>2. COLLECTOR<br>3. EMITTER      |

|                         |                                  |  |
|-------------------------|----------------------------------|--|
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| <b>STATUS:</b>          | <b>ON SEMICONDUCTOR STANDARD</b> |  |
| <b>NEW STANDARD:</b>    |                                  |  |
| <b>DESCRIPTION:</b>     | <b>TO-92 (TO-226)</b>            | <b>PAGE 2 OF 3</b>   |



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