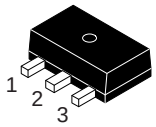
Bipolar Transistor

(−)50 V, (−)4 A, Low VCE(sat), (PNP) NPN Single PCP

2SA2013, 2SC5566



SOT−89 / PCP−1
CASE 419AU

特長

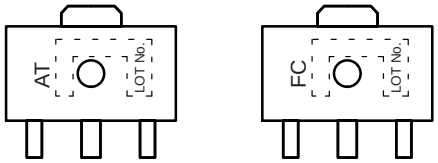
- FBET, MBIT プロセス採用
- コレクタ・エミッタ飽和電圧が低い
- 超小型パッケージのため、セットの小型化，薄型化が可能である
- 許容損失が大きい
- 電流容量が大きい
- スイッチングスピードが速い

用途

- リレードライブ，ランプドライブ，モータドライブ，フラッシュ

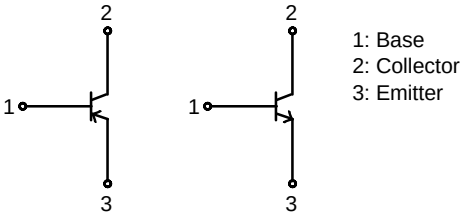
( ) 内は 2SA2013 の場合を示す。

マーキング



2SA2013　　2SC5566

電気的接続図



1: Base
2: Collector
3: Emitter

2SA2013　　2SC5566

絶対最大定格 ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

項目	記号	条件	定格値	Unit
コレクタ・ベース電圧	V_{CBO}		(−50) 100	V
コレクタ・エミッタ電圧	V_{CES}		(−50) 100	V
コレクタ・エミッタ電圧	V_{CEO}		(−)50	V
エミッタ・ベース電圧	V_{EBO}		(−)6	V
コレクタ電流	I_C		(−)4	A
コレクタ電流 (パルス)	I_{CP}		(−)7	A
ベース電流	I_B		(−)600	mA
コレクタ損失	P_C	セラミック基板 (250 mm^2 x 0.8 mm) 装着時	1.3	W
		Tc = 25°C	3.5	W
接合部温度	Tj		150	°C
保存周囲温度	Tstg		−55~+150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
(参考訳)
最大定格を超えるストレスは、デバイスにダメージを与える危険性があります。これらの定格値を超えた場合は、デバイスの機能性を損ない、ダメージが生じ、信頼性に影響を及ぼす危険性があります。

ORDERING INFORMATION

Device	パッケージ名 (JEITA, JEDEC)	最小梱包単位†
2SA2013−TD−E	PCP (Pb−Free)	1000 / Tape & Reel
2SC5566−TD−E		

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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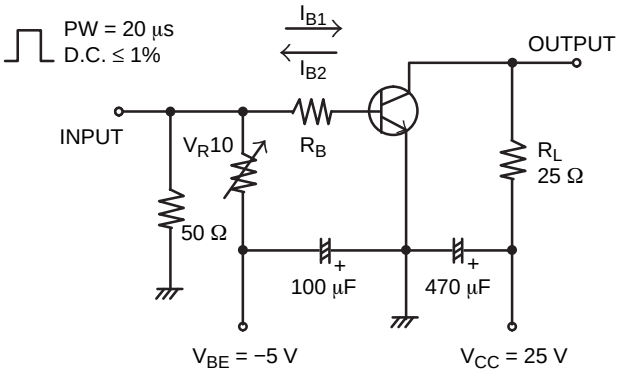
電気的特性 ELECTRICAL CHARACTERISTICS (T_A = 25°C)

項目	記号	条件	定格値			Unit
			Min	Typ	Max	
コレクタしゃ断電流	I_{CBO}	V_{CB} = (−)40 V, I_E = 0 A	−	−	(−)1	μA
エミッタしゃ断電流	I_{EBO}	V_{EB} = (−)4 V, I_C = 0 A	−	−	(−)1	μA
直流電流増幅率	h_{FE}	V_{CE} = (−)2 V, I_C = (−)500 mA	200	−	560	
利得帯域幅積	f_T	V_{CE} = (−)10 V, I_C = (−)500 mA	−	(360) 400	−	MHz
出力容量	Cob	V_{CB} = (−)10 V, f = 1 MHz	−	(24) 15	−	pF
コレクタ・エミッタ飽和電圧	V_{CE}(sat)1	I_C = (−)1 A, I_B = (−)50 mA	−	(−105) 85	(−180) 130	mV
	V_{CE}(sat)2	I_C = (−)2 A, I_B = (−)100 mA	−	(−200) 150	(−340) 225	mV
ベース・エミッタ飽和電圧	V_{BE}(sat)	I_C = (−)2 A, I_B= (−)100 mA	−	(−) 0.89	(−)1.2	V
コレクタ・ベース降伏電圧	$V_{(BR)CBO}$	I_C = (−)10 μA, I_E = 0 A	(−50) 100	−	−	V
コレクタ・エミッタ降伏電圧	$V_{(BR)CES}$	I_C = (−)100 μA, R_{BE} = 0 Ω	(−50) 100	−	−	V
コレクタ・エミッタ降伏電圧	$V_{(BR)CEO}$	I_C = (−)1 mA, R_{BE} = ∞	(−)50	−	−	V
エミッタ・ベース降伏電圧	$V_{(BR)EBO}$	I_E = (−)10 μA, I_C = 0 A	(−)6	−	−	V
ターンオン時間	t_{on}	指定回路において	−	(30) 35	−	ns
蓄積時間	t_{stg}		−	(230) 300	−	ns
下降時間	t_f		−	(15) 20	−	ns

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
(参考訳)
製品パラメータは、特別な記述が無い限り、記載されたテスト条件に対する電気的特性で示しています。異なる条件下で製品動作を行った時には、電気的特性で示している特性を得られない場合があります。

スイッチングタイム測定回路図



I_C = 10I_{B1} = −10I_{B2} = 1 A
PNP の場合極性逆

図 1. スイッチングタイム測定回路図

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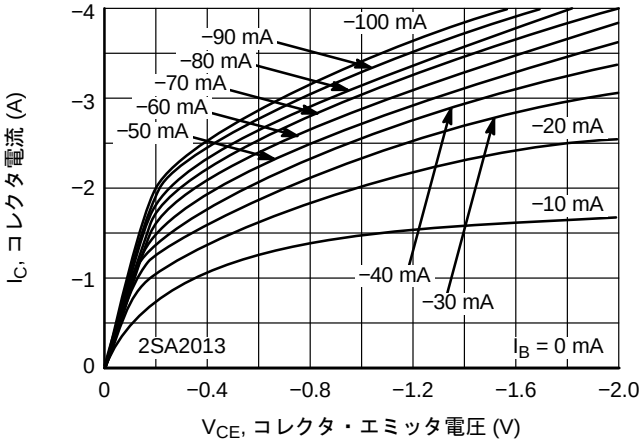

図 2. $I_C - V_{CE}$

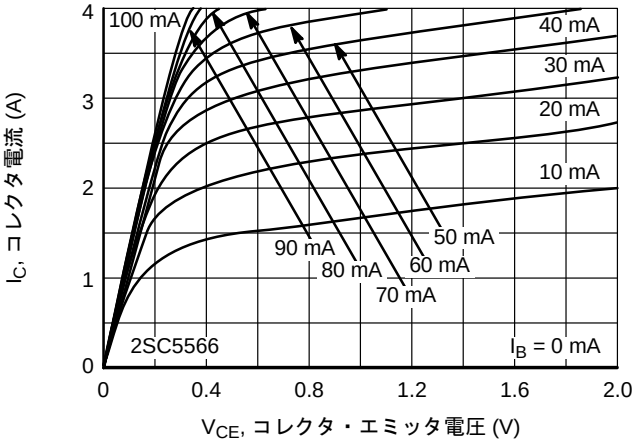

図 3. $I_C - V_{CE}$

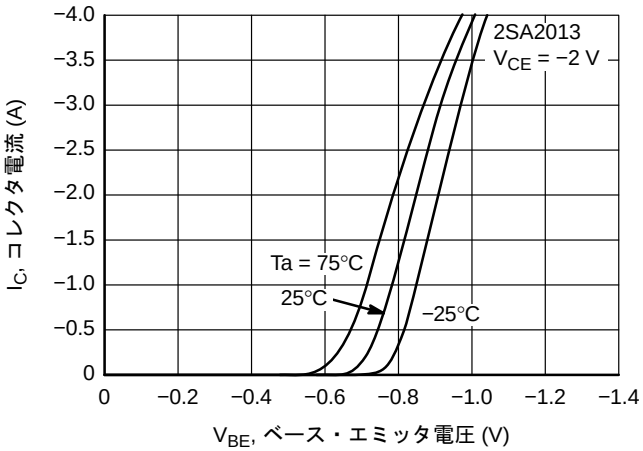

図 4. $I_C - V_{BE}$

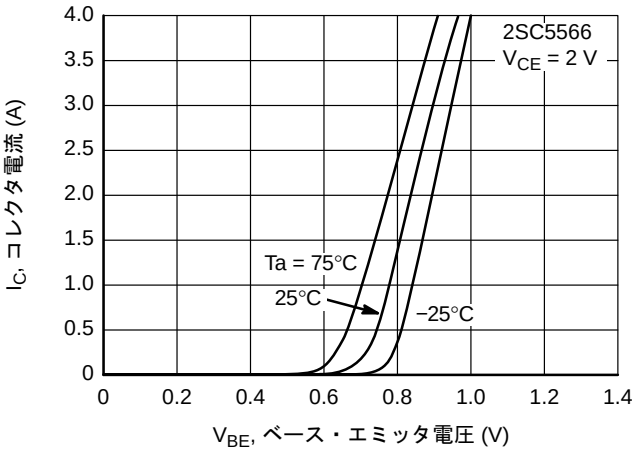

図 5. $I_C - V_{BE}$

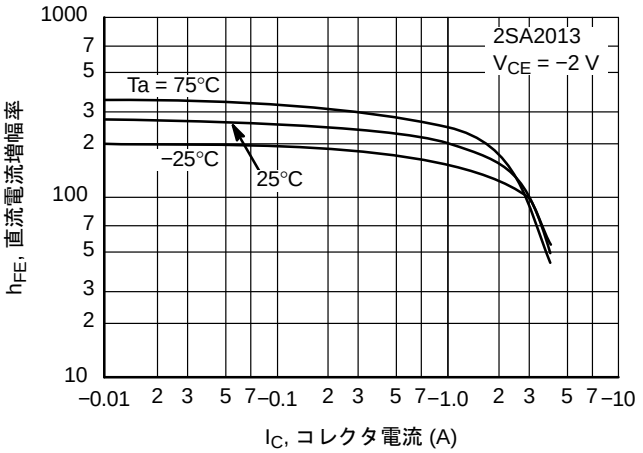

図 6. $h_{FE} - I_C$

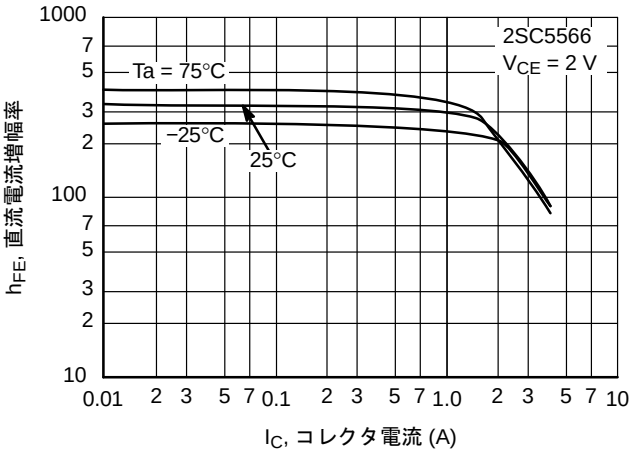

図 7. $h_{FE} - I_C$

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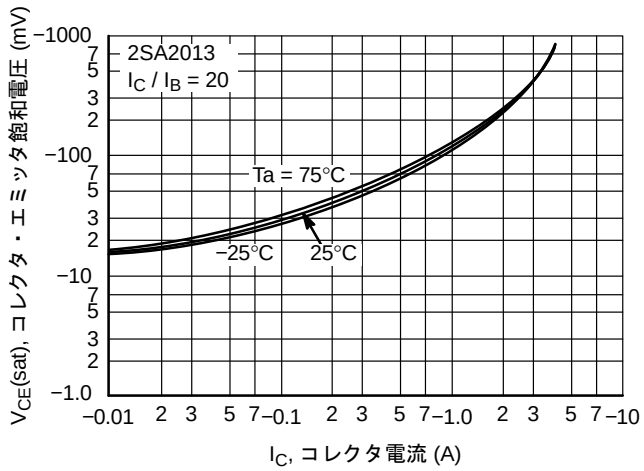

図 8. $V_{CE}(sat) - I_C$

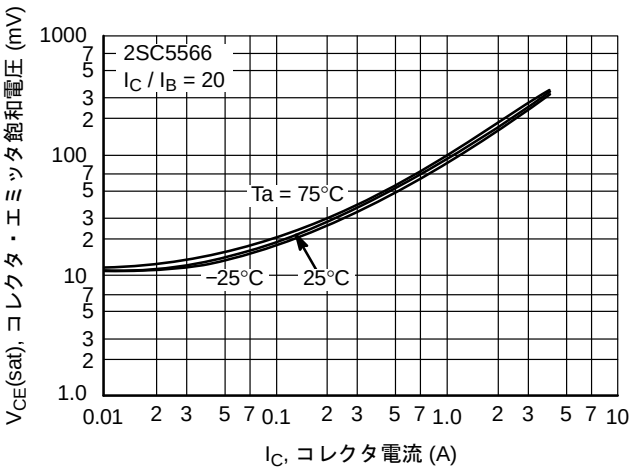

図 9. $V_{CE}(sat) - I_C$

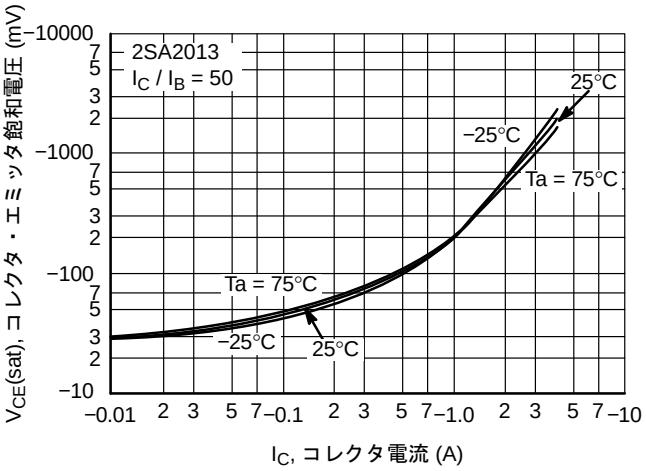

図 10. $V_{CE}(sat) - I_C$

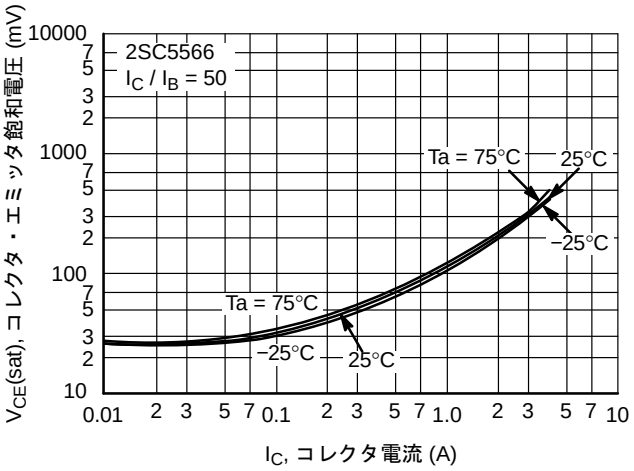

図 11. $V_{CE}(sat) - I_C$

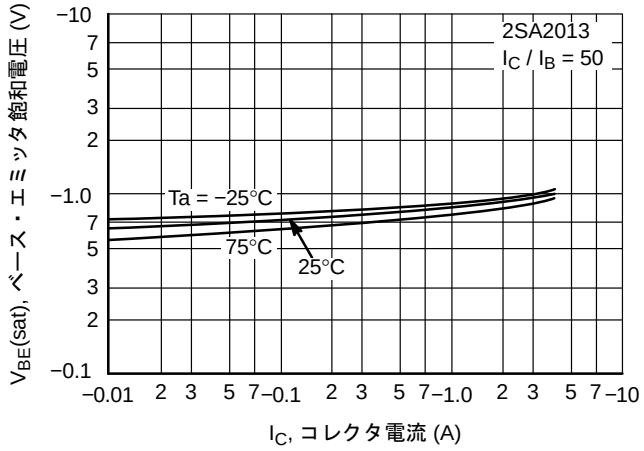

図 12. $V_{BE}(sat) - I_C$

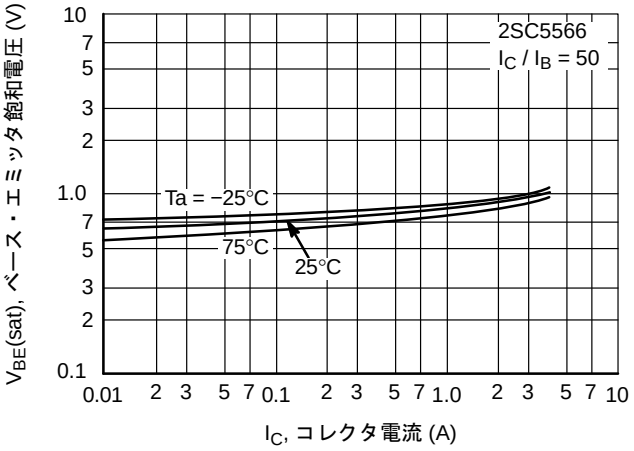

図 13. $V_{BE}(sat) - I_C$

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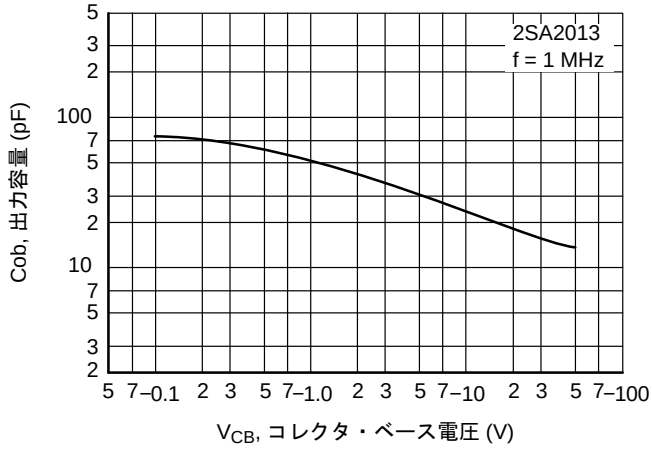

図 14. **Cob − V_{CB}**

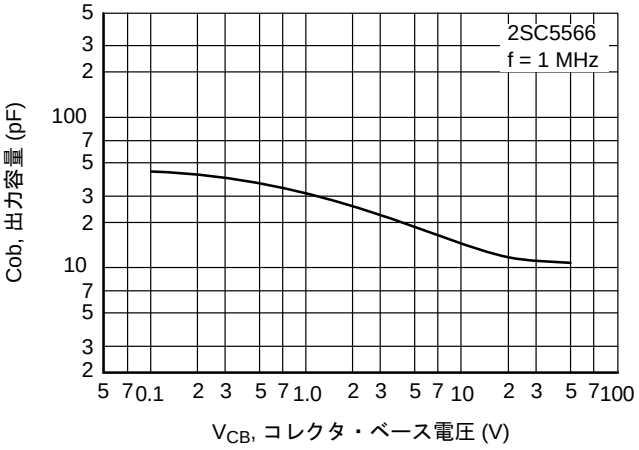

図 15. **Cob − V_{CB}**

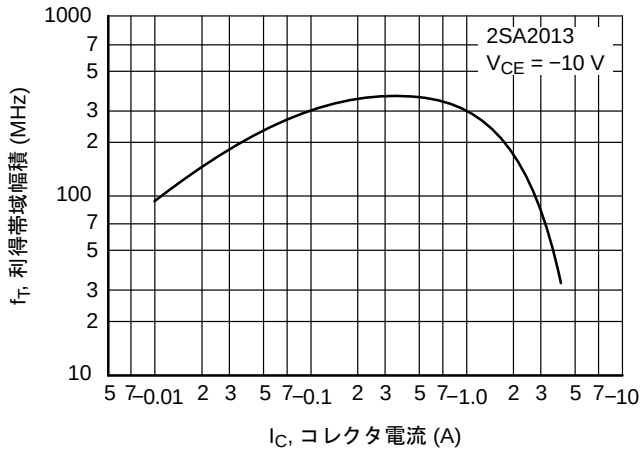

図 16. **f_T − I_C**

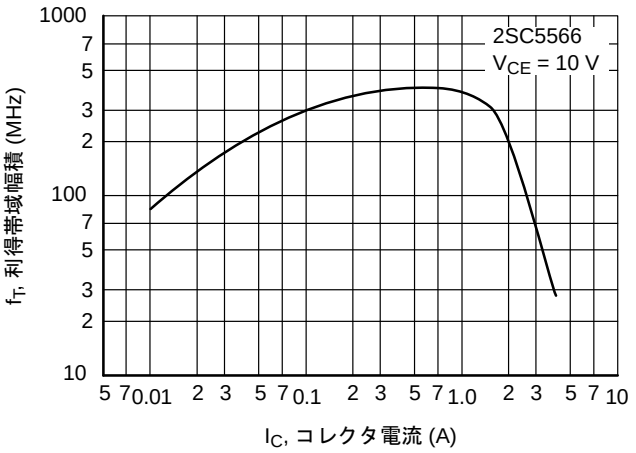

図 17. **f_T − I_C**

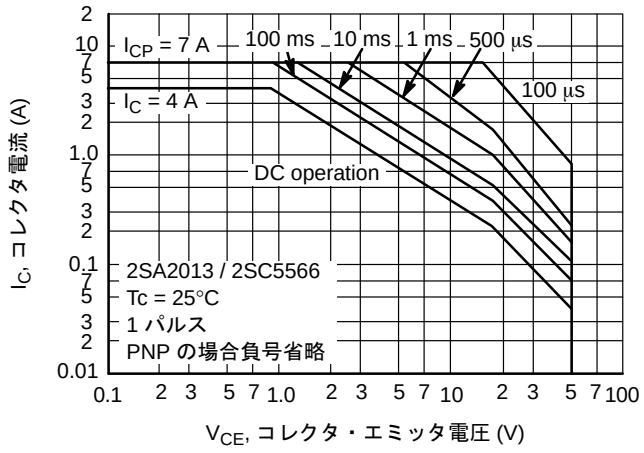

図 18. **ASO**

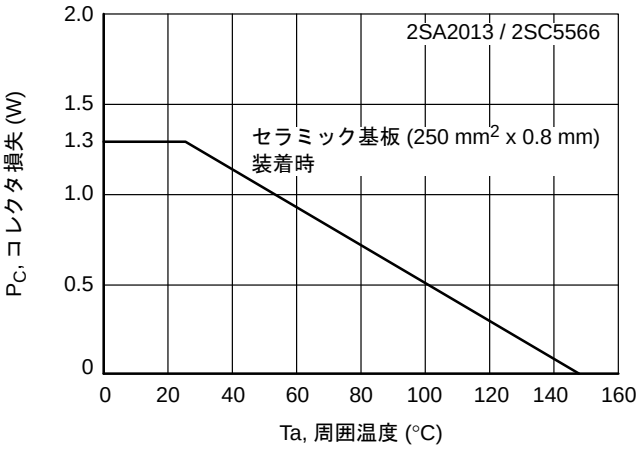

図 19. **P_C − Ta**

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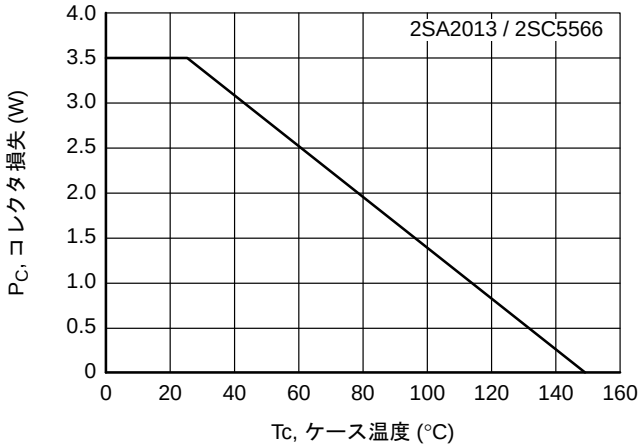

図 20. P_C − Tc

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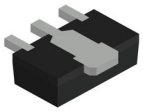

SOT−89−3 4.50x2.50x1.50 1.50P
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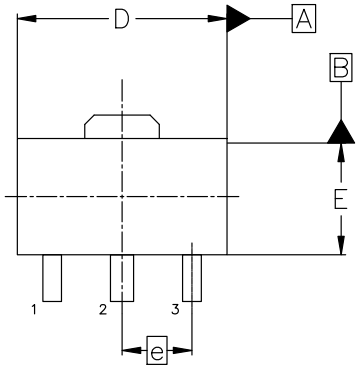
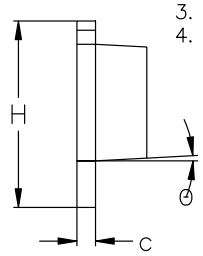
ISSUE B

DATE 06 NOV 2026



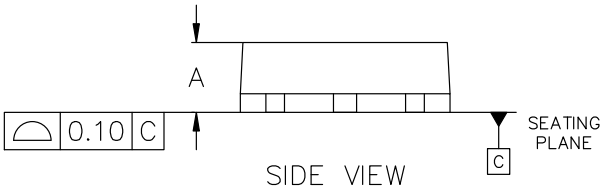
TOP VIEW



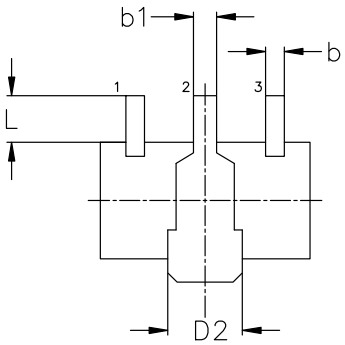
END VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

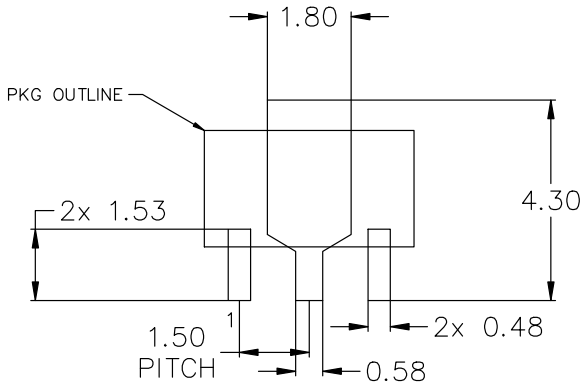
MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.40	1.50	1.60
b	0.35	0.40	0.48
b1	0.40	0.50	0.55
c	0.37	0.40	0.43
D	4.40	4.50	4.60
D2	1.40	1.60	1.80
E	2.40	2.50	2.60
e	1.50 BSC		
H	3.80	4.00	4.20
L	0.80	1.00	1.20
θ	0°	−−−	3°



SIDE VIEW



BOTTOM VIEW



RECOMMENDED MOUNTING FOOTPRINT

*For additional information on our Pb−Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**SOT−89−3 4.50x2.50x1.50 1.50P**		**PAGE 1 OF 1**

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