

# Quad 2-Input Multiplexer

## 74VHC157

The VHC157 is an advanced high speed CMOS Quad 2-Channel Multiplexer fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

It consists of four 2-input digital multiplexers with common select and enable inputs. When the  $\overline{\text{ENABLE}}$  input is held "H" level, selection of data is inhibited and all the outputs become "L" level. The SELECT decoding determines whether the I 0x or I 1x inputs get routed to their corresponding outputs.

An Input protection circuit ensures that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5 V to 3 V systems and on two supply systems such as battery back up. This circuit prevents device destruction due to mismatched supply and input voltages.

### Features

- High Speed:  $t_{PD} = 4.1 \text{ ns}$  (Typ.) at  $V_{CC} = 5 \text{ V}$
- Low Power Dissipation:  $I_{CC} = 4 \mu\text{A}$  (Max.) at  $T_A = 25^\circ\text{C}$
- High Noise Immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (Min.)
- Power Down Protection is Provided On All Inputs
- Low Noise:  $V_{OLP} = 0.8 \text{ V}$  (Max.)
- Pin and Function Compatible with 74HC157

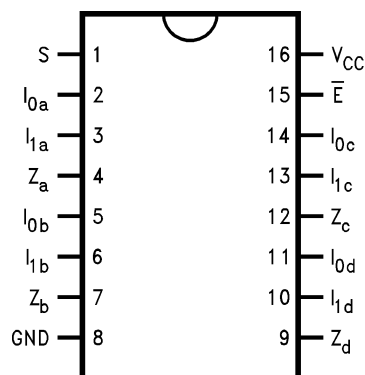


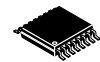
Figure 1. Connection Diagram

### PIN DESCRIPTION

Pin Names	Description
$I_{0a}-I_{0d}$	Source 0 Data Inputs
$I_{1a}-I_{1d}$	Source 1 Data Inputs
$\overline{\text{E}}$	Enable Input
S	Select Input
$Z_a-Z_d$	Outputs



SOIC-16  
D SUFFIX  
CASE 751B

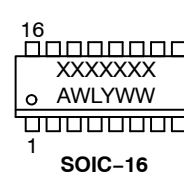


TSSOP-16  
DT SUFFIX  
CASE 948F

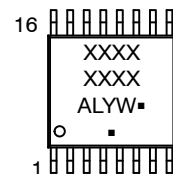


QFN16  
MN SUFFIX  
CASE 485AW

### MARKING DIAGRAMS



SOIC-16



TSSOP-16



QFN16\*

XXXXXXX = Specific Device Code  
A = Assembly Location  
WL, L = Wafer Lot  
YY, Y = Year  
WW, W = Work Week  
G, ■ = Pb-Free Package

(Note: Microdot may be in either location)

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 6 of this data sheet.

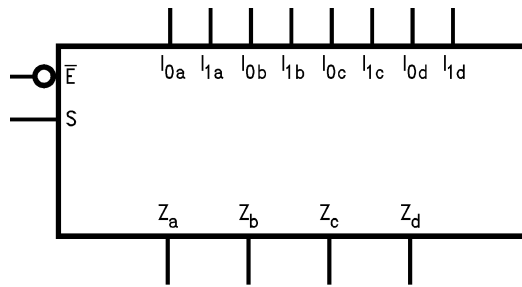
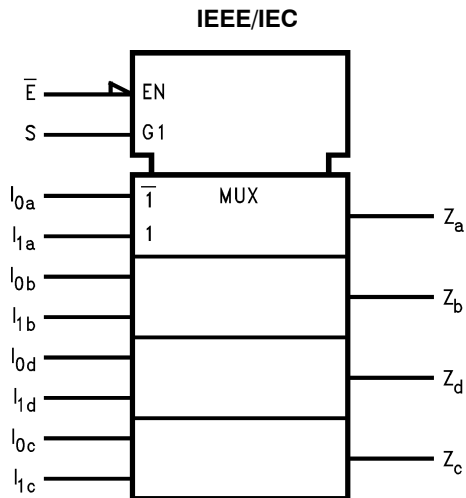


Figure 2. Logic Symbol



TRUTH TABLE

Inputs				Outputs
E	S	I <sub>0</sub>	I <sub>1</sub>	Z
H	X	X	X	L
L	H	X	L	L
L	H	X	H	H
L	L	L	X	L
L	L	H	X	H

H = HIGH Voltage Level

L = LOW Voltage Level

X = Immaterial

## FUNCTIONAL DESCRIPTION

The VHC157 is a quad 2-input multiplexer. It selects four bits of data from two sources under the control of a common Select input (S). The Enable input ( $\bar{E}$ ) is active- LOW. When  $\bar{E}$  is HIGH, all of the outputs (Z) are forced LOW regardless of all other inputs. The VHC157 is the logic implementation of a 4-pole, 2-position switch where the position of the switch is determined by the logic levels supplied to the Select input. The logic equations for the outputs are shown below:

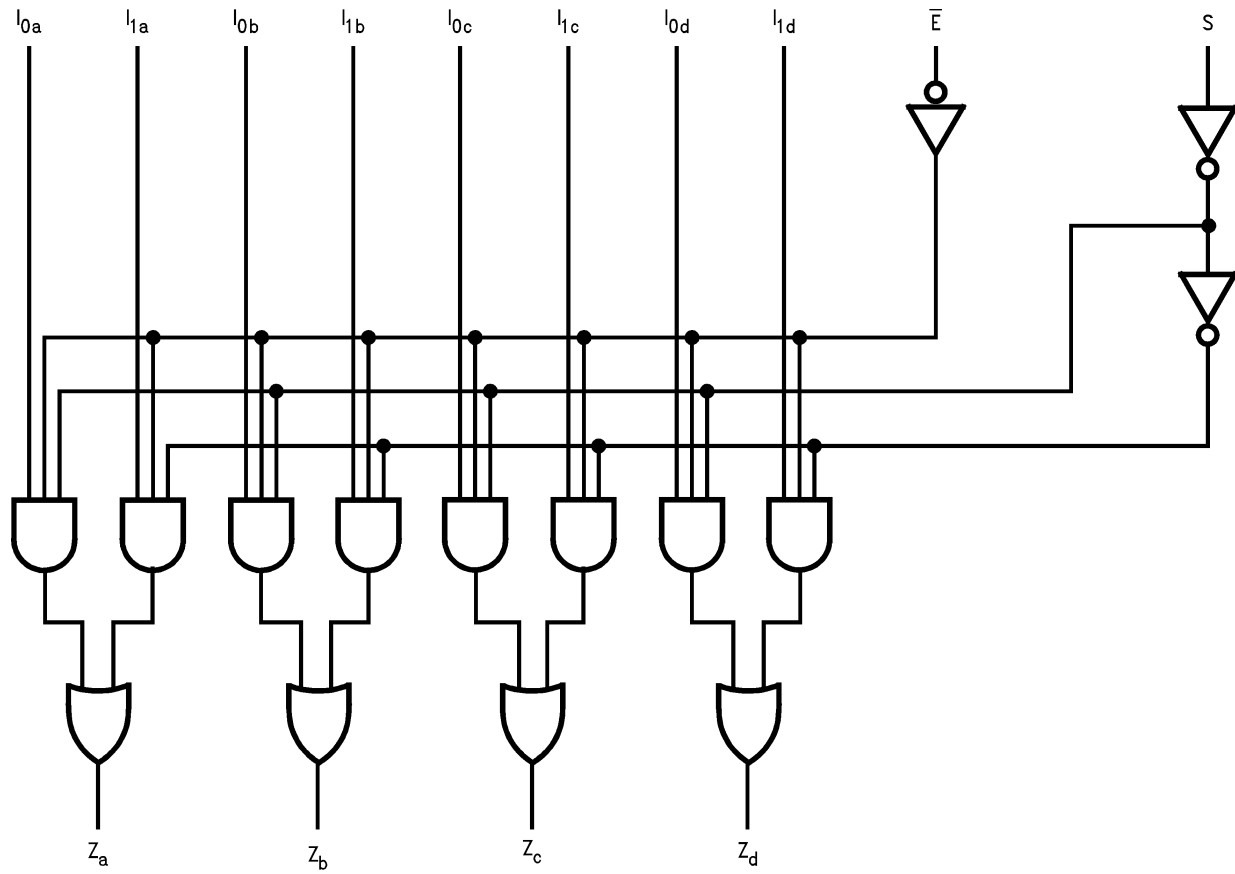
$$Z_a = \bar{E} \cdot (I_{1a} \cdot S + I_{0a} \cdot \bar{S})$$

$$Z_b = \bar{E} \cdot (I_{1b} \cdot S + I_{0b} \cdot \bar{S})$$

$$Z_c = \bar{E} \cdot (I_{1c} \cdot S + I_{0c} \cdot \bar{S})$$

$$Z_d = \bar{E} \cdot (I_{1d} \cdot S + I_{0d} \cdot \bar{S})$$

A common use of the VHC157 is the moving of data from two groups of registers to four common output busses. The particular register from which the data comes is determined by the state of the Select input. A less obvious use is as a function generator. The VHC157 can generate any four of the sixteen different functions of two variables with one variable common. This is useful for implementing gating functions.

**Logic Diagram**

Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V <sub>CC</sub>	DC Supply Voltage	–0.5 to +6.5	V
V <sub>IN</sub>	DC Input Voltage	–0.5 to +6.5	V
V <sub>OUT</sub>	DC Output Voltage	–0.5 to V <sub>CC</sub> +0.5	V
I <sub>IN</sub>	DC Input Current, per Pin	±20	mA
I <sub>OUT</sub>	DC Output Current, per Pin	±25	mA
I <sub>CC</sub>	DC Supply Current, V <sub>CC</sub> and GND Pins	±50	mA
I <sub>IK</sub>	Input Clamp Current	–20	mA
I <sub>OK</sub>	Output Clamp Current	±20	mA
T <sub>STG</sub>	Storage Temperature Range	–65 to +150	°C
T <sub>L</sub>	Lead Temperature, 1 mm from Case for 10 secs	260	°C
T <sub>J</sub>	Junction Temperature Under Bias	+150	°C
θ <sub>JA</sub>	Thermal Resistance (Note 2) <div>SOIC–16126 QFN16118 TSSOP–16159</div>		°C/W
P <sub>D</sub>	Power Dissipation in Still Air at 25°C <div>SOIC–16995 QFN161062 TSSOP–16787</div>		mW
MSL	Moisture Sensitivity	Level 1	–
F <sub>R</sub>	Flammability Rating Oxygen Index: 28 to 34	UL 94 V–0 @ 0.139 in	–
V <sub>ESD</sub>	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri–stated.
2. Measured with minimum pad spacing on an FR4 board, using 76mm–by–114mm, 2–ounce copper trace no air flow per JESD51–7.
3. HBM tested to EIA / JESD22–A114–A. CDM tested to JESD22–C101–A. JEDEC recommends that ESD qualification to EIA/JESD22–A115A (Machine Model) be discontinued.

## RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V <sub>CC</sub>	DC Supply Voltage	2.0	5.5	V
V <sub>IN</sub>	DC Input Voltage (Note 4 )	0	5.5	V
V <sub>OUT</sub>	DC Output Voltage (Note 4 )	0	V <sub>CC</sub>	V
T <sub>A</sub>	Operating Temperature	–40	+85	°C
t <sub>r</sub> , t <sub>f</sub>	Input Rise or Fall Rate	V <sub>CC</sub> = 3.0 V to 3.6 V V <sub>CC</sub> = 4.5 V to 55 V	0 100 20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V<sub>CC</sub>). Unused outputs must be left open.

## DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
V <sub>IH</sub>	HIGH Level Input Voltage		2.0 3.0 – 5.5	1.50 0.7 × V <sub>CC</sub>			1.50 0.7 × V <sub>CC</sub>		V
V <sub>IL</sub>	LOW Level Input Voltage		2.0 3.0 – 5.5			0.50 0.3 × V <sub>CC</sub>		0.50 0.3 × V <sub>CC</sub>	V
V <sub>OH</sub>	HIGH Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OH</sub> = -50 µA	2.0 3.0 4.5	1.9 2.9 4.4	2.0 3.0 4.5	1.9 2.9 4.4		V
			I <sub>OH</sub> = -4 mA I <sub>OH</sub> = -8 mA	3.0 4.5	2.58 3.94		2.48 3.80		
V <sub>OL</sub>	LOW Level Output Voltage	V <sub>IN</sub> = V <sub>IH</sub> or V <sub>IL</sub>	I <sub>OL</sub> = 50 µA	2.0 3.0 4.5	0.0 0.0 0.0	0.1 0.1 0.1		0.1 0.1 0.1	V
			I <sub>OH</sub> = 4 mA I <sub>OH</sub> = 8 mA	3.0 4.5		0.36 0.36		0.44 0.44	
I <sub>IN</sub>	Input Leakage Current	V <sub>IN</sub> = 5.5 V or GND	0 – 5.5			± 0.1		± 1.0	µA
I <sub>CC</sub>	Quiescent Supply Current	V <sub>IN</sub> = V <sub>CC</sub> or GND	5.5			4.0		40.0	µA

## NOISE CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C		Unit
				Typ	Limits	
V <sub>OLP</sub>	Quiet Output Maximum Dynamic V <sub>OL</sub> (Note 3 )	CL = 50 pF	5.0	0.3	0.8	V
V <sub>OLV</sub>	Quiet Output Minimum Dynamic V <sub>OL</sub> (Note 3 )	CL = 50 pF	5.0	- 0.3	- 0.8	V
V <sub>IHD</sub>	Minimum HIGH Level Dynamic Input Voltage (Note 3 )	CL = 50 pF	5.0		3.5	V
V <sub>ILD</sub>	Maximum LOW Level Dynamic Input Voltage (Note 3 )	CL = 50 pF	5.0		1.5	V

5. Parameter guaranteed by design.

## AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, I <sub>n</sub> to Z <sub>n</sub>	C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	3.3 ± 0.3		6.2 8.7	9.7 13.2	1.0 1.0	11.5 15.0	ns
		C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	5.0 ± 0.5		4.1 5.6	6.4 8.4	1.0 1.0	7.5 9.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, S to Z <sub>n</sub>	C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	3.3 ± 0.3		8.4 10.9	13.2 16.7	1.0 1.0	15.5 19.0	ns
		C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	5.0 ± 0.5		5.3 6.8	8.1 10.1	1.0 1.0	9.5 11.5	
t <sub>PLH</sub> , t <sub>PHL</sub>	Propagation Delay, E to Z <sub>n</sub>	C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	3.3 ± 0.3		8.7 11.2	13.6 17.1	1.0 1.0	16.0 19.5	ns
		C <sub>L</sub> = 15pF C <sub>L</sub> = 50pF	5.0 ± 0.5		5.6 7.1	8.6 10.6	1.0 1.0	10.0 12.0	

## 74VHC157

### AC ELECTRICAL CHARACTERISTICS (continued)

Symbol	Parameter	Conditions	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Unit
				Min	Typ	Max	Min	Max	
C <sub>IN</sub>	Input Capacitance	V <sub>CC</sub> = Open			4	10	–	10	pF
C <sub>PD</sub>	Power Dissipation Capacitance	(Note 3)			20	–	–	–	pF

6. C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation:  $I_{CC(OPR)} = C_{PD} \cdot V_{CC} \cdot f_{in} + I_{CC}$ .

### ORDERING INFORMATION

Device	Marking	Package	Shipping <sup>†</sup>
74VHC157MX	VHC157	SOIC-16	2500 / Tape & Reel
74VHC157MTCX	VHC157	TSSOP-16	2500 / Tape & Reel

<sup>†</sup>For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

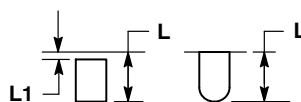
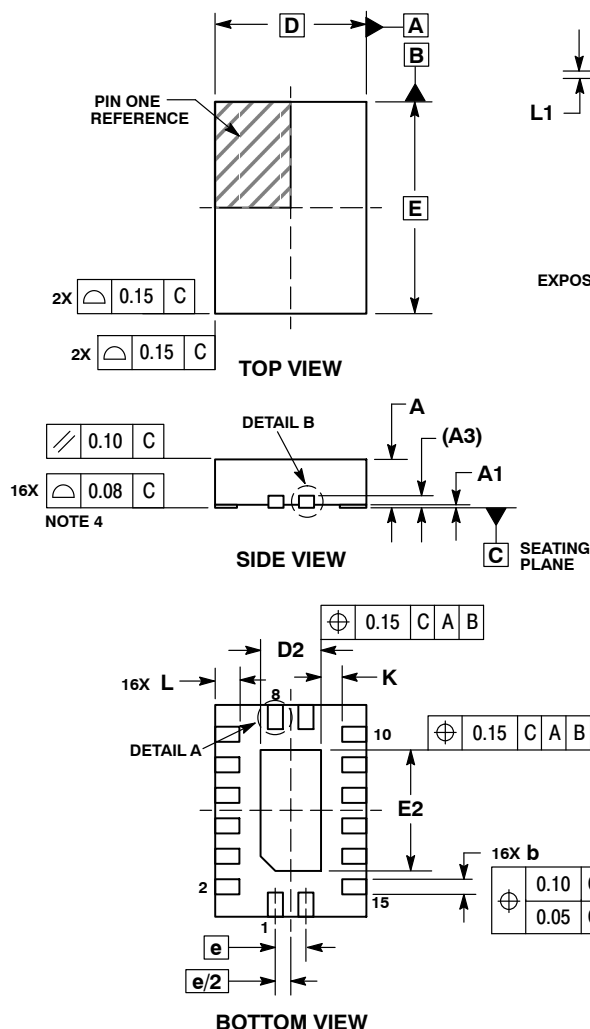
# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



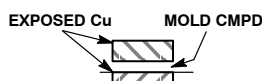
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**QFN16, 2.5x3.5, 0.5P**  
CASE 485AW  
ISSUE O

DATE 11 DEC 2008



**DETAIL A**  
ALTERNATE TERMINAL  
CONSTRUCTIONS



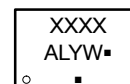
**DETAIL B**  
ALTERNATE  
CONSTRUCTIONS

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSIONS b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20 REF	
b	0.20	0.30
D	2.50 BSC	
D2	0.85	1.15
E	3.50 BSC	
E2	1.85	2.15
e	0.50 BSC	
K	0.20	---
L	0.35	0.45
L1	---	0.15

## GENERIC MARKING DIAGRAM\*

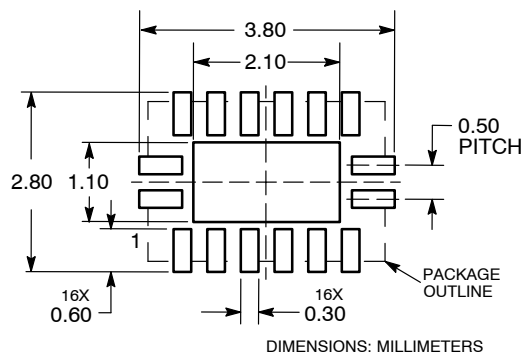


XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Package

(Note: Microdot may be in either location)

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

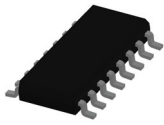
## RECOMMENDED SOLDERING FOOTPRINT\*



\*For additional information on our Pb-Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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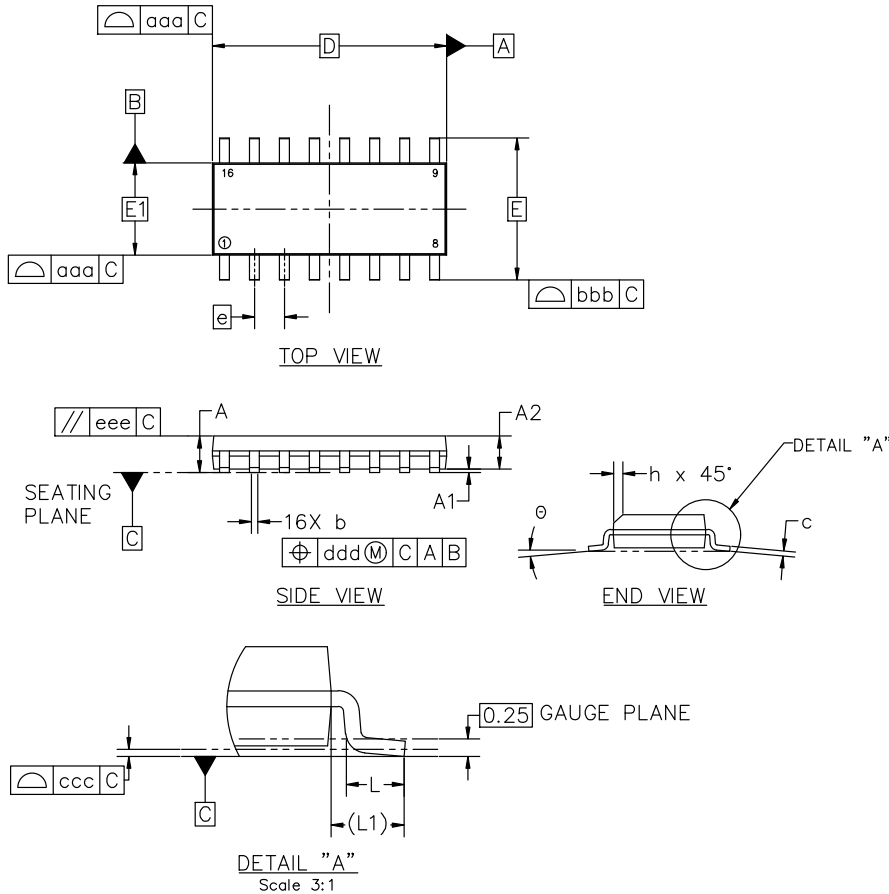
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**SOIC-16 9.90x3.90x1.37 1.27P**  
**CASE 751B**  
**ISSUE M**

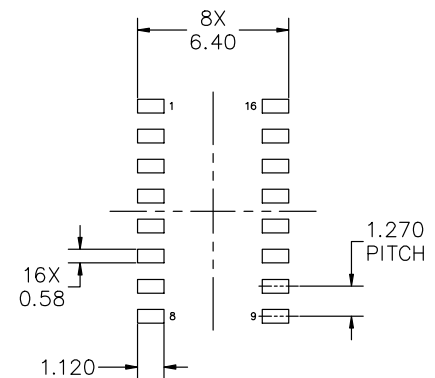
DATE 18 OCT 2024

## NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
2. DIMENSION IN MILLIMETERS. ANGLE IN DEGREES.
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15mm PER SIDE.
5. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127mm TOTAL IN EXCESS OF THE b DIMENSION AT MAXIMUM MATERIAL CONDITION.



MILLIMETERS			
DIM	MIN	NOM	MAX
A	1.35	1.55	1.75
A1	0.10	0.18	0.25
A2	1.25	1.37	1.50
b	0.35	0.42	0.49
c	0.19	0.22	0.25
D	9.90 BSC		
E	6.00 BSC		
E1	3.90 BSC		
e	1.27 BSC		
h	0.25	---	0.50
L	0.40	0.83	1.25
L1	1.05 REF		
θ	0°	---	7°
TOLERANCE OF FORM AND POSITION			
aaa	0.10		
bbb	0.20		
ccc	0.10		
ddd	0.25		
eee	0.10		



\*FOR ADDITIONAL INFORMATION ON OUR  
PB-FREE STRATEGY AND SOLDERING DETAILS,  
PLEASE DOWNLOAD THE onsemi SOLDERING  
AND MOUNTING TECHNIQUES REFERENCE  
MANUAL, SOLDERM/D

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<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 1 OF 2</b>

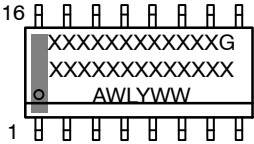
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SOIC-16 9.90x3.90x1.37 1.27P  
CASE 751B  
ISSUE M

DATE 18 OCT 2024

GENERIC  
MARKING DIAGRAM\*

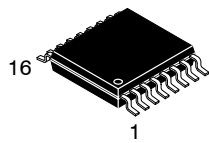


XXXXX = Specific Device Code  
A = Assembly Location  
WL = Wafer Lot  
Y = Year  
WW = Work Week  
G = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

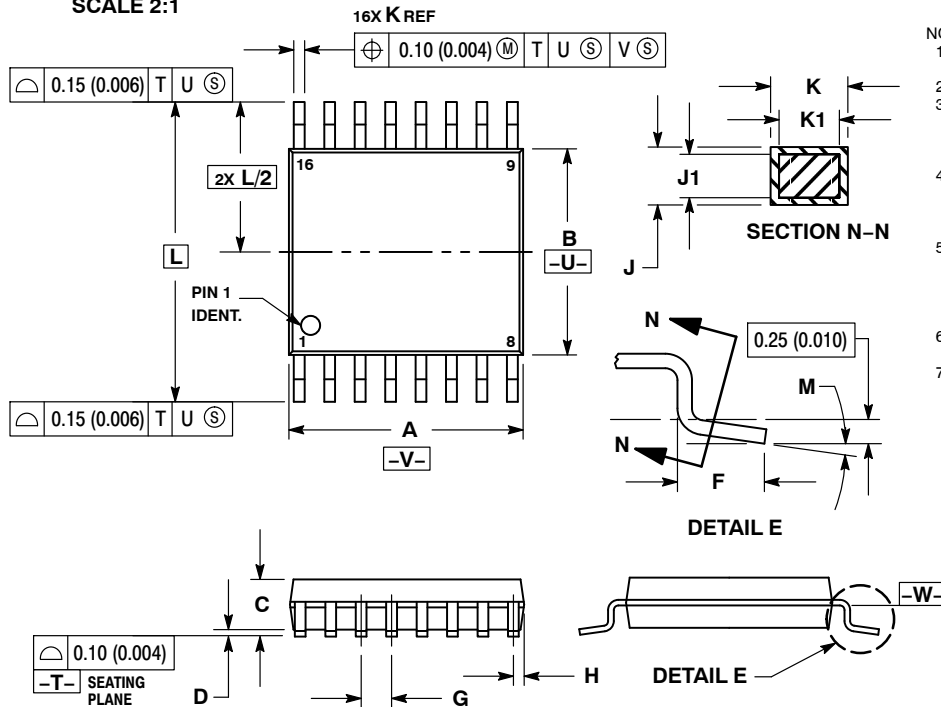
<b>STYLE 1:</b> PIN 1. COLLECTOR 2. BASE 3. EMITTER 4. NO CONNECTION 5. EMITTER 6. BASE 7. COLLECTOR 8. COLLECTOR 9. BASE 10. EMITTER 11. NO CONNECTION 12. EMITTER 13. BASE 14. COLLECTOR 15. EMITTER 16. COLLECTOR	<b>STYLE 2:</b> PIN 1. CATHODE 2. ANODE 3. NO CONNECTION 4. CATHODE 5. CATHODE 6. NO CONNECTION 7. ANODE 8. CATHODE 9. CATHODE 10. ANODE 11. NO CONNECTION 12. CATHODE 13. CATHODE 14. NO CONNECTION 15. ANODE 16. CATHODE	<b>STYLE 3:</b> PIN 1. COLLECTOR, DYE #1 2. BASE, #1 3. EMITTER, #1 4. COLLECTOR, #1 5. COLLECTOR, #2 6. BASE, #2 7. EMITTER, #2 8. COLLECTOR, #2 9. COLLECTOR, #3 10. BASE, #3 11. EMITTER, #3 12. COLLECTOR, #3 13. COLLECTOR, #4 14. BASE, #4 15. EMITTER, #4 16. COLLECTOR, #4	<b>STYLE 4:</b> PIN 1. COLLECTOR, DYE #1 2. COLLECTOR, #1 3. COLLECTOR, #2 4. COLLECTOR, #2 5. COLLECTOR, #3 6. COLLECTOR, #3 7. COLLECTOR, #4 8. COLLECTOR, #4 9. BASE, #4 10. EMITTER, #4 11. BASE, #3 12. EMITTER, #3 13. BASE, #2 14. EMITTER, #2 15. BASE, #1 16. EMITTER, #1
<b>STYLE 5:</b> PIN 1. DRAIN, DYE #1 2. DRAIN, #1 3. DRAIN, #2 4. DRAIN, #2 5. DRAIN, #3 6. DRAIN, #3 7. DRAIN, #4 8. DRAIN, #4 9. GATE, #4 10. SOURCE, #4 11. GATE, #3 12. SOURCE, #3 13. GATE, #2 14. SOURCE, #2 15. GATE, #1 16. SOURCE, #1	<b>STYLE 6:</b> PIN 1. CATHODE 2. CATHODE 3. CATHODE 4. CATHODE 5. CATHODE 6. CATHODE 7. CATHODE 8. CATHODE 9. ANODE 10. ANODE 11. ANODE 12. ANODE 13. ANODE 14. ANODE 15. ANODE 16. ANODE	<b>STYLE 7:</b> PIN 1. SOURCE N-CH 2. COMMON DRAIN (OUTPUT) 3. COMMON DRAIN (OUTPUT) 4. GATE P-CH 5. COMMON DRAIN (OUTPUT) 6. COMMON DRAIN (OUTPUT) 7. COMMON DRAIN (OUTPUT) 8. SOURCE P-CH 9. SOURCE P-CH 10. COMMON DRAIN (OUTPUT) 11. COMMON DRAIN (OUTPUT) 12. COMMON DRAIN (OUTPUT) 13. GATE N-CH 14. COMMON DRAIN (OUTPUT) 15. COMMON DRAIN (OUTPUT) 16. SOURCE N-CH	

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<b>DESCRIPTION:</b>	<b>SOIC-16 9.90X3.90X1.37 1.27P</b>	<b>PAGE 2 OF 2</b>
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TSSOP-16 WB  
CASE 948F  
ISSUE B

DATE 19 OCT 2006

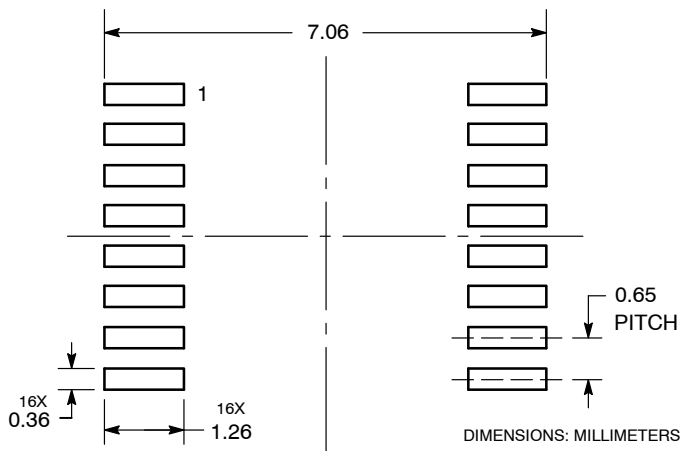


NOTES:

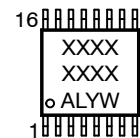
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE -W-.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	---	1.20	---	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.18	0.28	0.007	0.011
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0°	8°	0°	8°

RECOMMENDED  
SOLDERING FOOTPRINT\*



GENERIC  
MARKING DIAGRAM\*



XXXX = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
G or ■ = Pb-Free Package

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

\*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	TSSOP-16	PAGE 1 OF 1

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