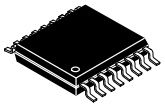
3-of-8 Decoder/Demultiplexer

74VHCT138A



TSSOP 16
CASE 948AH

General Description

The VHCT138A is an advanced high speed CMOS 3-to-8 DECODER fabricated with silicon gate CMOS technology. It achieves the high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation.

When the device is enabled, 3 Binary Select inputs (A_0, A_1 and A_2) determine which one of the outputs ($\overline{O}_0$–$\overline{O}_7$) will go LOW. When enable input E_3 is held LOW or either $\overline{E}_1$ or $\overline{E}_2$ is held HIGH, decoding function is inhibited and all outputs go HIGH. E_3, $\overline{E}_1$ and $\overline{E}_2$ inputs are provided to ease cascade connection and for use as an address decoder for memory systems. Protection circuits ensure that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage and to the output pins with V_{CC} = 0 V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3 V to 5 V systems and two supply systems such as battery backup.

Features

- High Speed: t_{PD} = 7.6 ns (Typ) at V_{CC} = 5 V
- Low Power Dissipation: I_{CC} = 4 μA (Max.) at T_A = 25 °C
- Power Down Protection Provided on All Inputs and Outputs
- Pin and Function Compatible with 74HCT138
- This Device is Pb-Free, Halide Free and is RoHS Compliant

Logic Symbols

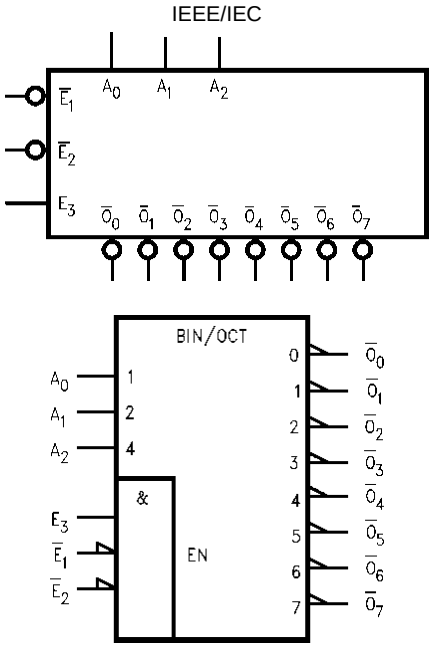
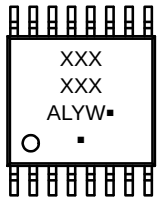


Figure 1. Logic Symbols

MARKING DIAGRAMS

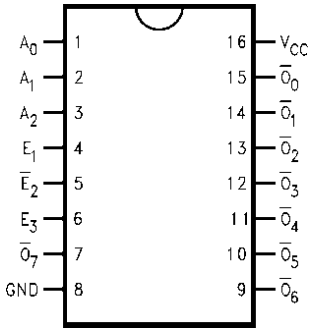


TSSOP 16

XXXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
A_0–A_2	Address Inputs
$\overline{E}_1$–$\overline{E}_2$	Enable Inputs
E_3	Enable Input
$\overline{O}_0$–$\overline{O}_7$	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 4 of this data sheet.

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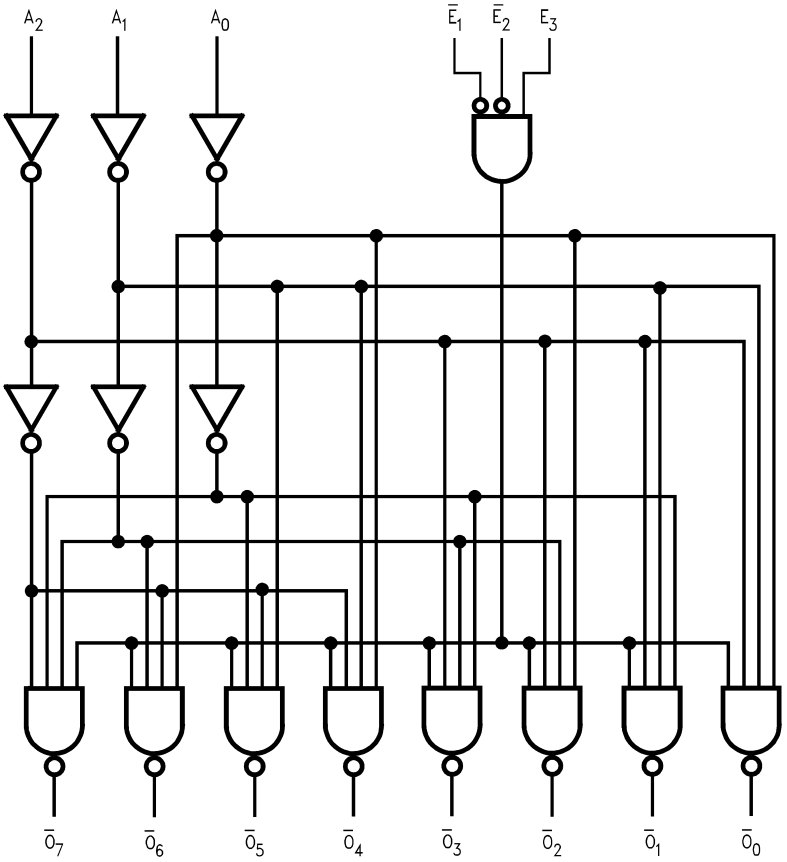
TRUTH TABLE

Inputs						Outputs							
$\overline{E}_1$	$\overline{E}_2$	E_3	A_0	A_1	A_2	$\overline{O}_0$	$\overline{O}_1$	$\overline{O}_2$	$\overline{O}_3$	$\overline{O}_4$	$\overline{O}_5$	$\overline{O}_6$	$\overline{O}_7$
H	X	X	X	X	X	H	H	H	H	H	H	H	H
X	H	X	X	X	X	H	H	H	H	H	H	H	H
X	X	L	X	X	X	H	H	H	H	H	H	H	H
L	L	H	L	L	L	L	H	H	H	H	H	H	H
L	L	H	H	L	L	H	L	H	H	H	H	H	H
L	L	H	L	H	L	H	H	L	H	H	H	H	H
L	L	H	H	H	L	H	H	H	L	H	H	H	H
L	L	H	L	L	H	H	H	H	H	L	H	H	H
L	L	H	H	L	H	H	H	H	H	H	L	H	H
L	L	H	L	H	H	H	H	H	H	H	H	L	H
L	L	H	H	H	H	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

LOGIC DIAGRAM



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Figure 2. Logic Diagram

MAXIMUM RATINGS

Symbol	Parameter		Value	Unit
V_{CC}	DC Supply Voltage		−0.5 to +6.5	V
V_{IN}	DC Input Voltage		−0.5 to +6.5	V
V_{OUT}	DC Output Voltage	Active Mode (High or Low State) Tristate Mode (Note 1) Power-Off Mode (V_{CC} = 0 V)	−0.5 to V_{CC} + 0.5 −0.5 to +6.5 −0.5 to +6.5	V
I_{IN}	DC Input Current, per Pin		±20	mA
I_{OUT}	DC Output Current, Per Pin		±25	mA
I_{CC}	DC Supply Current, V_{CC} and GND Pins		±75	mA
I_{IK}	Input Clamp Current		−20	mA
I_{OK}	Output Clamp Current		−20	mA
T_{STG}	Storage Temperature Range		−65 to +150	°C
T_L	Lead Temperature, 1 mm from Case for 10 Seconds		260	°C
T_J	Junction Temperature Under Bias		+150	°C
θ_{JA}	Thermal Resistance (Note 2)		159	°C/W
P_D	Power Dissipation in Still Air at 25 °C		787	mW
MSL	Moisture Sensitivity		Level 1	
F_R	Flammability Rating	Oxygen Index: 28 to 34	UL 94 V−0 @ 0.138 in	
V_{ESD}	ESD Withstand Voltage (Note 3)	Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri-stated.
2. Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
3. HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter		Min	Max	Unit
V_{CC}	DC Supply Voltage		2.0	5.5	V
V_{IN}	DC Input Voltage (Note 4)		0	5.5	V
V_{OUT}	DC Output Voltage (Note 4)	Active Mode (High or Low State) Tristate Mode Power-Off Mode (V_{CC} = 0 V)	0 0 0	V_{CC} 5.5 53.5	V
T_A	Operating Temperature		−40	+85	°C
t_r, t_f	Input Rise and Fall Time	V_{CC} = 4.5 V to 5.5 V	0	20	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must always be tied to an appropriate logic voltage level (e.g., either GND or V_{CC}). Unused outputs must be left open.

DC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions		V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to 85 °C		Unit
					Min	Typ	Max	Min	Max	
V_{IH}	HIGH Level Input Voltage			4.5−5.5	2.0	−	−	2.0	−	V
V_{IL}	LOW Level Input Voltage			4.5−5.5	−	−	0.8	−	0.8	V
V_{OH}	HIGH Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OH} = −50 μA	4.5	4.4	4.5	−	4.4	−	V
			I_{OH} = −8 mA		3.94	−	−	3.80	−	
V_{OL}	LOW Level Output Voltage	V_{IN} = V_{IH} or V_{IL}	I_{OL} = 50 μA	4.5	−	0.0	0.1	−	0.1	V
			I_{OL} = 8 mA		−	−	0.36	−	0.44	
I_{IN}	Input Leakage Current	V_{IN} = 5.5 V or GND		0−5.5	−	−	±0.1	−	±1.0	μA
I_{CC}	Quiescent Supply Current	V_{IN} = V_{CC} or GND		5.5	−	−	4.0		20.0	μA
I_{CCT}	Maximum I_{CC} / Input	V_{IN} = 3.4 V, All other inputs = V_{CC} or GND		5.5	−	−	1.35	−	1.50	mA
I_{OFF}	Output Leakage Current	V_{OUT} = 5.5 V		0	−	−	0.5	−	5.0	μA

AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = 25 °C			T_A = −40 °C to 85 °C		Unit
				Min	Typ	Max	Min	Max	
t_{PLH}, t_{PHL}	Propagation Delay, A_n to $\overline{O}_n$	C_L = 15 pF	5.0 ±0.5	−	7.6	10.4	1.0	12.0	ns
		C_L = 50 pF		−	8.1	11.4	1.0	13.0	
t_{PLH}, t_{PHL}	Propagation Delay, E_3 to $\overline{O}_n$	C_L = 15 pF	5.0 ±0.5	−	6.6	9.1	1.0	10.5	ns
		C_L = 50 pF		−	7.1	10.1	1.0	11.5	
t_{PLH}, t_{PHL}	Propagation Delay, $\overline{E}_1$ or $\overline{E}_2$ to $\overline{O}_n$	C_L = 15 pF	5.0 ±0.5	−	7.0	9.6	1.0	11.0	ns
		C_L = 50 pF		−	7.5	10.6	1.0	12.0	
C_{IN}	Input Capacitance	V_{CC} = Open	−	−	4	10	−	10	pF
C_{PD}	Power Dissipation Capacitance	(Note 5)	−	−	49	−	−	−	pF

5. C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (opr.) = C_{PD} • V_{CC} • f_{IN} + I_{CC}.

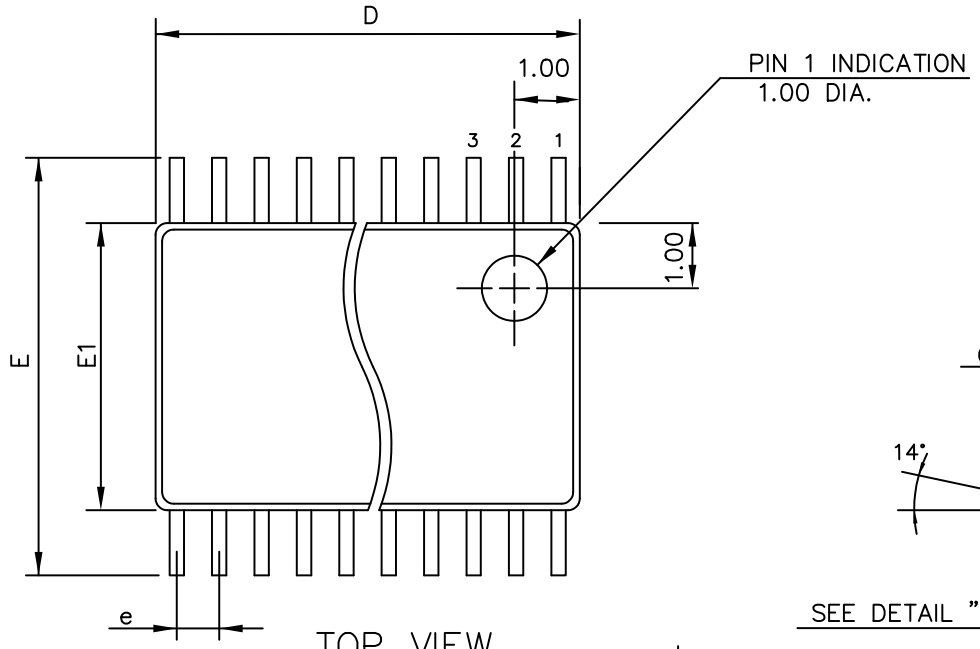
ORDERING INFORMATION

Device	Marking	Package	Shipping†
74VHCT138AMTCX	VHCT 138A	TSSOP 16 (Pb-Free, Halide Free)	2500 Tape & Reel

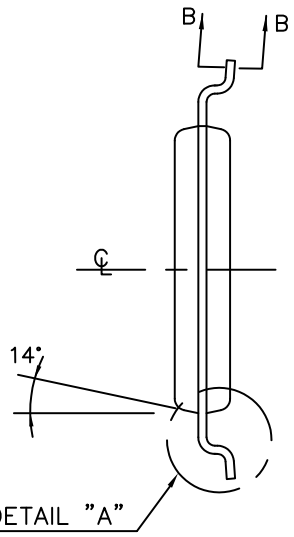
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

TSSOP 16
CASE 948AH
ISSUE O

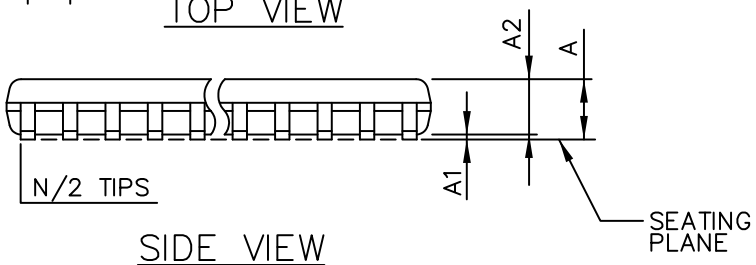
DATE 19 SEP 2008



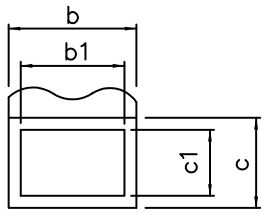
TOP VIEW



END VIEW



SIDE VIEW

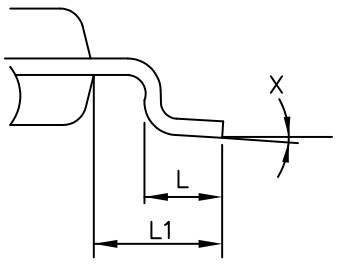


SECTION "B–B"

THIS TABLE FOR 0.65mm PITCH

SYMBOL	COMMON DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.10
A_1	0.05	——	0.15
A_2	0.85	0.90	0.95
b	0.19	–	0.30
b1	0.19	0.22	0.25
c	0.09	–	0.20
c1	0.09	0.127	0.16
D	SEE VARIATIONS		
E1	4.30	4.40	4.50
e	0.65 BSC		
E	6.40 BSC		
L	0.50	0.60	0.70
L1	1.00 REF		
N	SEE VARIATIONS		
X	0°	——	8°

NOTE VARIATIONS	D	N
AA/AAT	3.00 BSC	8
AB–1/ABT	5.00 BSC	14
AB/ABT	5.00 BSC	16
AD/ADT	7.80 BSC	24



DETAIL 'A'

ALL DIMENSIONS IN MILLIMETERS

MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15mm ON D PER SIDE

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