

Hex Schmitt Inverter 74VHCT14A

General Description

The VHCT14A is an advanced high speed CMOS Hex Schmitt Inverter fabricated with silicon gate CMOS technology. The VHCT14A contains six independent inverters which are capable of transforming slowly changing input signals into sharply defined, jitter–free output signals.

Protection circuits ensure that 0 V to 5.5 V can be applied to the input pins without regard to the supply voltage and to the output pins with $V_{CC}=0$ V. These circuits prevent device destruction due to mismatched supply and input/output voltages. This device can be used to interface 3 V to 5 V systems and two supply systems such as battery backup.

Features

- High Speed: $t_{PD} = 5.0 \text{ ns (Typ.)}$ at $T_A = 25^{\circ}\text{C}$
- High Noise Immunity: $V_{IH} = 2.0 \text{ V}$, $V_{IL} = 0.8 \text{ V}$
- Power Down Protection is Provided on All Inputs and Outputs
- Low Noise: $V_{OLP} = 1.0 \text{ V (Max.)}$
- Low Power Dissipation: $I_{CC} = 2 \mu A$ (Max.) at $T_A = 25^{\circ}C$
- Pin and Function Compatible with 74HCT14
- Pb-Free, Halogen Free/BFR Free and RoHS Compliant

Logic Symbol

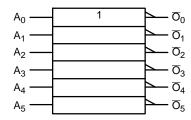


Figure 1. Logic Symbol

TRUTH TABLE

Α	Ō
L	Н
Н	L



TSSOP-14 WB CASE 948G

MARKING DIAGRAM

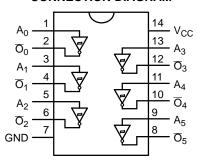


XXXXX = Specific Device Code A = Assembly Location

L = Wafer Lot Y = Year W = Work Week ■ Pb-Free Package

(Note: Microdot may be in either location)

CONNECTION DIAGRAM



PIN DESCRIPTION

Pin Names	Description
A _n	Inputs
Ō _n	Outputs

ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

74VHCT14A

MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V _{CC}	DC Supply Voltage	-0.5 to +6.5	V
V _{IN}	DC Input Voltage	-0.5 to +6.5	V
V _{OUT}	DC Output Voltage Active Mode (High or Low State) Tristate Mode (Note 1) Power–Off Mode (V _{CC} = 0 V)	-0.5 to V _{CC} + 0.5 -0.5 to +6.5 -0.5 to +6.5	V
I _{IN}	DC Input Current, Per Pin	±20	mA
I _{OUT}	DC Output Current, Per Pin	±25	mA
I _{CC}	DC Supply Current, V _{CC} and GND Pins	±50	mA
I _{IK}	Input Clamp Current	-20	mA
lok	Output Clamp Current	-20	mA
T _{STG}	Storage Temperature Range	-65 to +150	°C
TL	Lead Temperature, 1 mm from Case for 10 s	260	°C
TJ	Junction Temperature Under Bias	+150	°C
$\theta_{\sf JA}$	Thermal Resistance (Note 2)	150	°C/W
P _D	Power Dissipation in Still Air at 25°C	833	mW
V _{ESD}	ESD Withstand Voltage (Note 3) Human Body Model Charged Device Model	2000 N/A	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Applicable to devices with outputs that may be tri–stated.

- Measured with minimum pad spacing on an FR4 board, using 76 mm-by-114 mm, 2-ounce copper trace no air flow per JESD51-7.
 HBM tested to EIA / JESD22-A114-A. CDM tested to JESD22-C101-A. JEDEC recommends that ESD qualification to EIA/JESD22-A115A (Machine Model) be discontinued.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Unit
V _{CC}	DC Supply Voltage	4.5	5.5	V
V _{IN}	DC Input Voltage (Note 4)	0	5.5	V
V _{OUT}	DC Output Voltage (Note 4) Active Mode (High or Low State) Tristate Mode Power–Off Mode (V _{CC} = 0 V)	0 0 0	V _{CC} 5.5 5.5	V
T _A	Operating Temperature	-40	+85	°C
t _r , t _f	Input Rise or Fall Rate	0	No Limit	ns/V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

4. Unused inputs must be held HIĞH or LOW. They may not float.

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DC ELECTRICAL CHARACTERISTICS

			T _A = 25°C			$T_A = -40^{\circ}$	C to +85°C			
Symbol	Parameter	V _{CC} (V)	Con	nditions	Min	Тур	Max	Min	Max	Unit
V _P	Positive Threshold	4.5			-	_	1.9	_	1.9	V
	Voltage	5.5]		-	-	2.1	_	2.1	
V _N	Negative Threshold	4.5			0.5	-	_	0.5	-	V
	Voltage	5.5]		0.6	-	_	0.6	-	
V_{H}	Hysteresis Voltage	4.5			0.4	-	1.4	0.4	1.4	V
		5.5	1		0.4	_	1.5	0.4	1.5	
V _{OH}	HIGH Level Output	4.5	$V_{IN} = V_{IL}$	$I_{OH} = -50 \mu A$	4.40	4.50	_	4.40	-	V
	Voltage			$I_{OH} = -8 \text{ mA}$	3.94	-	_	3.80	-	
V _{OL}	LOW Level Output	4.5	$V_{IN} = V_{IH}$	I _{OL} = 50 μA	-	0.0	0.1	_	0.1	V
	Voltage			$I_{OL} = 8 \text{ mA}$	-	-	0.36	_	0.44	
I _{IN}	Input Leakage Current	0–5.5	V _{IN} = 5.5 V	or GND	-	-	±0.1	-	±1.0	μА
Icc	Quiescent Supply Current	5.5	$V_{IN} = V_{CC}$	V _{IN} = V _{CC} or GND		-	2.0	-	20.0	μА
Ісст	Maximum I _{CC} / Input	5.5	V _{IN} = 3.4 V, Other Inputs = V _{CC} or GND		-	-	1.35	-	1.50	mA
I _{OFF}	Output Leakage Current (Power Down State)	0.0	V _{OUT} = 5.5	V	_	_	0.5	_	5.0	μΑ

NOISE CHARACTERISTICS

	T _A = 25°C		25°C			
Symbol	Parameter		Conditions	Тур	Limits	Unit
V _{OLP}	Quiet Output Maximum Dynamic V _{OL} (Note 5)	5.0	C _L = 50 pF	0.8	1.0	V
V_{OLV}	Quiet Output Minimum Dynamic V _{OL} (Note 5)		C _L = 50 pF	-0.8	1.0	V
V_{IHD}	Minimum HIGH Level Dynamic Input Voltage (Note 5)	5.0	C _L = 50 pF	-	2.0	V
V _{ILD}	Maximum LOW Level Dynamic Input Voltage (Note 5)	5.0	C _L = 50 pF	_	0.8	V

^{5.} Parameter guaranteed by design.

AC ELECTRICAL CHARACTERISTICS

				T _A = 25°C T		$T_A = -40^{\circ}$	$T_A = -40^{\circ}C$ to +85°C		
Symbol	Parameter	V _{CC} (V)	Conditions	Min	Тур	Max	Min	Max	Unit
t _{PHL} ,	Propagation Delay	5.0 ±0.5	C _L = 15 pF	-	5.0	7.6	1.0	9.0	ns
t _{PLH}			C _L = 50 pF	-	6.5	9.6	1.0	11.0	
C _{IN}	Input Capacitance		V _{CC} = OPEN	-	2	10	-	10	pF
C _{PD}	Power Dissipation Capacitance		(Note 6)	-	11	-	-	-	pF

^{6.} C_{PD} is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I_{CC} (Opr.) = C_{PD} × V_{CC} × f_{IN} + I_{CC} / 6 (per gate)

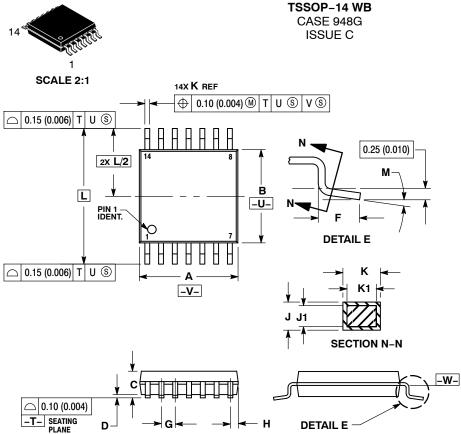
ORDERING INFORMATION

Device Order Number	Top Marking	Package Type	Shipping [†]
74VHCT14AMTCX	VHCT 14A	TSSOP-14 WB (Pb-Free, Halide Free)	2,500 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

DATE 17 FEB 2016





- NOTES.

 1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.

 2. CONTROLLING DIMENSION: MILLIMETER.

 3. DIMENSION A DOES NOT INCLUDE MOLD
- FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
 DIMENSION B DOES NOT INCLUDE
- INTERLEAD FLASH OR PROTRUSION.
 INTERLEAD FLASH OR PROTRUSION SHALL
- INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.

 DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.

 TERMINAL NUMBERS ARE SHOWN FOR DEEEDENIC OMITY.
- REFERENCE ONLY.
 DIMENSION A AND B ARE TO BE
- DETERMINED AT DATUM PLANE -W-.

	MILLIN	IETERS	INC	HES
DIM	MIN	MAX	MIN	MAX
Α	4.90	5.10	0.193	0.200
В	4.30	4.50	0.169	0.177
С		1.20		0.047
D	0.05	0.15 0.002		0.006
F	0.50	0.75	0.020	0.030
G	0.65	BSC	0.026 BSC	
Н	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40	BSC	0.252 BSC	
М	0°	8 °	0 °	8 °

GENERIC MARKING DIAGRAM*



= Assembly Location

L = Wafer Lot = Year

= Work Week W = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "■", may or may not be present. Some products may not follow the Generic Marking.

RECOMMENDED SOLDERING FOOTPRINT*

-	7.06
1	
	-
	U 0.65 PITCH
↓ □	The state of the s
14X 0.36	+==+ +
0.36 - 1.26	DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the onsemi Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

DOCUMENT NUMBER:	98ASH70246A	Electronic versions are uncontrolled except when accessed directly from the Document Report Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.			
DESCRIPTION:	TSSOP-14 WB		PAGE 1 OF 1		

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