# AMIS-42700

# Dual High Speed CAN Transceiver

## General Description

Controller area network (CAN) is a serial communication protocol, which supports distributed real−time control and multiplexing with high safety level. Typical applications of CAN−based networks can be found in automotive and industrial environments.

The AMIS−42700 Dual−CAN transceiver is the interface between up to two physical bus lines and the protocol controller and will be used for serial data interchange between different electronic units at more than one bus line. It can be used for both 12 V and 24 V systems.

The circuit consists of following blocks:

- Two differential line transmitters
- Two differential line receivers
- Interface to the CAN protocol handler
- Interface to expand the number of CAN busses
- Logic block including repeater function and the feedback suppression
- Thermal shutdown circuit (TSD)
- Short to battery treatment circuit

Due to the wide common−mode voltage range of the receiver inputs, the AMIS−42700 is able to reach outstanding levels of electromagnetic susceptibility (EMS). Similarly, extremely low electromagnetic emission (EME) is achieved by the excellent matching of the output signals.

### Key Features

- Fully compatible with the ISO 11898−2 standard
- Certified “Authentication on CAN Transceiver Conformance (d1.1)”
- High speed (up to 1 Mbit/s in function of the bus topology)
- Ideally suited for 12 V and 24 V industrial and automotive applications
- Low EME common−mode−choke is no longer required
- Differential receiver with wide common−mode range (±35 V) for high EMS
- No disturbance of the bus lines with an un−powered node
- Dominant time−out function
- Thermal protection
- Bus pins protected against transients in an automotive environment
- Short circuit proof to supply voltage and ground

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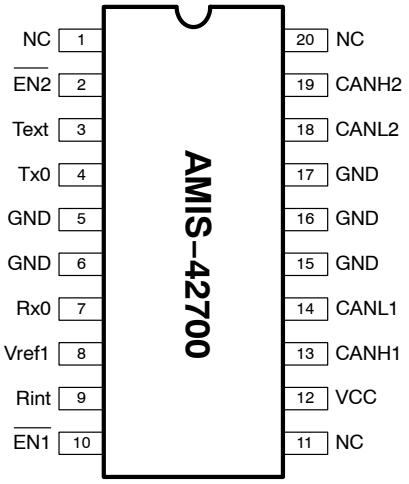
**PIN CONFIGURATION**




**SOIC 20**
**WC SUFFIX**
**CASE 751AQ**

**ORDERING INFORMATION**

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

**Table 1. Technical Characteristics**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CANHx}$ | DC voltage at pin CANH1/2 | 0 < $V_{CC}$ < 5.25 V; no time limit | −45 | +45 | V |
| $V_{CANLx}$ | DC voltage at pin CANL1/2 | 0 < $V_{CC}$ < 5.25 V; no time limit | −45 | +45 | V |
| $V_{o(dif)(bus\_dom)}$ | Differential bus output voltage in dominant state | 42.5 Ω < $R_{LT}$ < 60 Ω | 1.5 | 3 | V |
| CM−range | Input common−mode range for comparator | Guaranteed differential receiver threshold and leakage current | −35 | +35 | V |
| $V_{CM-peak}$ | Common−mode peak | See Figures 9 and 10 (Note 1) | −1000 | 1000 | mV |
| $V_{CM-step}$ | Common−mode step | See Figures 9 and 10 (Note 1) | −250 | 250 | mV |

1. The parameters $V_{CM-peak}$ and $V_{CM-step}$ guarantee low EME.

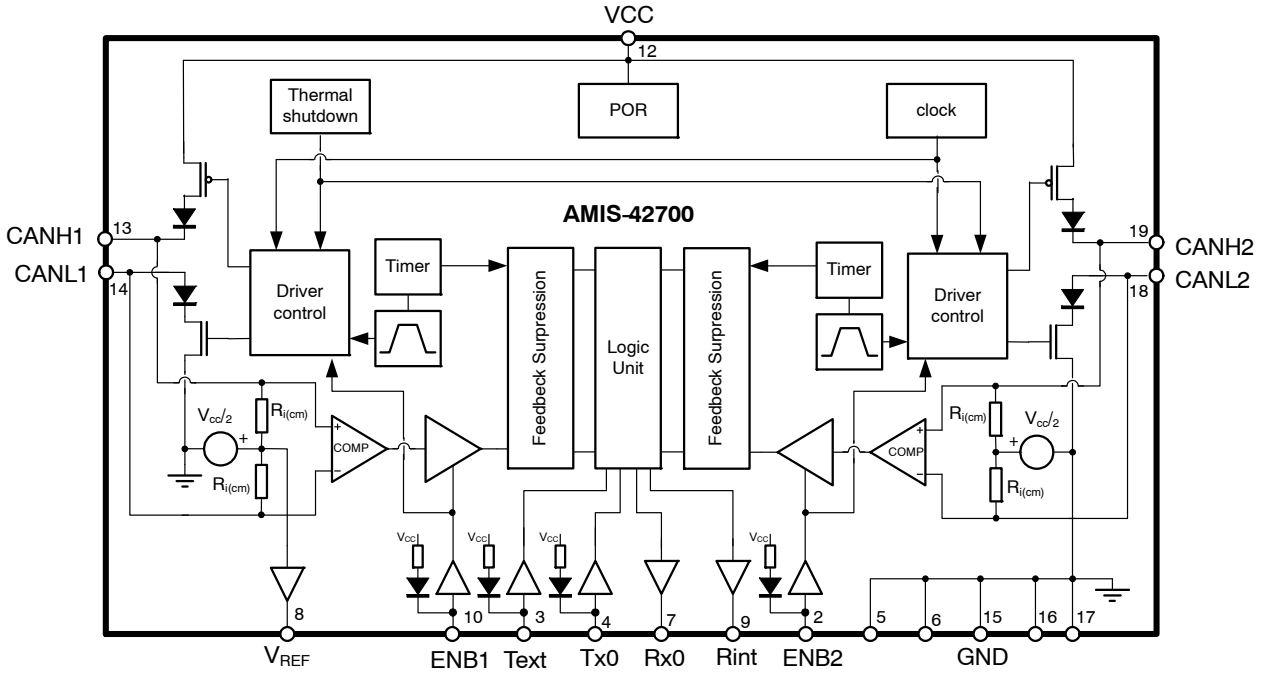



**Figure 1. Block Diagram**

## Typical Application

### Application Description

AMIS−42700 is especially designed to provide the link between a CAN controller (protocol IC) and two physical busses. It is able to operate in three different modes:

- Dual CAN
- A CAN−bus extender
- A CAN−bus repeater

## Application Schematics

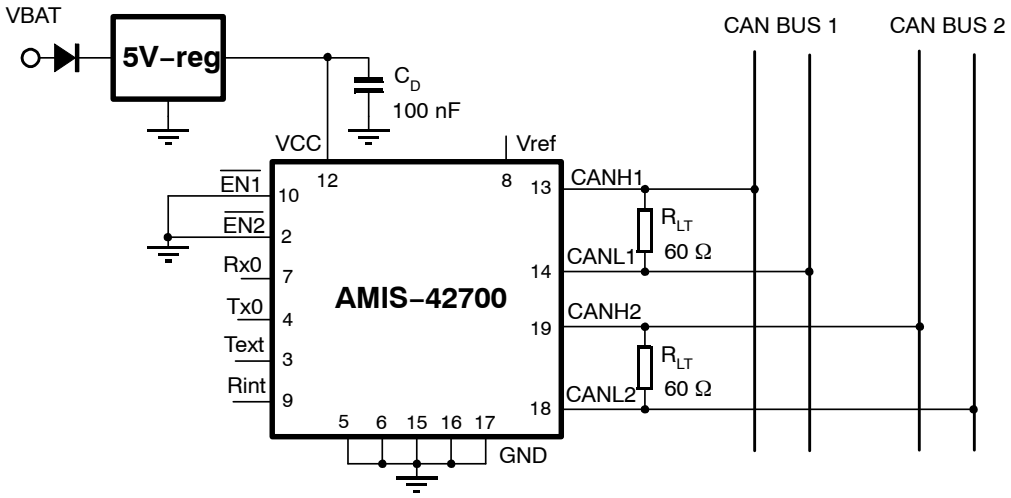



**Figure 2. Application Diagram CAN−bus Repeater**

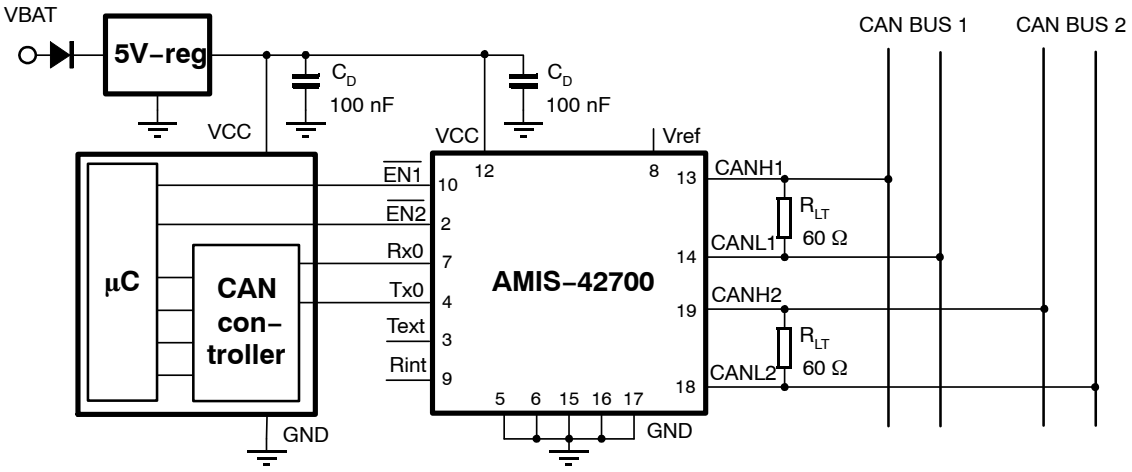



**Figure 3. Application Diagram Dual−CAN**

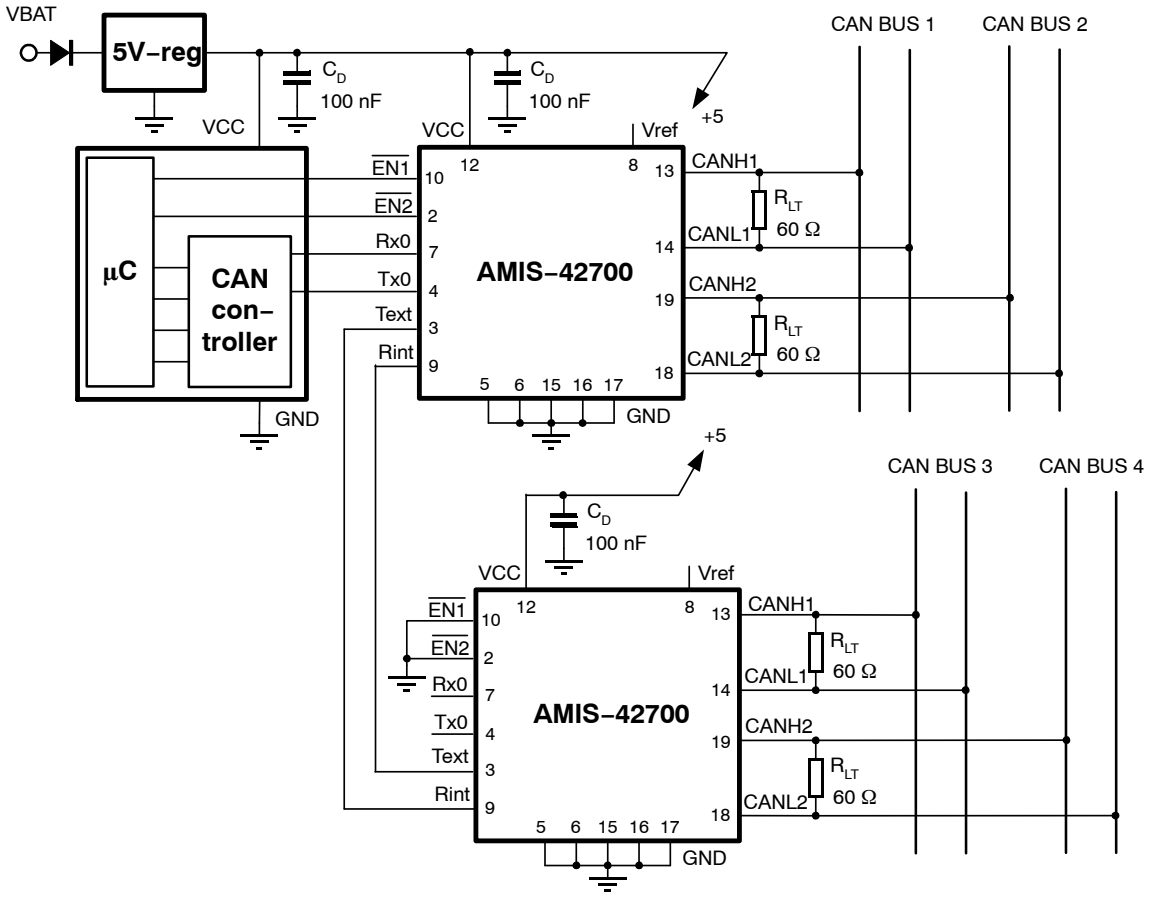



**Figure 4. Application Diagram CAN−bus Extender**

**Table 2. Pin Out**

| Pin | Name | Description |
|---|---|---|
| 1 | NC | Not connected |
| 2 | ENB2 | Enable input, bus system 2; internal pull−up |
| 3 | Text | Multi−system transmitter Input; internal pull−up |
| 4 | Tx0 | Transmitter input; internal pull−up |
| 5 | GND | Ground connection (Note 2) |
| 6 | GND | Ground connection (Note 2) |
| 7 | Rx0 | Receiver output |
| 8 | $V_{REF1}$ | Reference voltage |
| 9 | Rint | Multi−system receiver output |
| 10 | ENB1 | Enable input, bus system 1; internal pull−up |
| 11 | NC | Not connected |
| 12 | VCC | Positive supply voltage |
| 13 | CANH1 | CANH transceiver I/O bus system 1 |
| 14 | CANL1 | CANL transceiver I/O bus system 1 |
| 15 | GND | Ground connection (Note 2) |
| 16 | GND | Ground connection (Note 2) |
| 17 | GND | Ground connection (Note 2) |
| 18 | CANL2 | CANL transceiver I/O bus system 2 |
| 19 | CANH2 | CANH transceiver I/O bus system 2 |
| 20 | NC | Not connected |

2. In order to ensure the chip performance, all these pins need to be connected to GND on the PCB.

## Functional Description

### Overall Functional Description

AMIS−42700 is specially designed to provide the link between the protocol IC (CAN controller) and two physical bus lines. Data interchange between those two bus lines is realized via the logic unit inside the chip. To provide an independent switch−off of the transceiver units for both bus systems by a third device (e.g. the μC), enable−inputs for the corresponding driving and receiving sections are provided. As long as both lines are enabled, they appear as one logical bus to all nodes connected to either of them.

The bus lines can have two logical states, dominant or recessive. A bus is in the recessive state when the driving sections of all transceivers connected to the bus are passive. The differential voltage between the two wires is approximately zero. If at least one driver is active, the bus changes into the dominant state. This state is represented by a differential voltage greater than a minimum threshold and therefore by a current flow through the terminating resistors of the bus line. The recessive state is overwritten by the dominant state.

In case of a fault (like short circuit) is present on one of the bus lines, it remains limited to that bus line where it occurs. Data interchange from the protocol IC to the other bus system and on this bus system itself can be continued.

AMIS−42700 can be also used for only one bus system. If the connections for the second bus system are simply left open it serves as a single transceiver for an electronic unit. For correct operation, it is necessary to terminate the open bus by the proper termination resistor.

### Logic Unit and CAN Controller Interface

The logic unit inside AMIS−42700 provides data transfer from/to the digital interface to/from the two busses and from one bus to the other bus. The detailed function of the logic unit is described in Table 3.

All digital input pins, including ENBx, have an internal pull-up resistor to ensure a recessive state when the input is not connected or is accidentally interrupted. A dominant state on the bus line is represented by a low-level at the digital interface; a recessive state is represented by a high-level.

Dominant state received on any bus (if enabled) causes a dominant state on both busses, pin Rint and pin Rx0. Dominant signal on any of the input pins Tx0 and Text causes transmission of dominant on both bus lines (if enabled).

Digital inputs Tx0 and Text are used for connecting the internal logic's of several IC's to obtain versions with more than two bus outputs (see Figure 4: Application Diagram CAN-bus Extender). They have also a direct logical link to pins Rx0 and Rint independently on the EN1x pins − dominant on Tx0 is directly transferred to both Rx0 and Rint pins, dominant on Text is only transferred to Rx0.

### Transmitters

The transceiver includes two transmitters, one for each bus line, and a driver control circuit. Each transmitter is implemented as a push and a pull driver. The drivers will be active if the transmission of a dominant bit is required. During the transmission of a recessive bit all drivers are passive. The transmitters have a built−in current limiting circuit that protects the driver stages from damage caused by accidental short circuit to either positive supply voltage or to ground. Additionally a thermal protection circuit is integrated.

The driver control circuit ensures that the drivers are switched on and off with a controlled slope to limit EME. The driver control circuit will be controlled itself by the thermal protection circuit, the timer circuit and the logic unit.

The enable signal ENBx allows the transmitter to be switched off by a third device (e.g. the μC). In the disabled state (ENBx = high) the corresponding transmitter behaves as in the recessive state.

**Table 3. Function of the Logic Unit** (**bold** letters describe input signals)

| EN1B | EN2B | TX0 | TEXT | Bus 1 State | Bus 2 State | RX0 | RINT |
|---|---|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | dominant | dominant | 0 | 0 |
| 0 | 0 | 0 | 1 | dominant | dominant | 0 | 0 |
| 0 | 0 | 1 | 0 | dominant | dominant | 0 | 1 |
| 0 | 0 | 1 | 1 | recessive | recessive | 1 | 1 |
| 0 | 0 | 1 | 1 | **dominant** (Note 3) | dominant | 0 | 0 |
| 0 | 0 | 1 | 1 | dominant | **dominant** (Note 3) | 0 | 0 |
| 0 | 1 | 0 | 0 | dominant | recessive | 0 | 0 |
| 0 | 1 | 0 | 1 | dominant | recessive | 0 | 0 |
| 0 | 1 | 1 | 0 | dominant | recessive | 0 | 1 |
| 0 | 1 | 1 | 1 | recessive | recessive | 1 | 1 |
| 0 | 1 | 1 | 1 | **dominant** (Note 3) | recessive | 0 | 0 |

3. Dominant detected by the corresponding receiver.

**Table 3. Function of the Logic Unit** (**bold** letters describe input signals)

| EN1B | EN2B | TX0 | TEXT | Bus 1 State | Bus 2 State | RX0 | RINT |
|---|---|---|---|---|---|---|---|
| 0 | 1 | 1 | 1 | recessive | **dominant** (Note 3) | 1 | 1 |
| 1 | 0 | 0 | 0 | recessive | dominant | 0 | 0 |
| 1 | 0 | 0 | 1 | recessive | dominant | 0 | 0 |
| 1 | 0 | 1 | 0 | recessive | dominant | 0 | 1 |
| 1 | 0 | 1 | 1 | recessive | recessive | 1 | 1 |
| 1 | 0 | 1 | 1 | **dominant** (Note 3) | recessive | 1 | 1 |
| 1 | 0 | 1 | 1 | recessive | **dominant** (Note 3) | 0 | 0 |
| 1 | 1 | 0 | 0 | recessive | recessive | 0 | 0 |
| 1 | 1 | 0 | 1 | recessive | recessive | 0 | 0 |
| 1 | 1 | 1 | 0 | recessive | recessive | 0 | 1 |
| 1 | 1 | 1 | 1 | recessive | recessive | 1 | 1 |
| 1 | 1 | 1 | 1 | **dominant** (Note 3) | recessive | 1 | 1 |
| 1 | 1 | 1 | 1 | recessive | **dominant** (Note 3) | 1 | 1 |

3. Dominant detected by the corresponding receiver.

### Receivers

Two bus receiving sections sense the states of the bus lines. Each receiver section consists of an input filter and a fast and accurate comparator. The aim of the input filter is to improve the immunity against high−frequency disturbances and also to convert the voltage at the bus lines CANHx and CANLx, which can vary from –12 V to +12 V, to voltages in the range 0 to 5 V, which can be applied to the comparators.

The output signal of the comparators is gated by the ENBx signal. In the disabled state (ENBX = high), the output signal of the comparator will be replaced by a permanently recessive state and does not depend on the bus voltage. In the enabled state the receiver signal sent to the logic unit is identical to the comparator output signal.

### Time−out Counters

To avoid that the transceiver drives a permanent dominant state on either of the bus lines (blocking all communication), time−out function is implemented. Signals on pins Tx0 and Text as well as both bus receivers are connected to the logic unit through independent timers. If the input of the timer stays dominant for longer than parameter tdom, it's replaced by a recessive signal on the timer output.

### Feedback Suppression

The logic unit described in Table 3 constantly ensures that dominant symbols on one bus line are transmitted to the other bus line without imposing any priority on either of the lines. This feature would lead to an "interlock" state with permanent dominant signal transmitted to both bus lines, if no extra measure is taken.

Therefore a feedback suppression is included inside the logic unit of the transceiver. This block masks−out reception on that bus line, on which a dominant is actively transmitted. The reception becomes active again only with certain delay after the dominant transmission on this line is finished.

### Power−on−Reset (POR)

While Vcc voltage is below the POR level, the POR circuit makes sure that:

- The counters are kept in the reset mode and stable state without current consumption
- Inputs are disabled (don't care)
- Outputs are high impedant; only Rx0 = high−level
- Analog blocks are in power down
- Oscillator not running and in power down
- CANHx and CANLx are recessive
- VREF output high impedant for POR not released

### Over Temperature Detection

A thermal protection circuit is integrated to prevent the transceiver from damage if the junction temperature exceeds thermal shutdown level. Because the transmitters dissipate most of the total power, the transmitters will be switched off only to reduce power dissipation and IC temperature. All other IC functions continue to operate.

### Fault Behavior

A fault like a short circuit is limited to that bus line where it occurs; hence data interchange from the protocol IC to the other bus system is not affected.

When the voltage at the bus lines is going out of the normal operating range (−12 V to +12 V), the receiver is not allowed to erroneously detect a dominant state.

### Short Circuits

As specified in the maximum ratings, short circuits of the bus wires CANHx and CANLx to the positive supply voltage Vbat or to ground must not destroy the transceiver. A short circuit between CANHx and CANLx must not destroy the IC as well.

The dedicated comparator (L2VBAT) on CANL pin detects the short to battery and after debounce time−out switches off the affected driver only. The receiver of the affected driver has to operate normally.

### Faulty Supply

In case of a faulty supply (missing connection of the electronic unit or the transceiver to ground, missing connection of the electronic unit to Vbat or missing connection of the transceiver to Vcc), the power supply module of the electronic unit will operate such that the transceiver is not supplied, i.e. the voltage Vcc is below the POR level. In this condition the bus connections of the transceiver must be in the POR state.

If the ground line of the electronic unit is interrupted, Vbat may be applied to the Vcc pin (measured relative to the original ground potential, to which the other units on the bus are connected).

### Reverse Electronic Unit (ECU) Supply

If the connections for ground and supply voltage of an electronic unit (ECU) (max. 50 V) which provides Vcc for the transceiver are exchanged, this transceiver has a ground potential which may be up to 50 V higher than that of the other transceivers. In this case no transceiver must be destroyed even if several of them are connected via the bus system.

Any exchange among the six connections CANH1, CANH2, CANL1, CANL2, ground, and supply voltage of the electronic unit at the connector of the unit must never lead to the destruction of any transceiver of the bus system.

## Electrical Characteristics

### Definitions

All voltages are referenced to GND. Positive currents flow into the IC. Sinking current means that the current is flowing into the pin. Sourcing current means that the current is flowing out of the pin.

### Absolute Maximum Ratings

Stresses above those listed in Table 4 may cause permanent device failure. Exposure to absolute maximum ratings for extended periods may affect device reliability.

**Table 4. Absolute Maximum Ratings**

| Symbol | Parameter | Conditions | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{CC}$ | Supply voltage | | −0.3 | +7 | V |
| $V_{CANHx}$ | DC voltage at pin CANH1/2 | $0 < V_{CC} < 5.25$ V; no time limit | −45 | +45 | V |
| $V_{CANLx}$ | DC voltage at pin CANL1/2 | $0 < V_{CC} < 5.25$ V; no time limit | −45 | +45 | V |
| $V_{digIO}$ | DC voltage at digital IO pins (EN1B, EN2B, Rint, Rx0, Text, Tx0) | | −0.3 | $V_{CC}$ + 0.3 | V |
| $V_{REF}$ | DC voltage at pin $V_{REF}$ | | −0.3 | $V_{CC}$ + 0.3 | V |
| $V_{tran(CANHx)}$ | Transient voltage at pin CANH1/2 | (Note 4) | −150 | +150 | V |
| $V_{tran(CANLx)}$ | Transient voltage at pin CANL1/2 | (Note 4) | −150 | +150 | V |
| $V_{esd(CANLx/CANHx)}$ | ESD voltage at CANH1/2 and CANL1/2 pins | (Note 5)<br>(Note 7) | −4<br>−500 | +4<br>+500 | kV<br>V |
| $V_{esd}$ | ESD voltage at all other pins | (Note 5)<br>(Note 7) | −2<br>−250 | +2<br>+250 | kV<br>V |
| Latch−up | Static latch−up at all pins | (Note 6) | | 100 | mA |
| $T_{stg}$ | Storage temperature | | −55 | +155 | °C |
| $T_{amb}$ | Ambient temperature | | −40 | +125 | °C |
| $T_{junc}$ | Maximum junction temperature | | −40 | +150 | °C |

4. Applied transient waveforms in accordance with “ISO 7637 part 3”, test pulses 1, 2, 3a, and 3b (see Figure 5).
5. Standardized human body model (HBM) ESD pulses in accordance to MIL883 method 3015. Supply pin 8 is ±2 kV.
6. Static latch−up immunity: static latch−up protection level when tested according to EIA/JESD78.
7. Standardized charged device model ESD pulses when tested according to EOS/ESD DS5.3−1993.

**Table 5. Thermal Characteristics**

| Symbol | Parameter | Conditions | Value | Unit |
|---|---|---|---|---|
| $R_{th(vj-a)}$ | Thermal resistance from junction to ambient in SO20 package | In free air | 85 | K/W |
| $R_{th(vj-s)}$ | Thermal resistance from junction to substrate of bare die | In free air | 45 | K/W |

**Table 6. DC and Timing Characteristics** ($V_{CC}$ = 4.75 to 5.25 V; $T_{junc}$ = −40 to +150°C; $R_{LT}$ = 60 W unless specified otherwise.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY (pin $V_{CC}$)** | | | | | | |
| $I_{CC}$ | Supply current, no loads on digital outputs, both busses enabled | Dominant transmitted<br>Recessive transmitted | | 45 | 137.5<br>19.5 | mA |
| PORL_VCC | Power−on−reset level on $V_{CC}$ | | 2.2 | | 4.7 | V |
| **DIGITAL INPUTS (Tx0, Text, EN1B, EN2B)** | | | | | | |
| $V_{IH}$ | High−level input voltage | | 0.7 x $V_{CC}$ | − | $V_{CC}$ | V |
| $V_{IL}$ | Low−level input voltage | | −0.3 | − | 0.3 x $V_{CC}$ | V |
| $I_{IH}$ | High−level input current | $V_{IN}$ = $V_{CC}$ | −5 | 0 | +5 | μA |
| $I_{IL}$ | Low−level input current | $V_{IN}$ = 0 V | −75 | −200 | −350 | μA |
| $C_i$ | Input capacitance | Not tested | − | 5 | 10 | pF |
| **DIGITAL OUTPUTS (pin Rx0, Rint)** | | | | | | |
| $I_{oh}$ | High−level output current | $V_o$ = 0.7 x $V_{CC}$ | −5 | −10 | −15 | mA |
| $I_{ol}$ | Low−level output current | $V_o$ = 0.3 x $V_{CC}$ | 5 | 10 | 15 | mA |
| **REFERENCE VOLTAGE OUTPUT (pin $V_{REF1}$)** | | | | | | |
| $V_{REF}$ | Reference output voltage | −50 μA < $I_{VREF}$ < +50 μA | 0.45 x $V_{CC}$ | 0.50 x $V_{CC}$ | 0.55 x $V_{CC}$ | V |
| $V_{REF\_CM}$ | Reference output voltage for full common mode range | −35 V <$V_{CANHx}$ < +35 V;<br>−35 V <$V_{CANLx}$ < +35 V | 0.40 x $V_{CC}$ | 0.50 x $V_{CC}$ | 0.60 x $V_{CC}$ | V |
| **BUS LINES (pins CANH1/2 and CANL1/2)** | | | | | | |
| $V_{o(reces)}$ (CANHx) | Recessive bus voltage at pin CANH1/2 | $V_{Tx0}$ = $V_{CC}$; no load | 2.0 | 2.5 | 3.0 | V |
| $V_{o(reces)}$ (CANLx) | Recessive bus voltage at pin CANL1/2 | $V_{Tx0}$ = $V_{CC}$; no load | 2.0 | 2.5 | 3.0 | V |
| $I_{o(reces)}$ (CANHx) | Recessive output current at pin CANH1/2 | −35 V < $V_{CANHx}$ < +35 V;<br>0 V < $V_{CC}$ < 5.25 V | −2.5 | − | +2.5 | mA |
| $I_{o(reces)}$ (CANLx) | Recessive output current at pin CANL1/2 | −35 V < $V_{CANLx}$ < +35 V;<br>0 V < $V_{CC}$ < 5.25 V | −2.5 | − | +2.5 | mA |
| $V_{o(dom)}$ (CANHx) | Dominant output voltage at pin CANH1/2 | $V_{Tx0}$ = 0 V | 3.0 | 3.6 | 4.25 | V |
| $V_{o(dom)}$ (CANLx) | Dominant output voltage at pin CANL1/2 | $V_{Tx0}$ = 0 V | 0. 5 | 1.4 | 1.75 | V |
| $V_{o(dif)\ (bus)}$ | Differential bus output voltage ($V_{CANHx}$ − $V_{CANLx}$) | $V_{Tx0}$ = 0 V; dominant;<br>42.5 Ω < $R_{LT}$ < 60 Ω | 1.5 | 2.25 | 3.0 | V |
| | | $V_{TxD}$ = $V_{CC}$;<br>recessive; no load | −120 | 0 | +50 | mV |
| $I_{o(sc)}$ (CANHx) | Short circuit output current at pin CANH1/2 | $V_{CANHx}$ = 0 V;<br>$V_{Tx0}$ = 0 V | −45 | −70 | −120 | mA |
| $I_{o(sc)\ (CANLx)}$ | Short circuit output current at pin CANL1/2 | $V_{CANLx}$ = 36 V;<br>$V_{Tx0}$ = 0 V (Note 8) | 45 | 70 | 120 | mA |

8. Guaranteed by design for VBAT = 36 V; measured in production for VBAT = 7 V to avoid short−2−VBAT detection

**Table 6. DC and Timing Characteristics** ($V_{CC}$ = 4.75 to 5.25 V; $T_{junc}$ = −40 to +150°C; $R_{LT}$ = 60 W unless specified otherwise.)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **BUS LINES (pins CANH1/2 and CANL1/2)** | | | | | | |
| $V_{i(dif)(th)}$ | Differential receiver threshold voltage | −5 V < $V_{CANLx}$ < +12 V; −5 V < $V_{CANHx}$ < +12 V; see Figure 6 | 0.5 | 0.7 | 0.9 | V |
| $V_{ihcm(dif)\ (th)}$ | Differential receiver threshold voltage for high common−mode | −35 V < $V_{CANLx}$ < +35 V; −35 V < $V_{CANHx}$ < +35 V; see Figure 6 | 0.3 | 0.7 | 1.05 | V |
| $V_{i(dif)\ (hys)}$ | Differential receiver input voltage hysteresis | −35V < $V_{CANL}$ < +35 V; −35 V < $V_{CANH}$ < +35 V; see Figure 6 | 50 | 70 | 100 | mV |
| $R_{i(cm)}$ (CANHx) | Common−mode input resistance at pin CANH1/2 | | 15 | 26 | 37 | KΩ |
| $R_{i(cm)}$ (CANLx) | Common−mode input resistance at pin CANL1/2 | | 15 | 26 | 37 | KΩ |
| $R_{i(cm)(m)}$ | Matching between pin CANH1/2 and pin CANL1/2 common−mode input resistance | $V_{CANHx}$ = $V_{CANLx}$ | −3 | 0 | +3 | % |
| $R_{i(dif)}$ | Differential input resistance | | 25 | 50 | 75 | KΩ |
| $C_{i(CANHx)}$ | Input capacitance at pin CANH1/2 | $V_{Tx0}$ = $V_{CC}$; not tested | | 7.5 | 20 | pF |
| $C_{i(CANLx)}$ | Input capacitance at pin CANL1/2 | $V_{Tx0}$ = $V_{CC}$; not tested | | 7.5 | 20 | pF |
| $C_{i(dif)}$ | Differential input capacitance | $V_{Tx0}$ = $V_{CC}$; not tested | | 3.75 | 10 | pF |
| $I_{LI(CANHx)}$ | Input leakage current at pin CANH1/2 | $V_{CC}$ < PORL_VCC; −5.25 V < $V_{CANHx}$ < 5.25 V | −350 | 170 | 350 | μA |
| $I_{LI(CANLx)}$ | Input leakage current at pin CANL1/2 | $V_{CC}$ < PORL_VCC; −5.25 V < $V_{CANLx}$ < 5.25 V | −350 | 170 | 350 | μA |
| $V_{CM-peak}$ | Common−mode peak during transition from dom → rec or rec → dom | see Figure 10 | −1000 | | 1000 | mV |
| $V_{CM-step}$ | Difference in common−mode between dominant and recessive state | see Figure 10 | −250 | | 250 | mV |
| $V_{CANL2VBAT}$ | Detection level for CANL1/2 short to VBAT | | 7 | | 9.5 | V |
| **THERMAL SHUTDOWN** | | | | | | |
| $T_{j(sd)}$ | Shutdown junction temperature | | 150 | | | °C |
| **TIMING CHARACTERISTICS** (see Figures 7 and 8) | | | | | | |
| $t_{d(Tx-BUSon)}$ | Delay Tx0/Text to bus active | | 40 | 85 | 120 | ns |
| $t_{d(Tx-BUSoff)}$ | Delay Tx0/Text to bus inactive | | 30 | 60 | 115 | ns |
| $t_{d(BUSon-RX)}$ | Delay bus active to Rx0/Rint | | 25 | 55 | 115 | ns |
| $t_{d(BUSoff-RX)}$ | Delay bus inactive to Rx0/Rint | | 65 | 100 | 145 | ns |
| $t_{d(ENxB)}$ | Delay from EN1B to bus active/inactive | | | 100 | 200 | ns |
| $t_{d(Tx-Rx)}$ | Delay from Tx0 to Rx0/Rint and from Text to Rx0 (direct logical path) | 15 pF on the digital output | 4 | 10 | 35 | ns |
| $t_{d(CAN2VBAT)}$ | Reaction time of the CANL−to−VBAT short detector | Short occurring | 1 | | 4 | μs |
| | | Short disappearing | 1 | | 5.5 | μs |
| $t_{dom}$ | Time out counter interval | | 250 | 450 | 750 | μs |
| $t_{d(FBS)}$ | Delay for feedback suppression release | | 5+ $t_{d(BUSon-RX)}$ | | 330 | ns |

8. Guaranteed by design for VBAT = 36 V; measured in production for VBAT = 7 V to avoid short−2−VBAT detection

## Measurement Set−ups and Definitions

Schematics are given for single CAN transceiver.

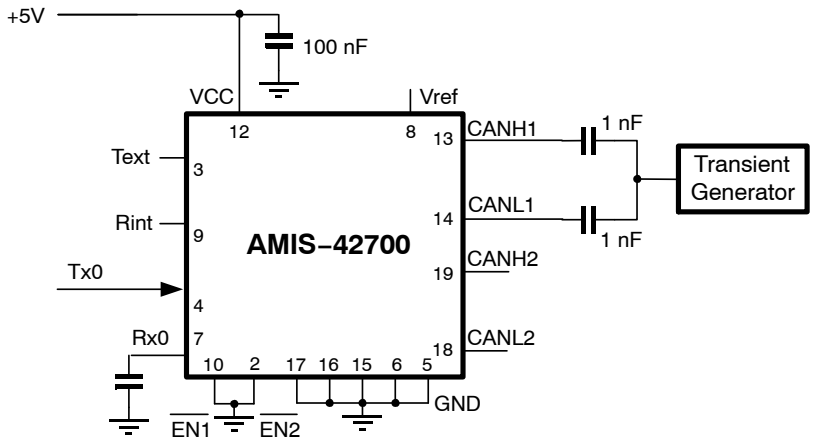



**Figure 5. Test Circuit for Automotive Transients**

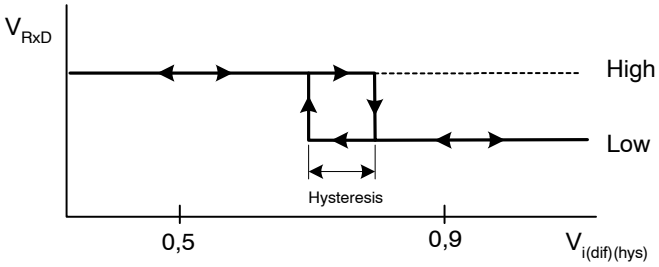



**Figure 6. Hysteresis of the Receiver**

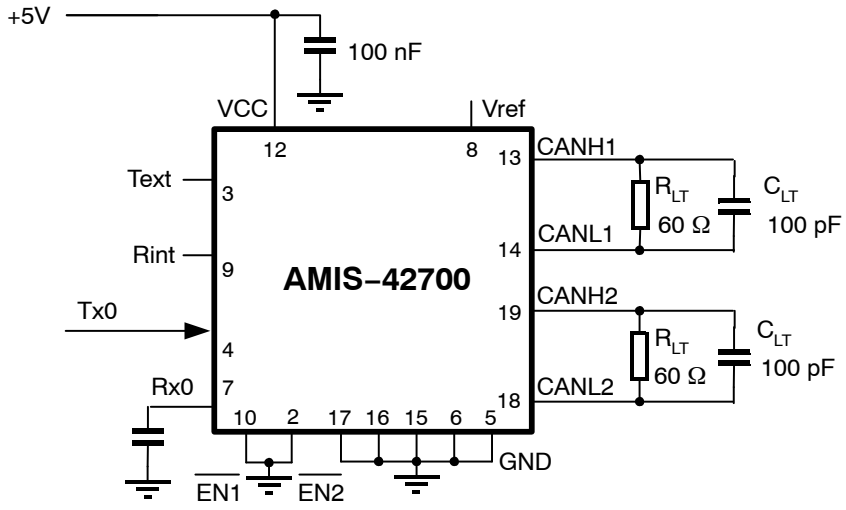



**Figure 7. Test Circuit for Timing Characteristics**

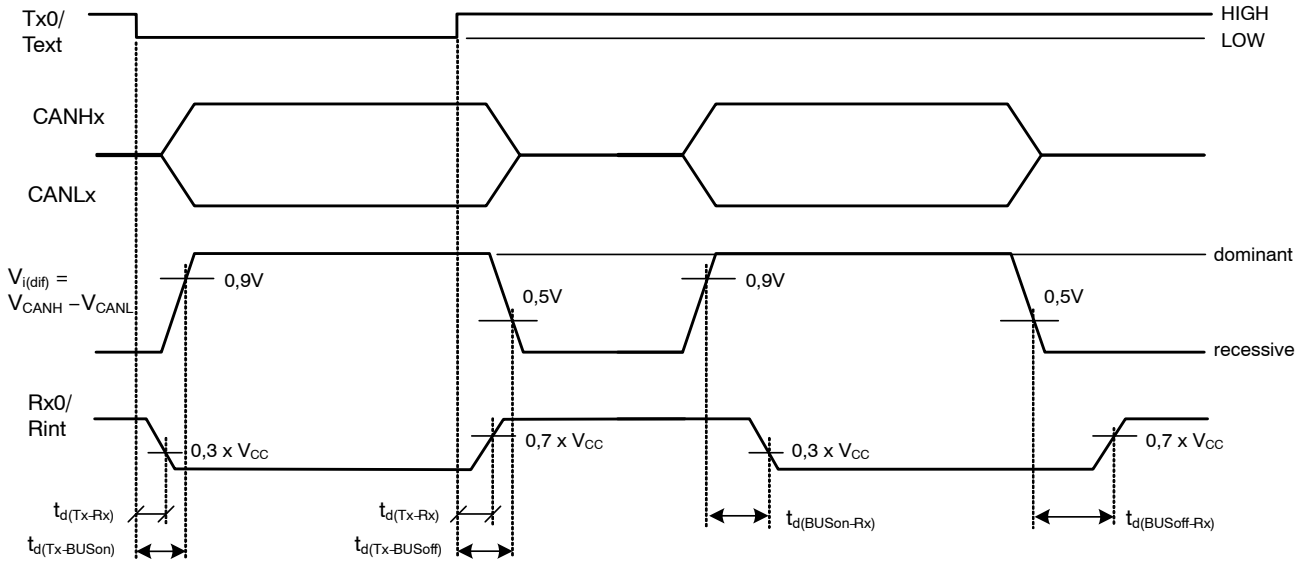



**Figure 8. Timing Diagram for AC Characteristics**

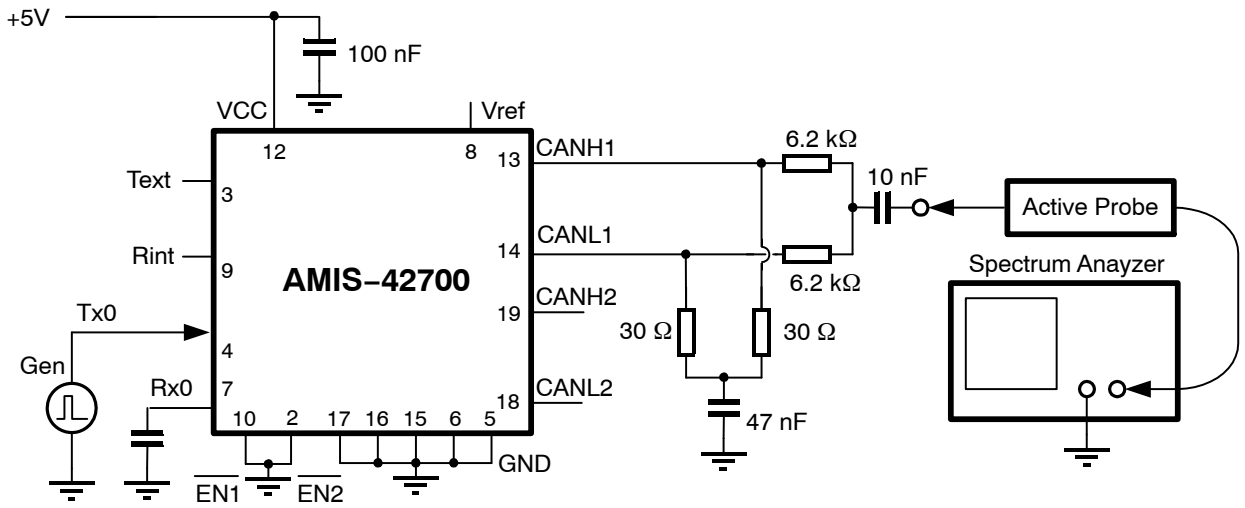



**Figure 9. Basic Test Set−up for Electromagnetic Measurement**

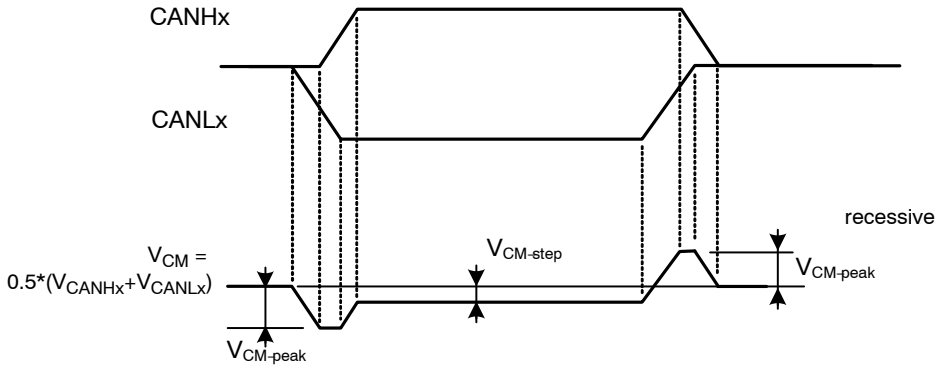



**Figure 10. Common−mode Voltage Peaks** (see measurement set−up Figure 9)

**ORDERING INFORMATION**

| Part Number | Package | Container | | Temperature Range |
|---|---|---|---|---|
| | | Shipping Configuration | Quantity | |
| AMIS42700WCGA4H | SOIC 150 20 300 GREEN | Rail | 38 | −40°C to 125°C |
| AMIS42700WCGA4RH | SOIC 150 20 300 GREEN | Tape & Reel | 1500 | −40°C to 125°C |

## Soldering

### Introduction to Soldering Surface Mount Packages

This text gives a very brief insight to a complex technology. A more in−depth account of soldering ICs can be found in the ON Semiconductor “Data Handbook IC26; Integrated Circuit Packages” (document order number 9398 652 90011). There is no soldering method that is ideal for all surface mount IC packages. Wave soldering is not always suitable for surface mount ICs, or for printed−circuit boards with high population densities. In these situations reflow soldering is often used.

### Re−flow Soldering

Re−flow soldering requires solder paste (a suspension of fine solder particles, flux and binding agent) to be applied to the printed−circuit board by screen printing, stenciling or pressure−syringe dispensing before package placement. Several methods exist for re−flowing; for example, infrared/convection heating in a conveyor type oven. Throughput times (preheating, soldering and cooling) vary between 100 and 200 seconds depending on heating method. Typical re−flow peak temperatures range from 215°C to 260°C.

### Wave Soldering

Conventional single wave soldering is not recommended for surface mount devices (SMDs) or printed−circuit boards with a high component density, as solder bridging and non−wetting can present major problems. To overcome these problems the double−wave soldering method was specifically developed.

If wave soldering is used the following conditions must be observed for optimal results:

- Use a double−wave soldering method comprising a turbulent wave with high upward pressure followed by a smooth laminar wave.
- For packages with leads on two sides and a pitch (e):
  - Larger than or equal to 1.27 mm, the footprint longitudinal axis is preferred to be parallel to the transport direction of the print−circuit board;
  - Smaller than 1.27 mm, the footprint longitudinal axis must be parallel to the transport direction of the printed−circuit board. The footprint must incorporate solder thieves at the downstream end.
- For packages with leads on four sides, the footprint must be placed at a 45° angle to the transport direction of the printed−circuit board. The footprint must incorporate solder thieves downstream and at the side corners.

During placement and before soldering, the package must be fixed with a droplet of adhesive. The adhesive can be applied by screen printing, pin transfer or syringe dispensing. The package can be soldered after the adhesive is cured. Typical dwell time is four seconds at 250°C. A mildly−activated flux will eliminate the need for removal of corrosive residues in most applications.

### Manual Soldering

Fix the component by first soldering two diagonally−opposite end leads. Use a low voltage (24 V or less) soldering iron applied to the flat part of the lead. Contact time must be limited to 10 seconds at up to 300°C.

When using a dedicated tool, all other leads can be soldered in one operation within two to five seconds between 270°C and 320°C.

**Table 7. Soldering Process**

| Package | Soldering Method | |
|---|---|---|
| | **Wave** | **Re−flow** (Note 9) |
| BGA, SQFP | Not suitable | Suitable |
| HLQFP, HSQFP, HSOP, HTSSOP, SMS | Not suitable (Note 10) | Suitable |
| PLCC (Note 11), SO, SOJ | Suitable | Suitable |
| LQFP, QFP, TQFP | Not recommended (Notes 11 and 12) | Suitable |
| SSOP, TSSOP, VSO | Not recommended (Note 13) | Suitable |

9. All SMD packages are moisture sensitive. Depending upon the moisture content, the maximum temperature (with respect to time) and body size of the package, there is a risk that internal or external package cracks may occur due to vaporization of the moisture in them (the so called popcorn effect). For details, refer to the dry pack information in the “Data Handbook IC26; Integrated Circuit Packages; Section: Packing Methods”.
10. These packages are not suitable for wave soldering as a solder joint between the printed−circuit board and heatsink (at bottom version) can not be achieved, and as solder may stick to the heatsink (on top version).
11. If wave soldering is considered, then the package must be placed at a 45° angle to the solder wave direction. The package footprint must incorporate solder thieves downstream and at the side corners.
12. Wave soldering is only suitable for LQFP, TQFP and QFP packages with a pitch (e) equal to or larger than 0.8 mm; it is definitely not suitable for packages with a pitch (e) equal or smaller than 0.65 mm.
13. Wave soldering is only suitable for SSOP and TSSOP packages with a pitch (e) equal to or larger than 0.65 mm; it is definitely not suitable for packages with a pitch (e) equal to or smaller than 0.5 mm.

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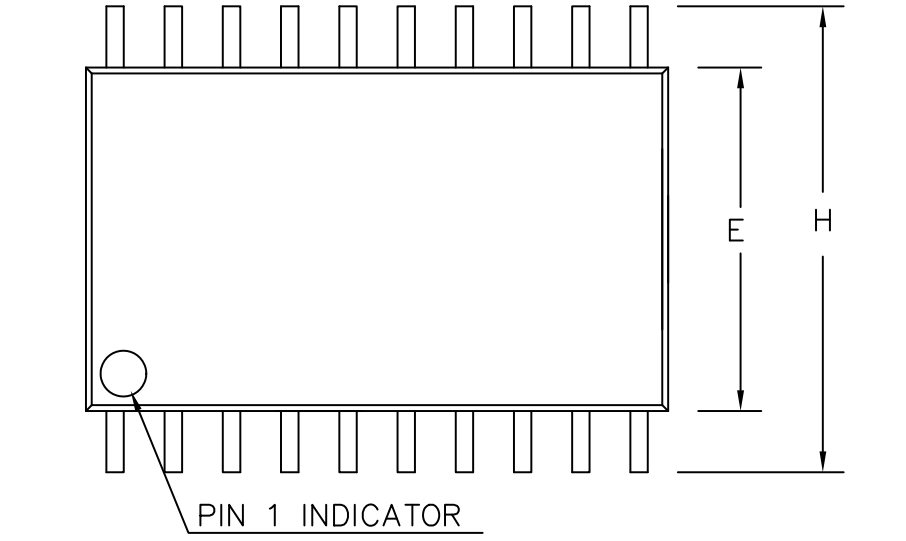


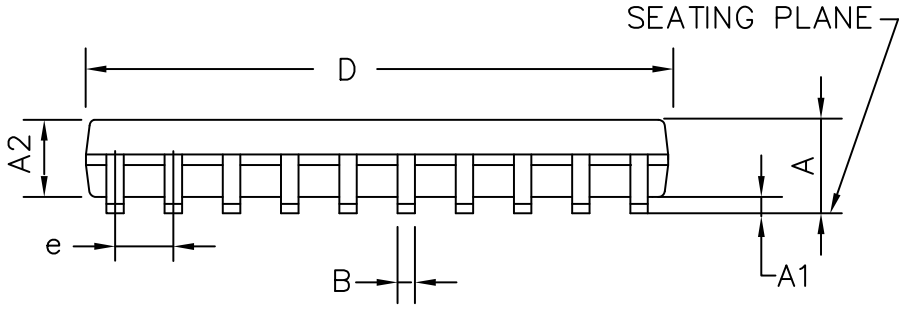


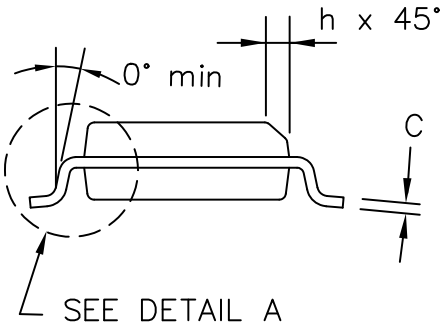


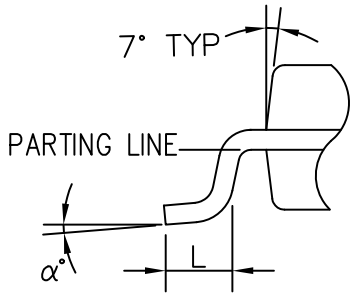


DETAIL A

| DIMENSIONS IN INCHES | | | |
|---|---|---|---|
| SYMBOL | MIN. | NOM. | MAX. |
| A | 0.093 | 0.099 | 0.104 |
| A1 | 0.004 | 0.008 | 0.012 |
| A2 | 0.088 | 0.094 | 0.100 |
| B | 0.013 | 0.016 | 0.020 |
| C | 0.0090 | 0.0100 | 0.0125 |
| D | 0.496 | 0.503 | 0.510 |
| E | 0.292 | 0.296 | 0.299 |
| e | .050 BSC. | | |
| H | 0.394 | 0.402 | 0.419 |
| h | 0.010 | 0.015 | 0.019 |
| L | 0.016 | 0.033 | 0.050 |
| α | 0° | 5° | 8° |

| | | |
|---|---|---|
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