

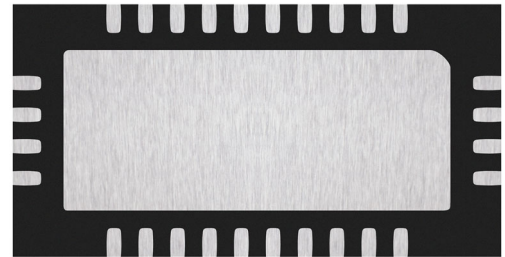
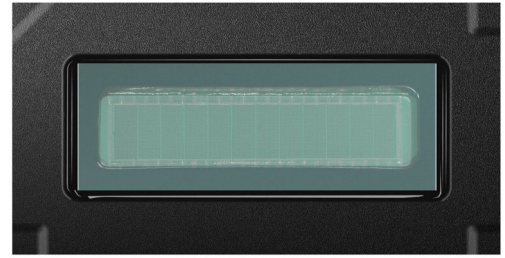
RDM-Series 1 x 12 SiPM Array

ArrayRDM-0112A20-QFN-TR (1)

The ArrayRDM-0112A20-QFN-TR(1) is a monolithic 1 × 12 array of Silicon Photomultiplier (SiPM) pixels based on the market-leading RDM process. The RDM process has been specifically developed to create products that give high PDE at the NIR wavelengths used for LiDAR and 3D ranging applications. For details of Automotive Qualification, please contact **onsemi**.

Table 1. KEY SENSOR AND PACKAGE SPECIFICATIONS

Parameter	Value	Comments
Silicon Process	RDM	
Number of Pixels	12	
Array Configuration	1 × 12	Monolithic silicon array
Pixel Size	1.12 × 0.47 mm	
Pixel Pitch	0.49 mm	
Microcell Size	20 μm	
Number of Microcells per Pixel	806	
Package Size	5.2 × 10.0 × 1.85 mm	W × L × H (see case outline on page 8 for more details)
Output Type	Analog	Standard output per pixel



The ArrayRDM-0112A20-QFN-TR Product
Case 485FZ

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 6 of this data sheet.

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Table 2. ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit	Comment
Maximum Overvoltage (Vov)	9	V	All temperatures
Maximum Current	20	mA	For entire array (12 channels) at recommended Vov
Maximum Storage Temperature	125	°C	
Functional Operating Temperature Range	-40 to 105	°C	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: $V_{op} = V_{br} + V_{ov}$. V_{br} is temperature dependent. V_{op} is also temperature dependent.

Table 3. ELECTRICAL SPECIFICATIONS

Parameter	-40°C		21°C		105°C		Unit
	Min	Max	Min	Max	Min	Max	
Breakdown Voltage (Vbr)	19.5	20.5	21.0	22.0	23.0	33.0	V

NOTES: V_{br} is defined as the intercept between the below-breakdown leakage current and the linear fit to the square root of the dark current above breakdown.

V_{br} is temperature dependent. At 105°C the V_{br} range within a lot will be 1 V. Refer to per lot data for exact range.

$V_{op} = V_{br} + V_{ov}$. V_{op} is also temperature dependent.

Table 4. BIASING SPECIFICATIONS

Parameter	Value	Unit	Comment
Recommended Overvoltage (Vov)	8	V	V_{ov} across full operating temperature range
Maximum Overvoltage (Vov)	9	V	All temperatures

NOTE: Operating bias voltage (V_{op}) = $V_{br} + V_{ov}$

Table 5. CALCULATED ELECTRICAL PARAMETERS

Parameter	Typical Value	Unit	Comment
Terminal Capacitance	20	pF	Per SiPM channel
Saturation Current (continuous)	2.8	mA	Per SiPM channel
Saturation Current (pulse)	6.2	mA	Per SiPM channel

NOTES: Terminal capacitance is calculated from Gain of a typical device at recommended V_{ov} .

Saturation current is calculated from Gain and recovery time of a typical device at recommended V_{ov} .

Table 6. PACKAGE SPECIFICATIONS

Parameter	Value	Unit	Comment
ESD – HBM	500	V	Class 1B
ESD – CDM	500	V	Class C2A
θ_{JC}	4	°C/W	Junction-to-Case thermal resistance is simulated with a heat sink at 25°C mounted on bottom of the package
θ_{JA}	58	°C/W	Junction-to-Ambient thermal resistance is simulated with a 1S0P test PCB according to JESD51-7 standard
MSL	4		All variants

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Table 7. TYPICAL SIPM PERFORMANCE SPECIFICATIONS

Parameter	Typical value at Vop		Unit
	Vop = 29.0 V	Vop = 30.0 V	
PDE @ 905 nm	15.6	16.8	%
Crosstalk	22	27	%
Thermal DCR per pixel	0.12	0.13	Mcps
Total DCR per pixel	0.13	0.14	Mcps
Delayed Crosstalk	7	9	%
1PE Level (via reference circuit)	47	54	mV
Gain	1.1x10 ⁶	1.2x10 ⁶	
Rise Time (20%–80%)	190	188	ps
Recovery Time (90%–10%)	49	51	ns

NOTE: Table shows typical performance parameters at 21°C.

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PIN ASSIGNMENT

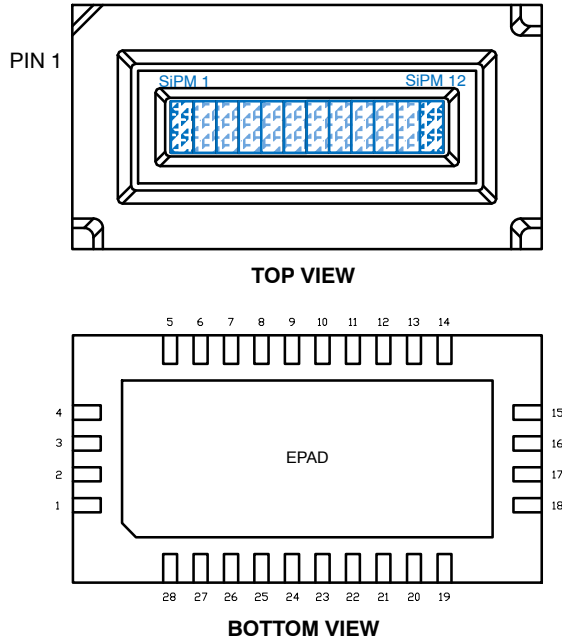


Figure 1. Device and Pin Numbering

Pin #	Pin Name	Pin Function
1	Cathode 1	SiPM 1 standard output
28	Cathode 2	SiPM 2 standard output
27	Cathode 3	SiPM 3 standard output
26	Cathode 4	SiPM 4 standard output
25	Cathode 5	SiPM 5 standard output
24	Cathode 6	SiPM 6 standard output
23	Cathode 7	SiPM 7 standard output
22	Cathode 8	SiPM 8 standard output
21	Cathode 9	SiPM 9 standard output
20	Cathode 10	SiPM 10 standard output
19	Cathode 11	SiPM 11 standard output
18	Cathode 12	SiPM 12 standard output
EPAD	Anode	Common Anode
2-17	NC	No Connect

APPLICATION ADVICE

The ArrayRDM-0112A20-QFN-TR(1) is formed of a linear array of 12 SiPM pixels. The QFN package provides a connection to each pixel cathode (for access to the individual signals) and a common anode. The common anode allows the provision of a single bias supply for all 12 pixels. The recommended test connections and biasing are as per the evaluation board that is detailed in the following section.

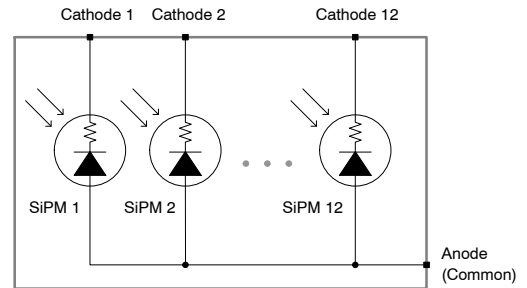


Figure 2. Array Schematic Showing Pixel Connections

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TYPICAL SiPM PERFORMANCE PLOTS

Below plots show the SiPM performance characteristics for a typical device at room temperature. For detailed characterization information please contact **onsemi**.

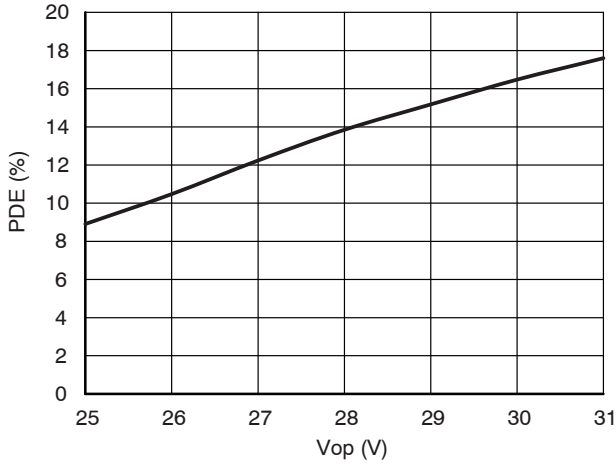


Figure 3. PDE at 905 nm vs. Bias Voltage

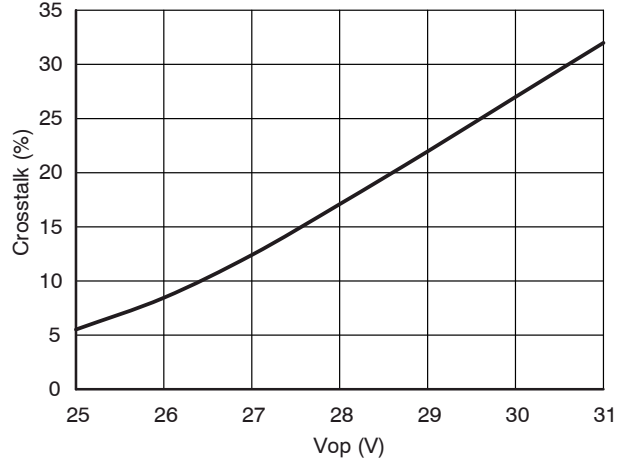


Figure 4. Crosstalk vs. Bias Voltage

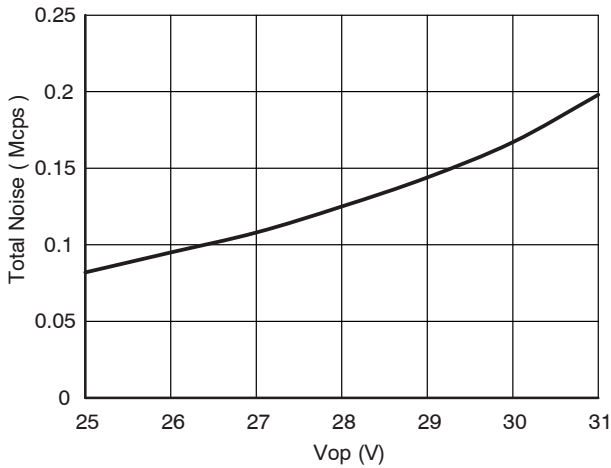


Figure 5. Total Noise (DCR per Channel) vs. Bias Voltage

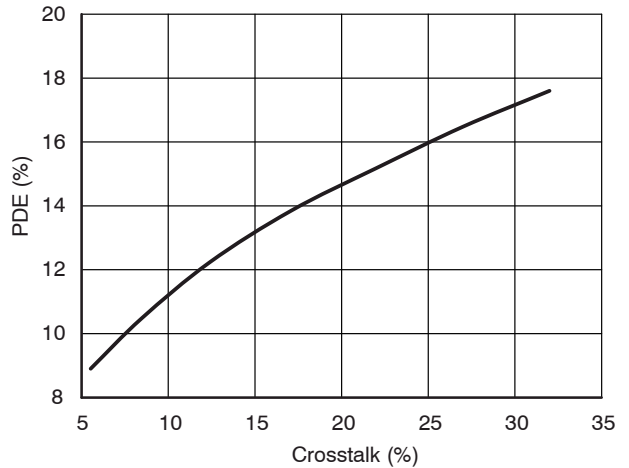


Figure 6. PDE at 905 nm vs. Crosstalk

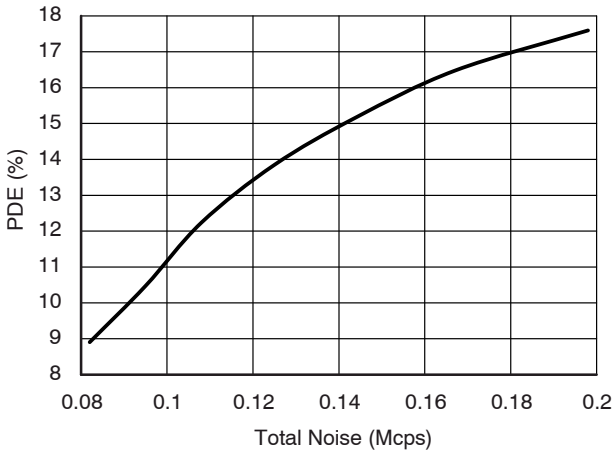


Figure 7. PDE at 905 nm vs. Total Noise (DCR per Channel)

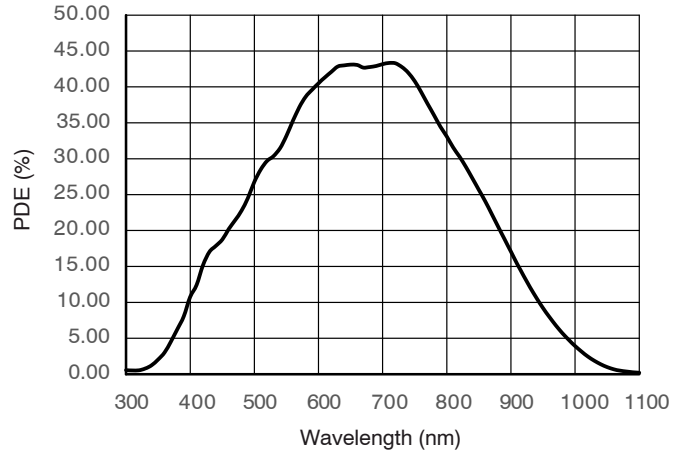


Figure 8. PDE vs Wavelength (21°C, Vop=29.5V)

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EVALUATION BOARD

The ArrayRDM-0112A20-GEVB evaluation board consists of:

- ArrayRDM-0112A20-QFN SiPM array
- 12 U.FL connectors for access to each pixel cathode for signal readout
- An SMA connector for applying the bias to the common anode
- Bias filtering circuit
- Decoupling capacitors (12 x 10 nF and 4 x 100 nF decoupling capacitors from anode to ground – not shown)

This product allows users to quickly and easily set up an evaluation of the array product.

Note that a negative bias supply should be supplied via the SMA connector (J13) and the U.FL connectors (J1 to J12) should be 50 Ω terminated.

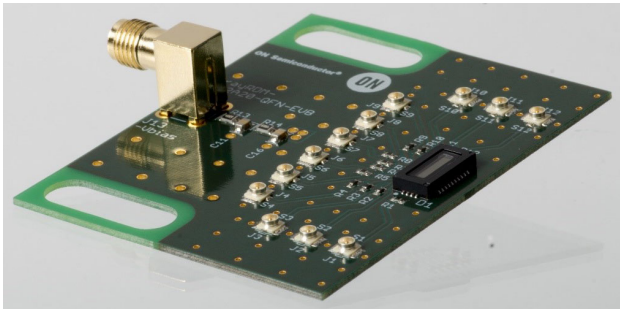


Figure 9. ArrayRDM-0112A20-GEVB Top Side View Showing the 1x12 Sensor

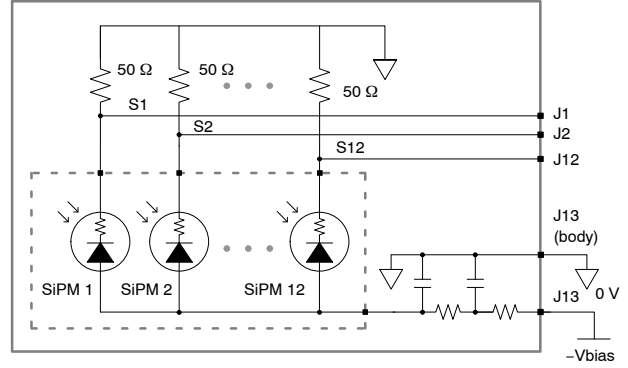


Figure 10. ArrayRDM-0112A20-GEVB Board Schematic

Connector	Style
J1–J12	U.FL Receptacle (Hirose U.FL-R-SMT)
J13	SMA Jack (F)

ORDERING INFORMATION

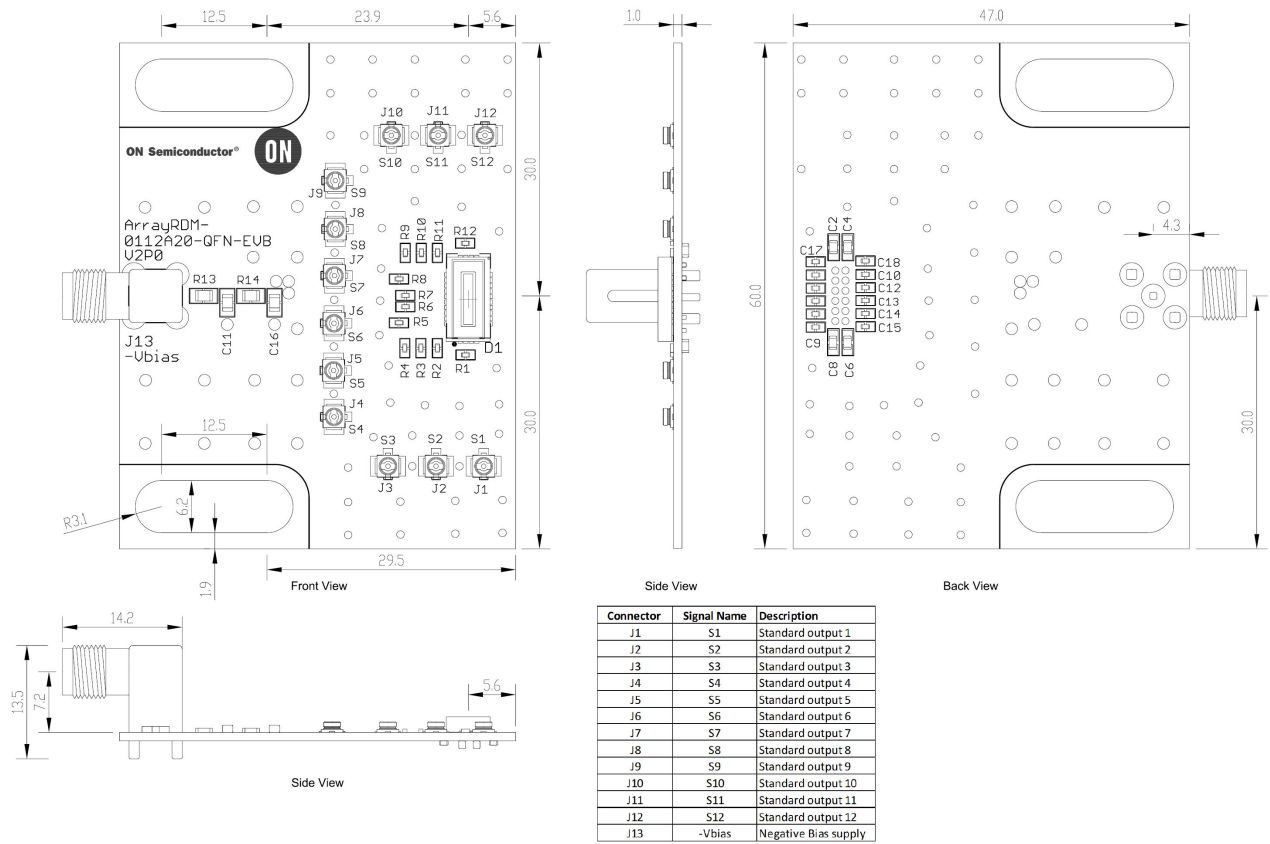
Table 8. ORDERING INFORMATION

Part Number	Product Description	Shipping Format
ArrayRDM-0112A20-QFN-TR	Monolithic 1 × 12 array of NIR sensitive SiPM pixels formed using the RDM process. Individual cathode connection per pixel and a common anode available via the 28-pin QFN package.	Tape and Reel
ArrayRDM-0112A20-QFN-TR1		Cut Tape
ArrayRDM-0112A20-QFN-TR-E	Prototype sample	Cut Tape
ArrayRDM-0112A20-GEVB	Evaluation board consisting of an ArrayRDM-0112A20-QFN mounted onto PCB. A U.FL connector gives access to each pixel cathode and fast output. The bias is supplied via an SMA connector to the common anode.	ESD Package

NOTE: For sample information please contact **onsemi**.

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EVALUATION BOARD DRAWING



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