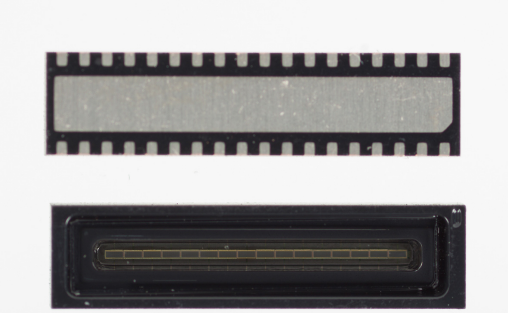
Silicon Photomultipliers (SiPM), RDM-Series 1 x 16 Monolithic Array

Product Preview

ArrayRDM-0116A10-DFN



The ARRAYRDM−0116A10−DFN Product

The ArrayRDM−0116A10−DFN is a monolithic 1 × 16 array of Silicon Photomultiplier (SiPM) pixels based on the market−leading RDM process. The RDM process has been specifically developed to create products that give high PDE at the NIR wavelengths used for LiDAR and 3D ranging applications.

In order to meet the requirements for automotive LiDAR applications, this product is intended to be qualified to the AEC−Q102 standard.

An evaluation board (ArrayRDM−0116A10−GEVB) will also be available for this product.

ORDERING INFORMATION

See detailed ordering and shipping information in the ordering information section on page 7 of this data sheet.

KEY SENSOR AND PACKAGE SPECIFICATIONS

Parameter	Value	Comment
Silicon Process	RDM	
Number of Pixels	16	
Array Configuration	1 × 16	
Pixel Size	0.17 × 0.49 mm	
Pixel Pitch	0.55 mm	
Microcell Size	10 μm	
Number of Microcells per Pixel	368	
Package Size	3 × 12 × 1.85 mm	DFN Package (W × L × H)
Output Type	Analog	Standard and Fast Output per Pixel

This document contains information on a product under development. **onsemi** reserves the right to change or discontinue this product without notice.

BIAS PARAMETERS

Parameter	Min	Typ	Max	Unit	Comment
Breakdown Voltage (Vbr)	–	21.7	–	V	
Over Voltage (Vov)	–	12.3	14.3	V	Typical value recommended for operation and used for characterization
Operating Bias (Vop)	Vop = Vbr + Vov				
Temperature Coefficient of Vbr	TBD			mV/°C	

ABSOLUTE MAXIMUM RATINGS

Parameter	Value	Unit	Comment
Maximum Bias	36	V	
Maximum Current	14	mA	For the whole array at Vop and 21°C
Maximum Storage Temperature	125	°C	
Operating Temperature Range	−40 to +105	°C	Ambient temperature

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

PACKAGE SPECIFICATIONS

Parameter	Value	Unit	Comment
ESD−HBM	TBD		
ESD−CDM	TBD		
θ_{JC}	4	°C/W	
θ_{JA}	245	°C/W	
MSL	3		For all part numbers

90% − 10% Recovery Time Parameter

The recovery time indicates the time taken for the microcells to recover to fully biased state. Recovery time is measured by applying a low power 905 nm 50 ps laser pulse at the SiPM and measuring the resulting pulse shape on the standard output. The 90% to 10 % recovery time is the time interval between the signal crossing the 90% threshold and the 10% threshold, relative to the peak amplitude. Note that recovery time will depend on a number of factors including the circuit. The circuit used for this measurement is pictured in Figure 1. Typical pulse shapes for both the standard and fast output, also using this circuit, are shown in Figure 2.

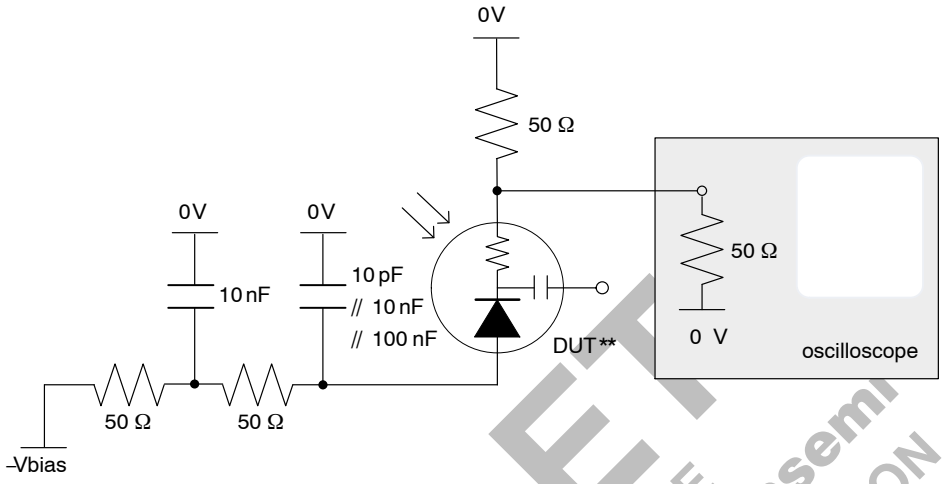


Figure 1. The Circuit used for Recovery Time Parameter Measurement

Note that any unused fast outputs should be directly connected to GND or terminated using a 50 Ω resistor to GND.

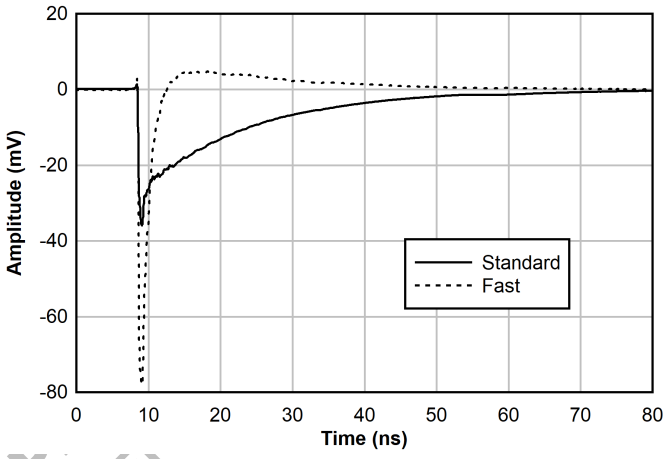


Figure 2. Pulse Shape

CONNECTION AND BOARD LAYOUT RECOMMENDATIONS

The ArrayRDM−0116A10−DFN is formed of a linear array of 16 SiPM pixels and housed in a 36−pin DFN package. Figure 3 shows the sensor array schematic. The signals from each pixel can be accessed either via the pixel cathode or fast output. The common anode is also available and allows the provision of a single bias supply for all 16 pixels. Note that any unused fast outputs should be connected to GND, or terminated using a 50 Ω resistor to GND.

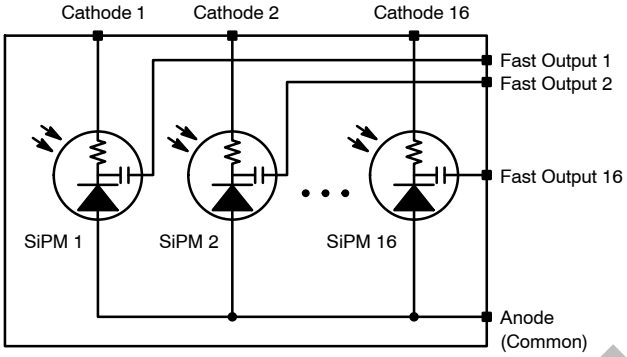


Figure 3. Array Schematic Showing Pixel Connections

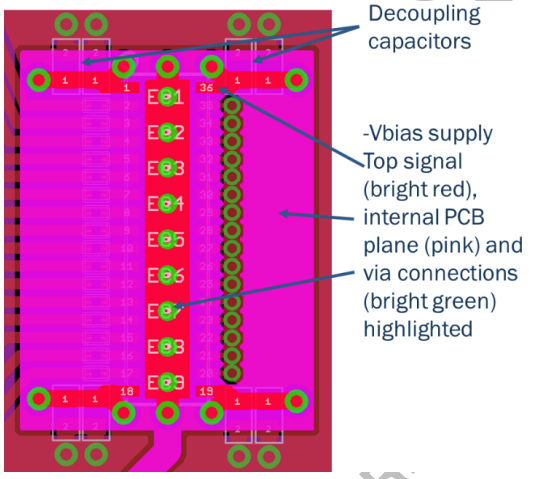


Figure 4.

The following recommendations for the bias are advised (see Figure 4):

- **onsemi** recommend the use of a negative bias supplied to the anode with cathode terminated to GND as illustrated in EVB schematic in Figure 7
- Use an internal power plane below the GND plane for the bias
- Place decoupling capacitors close to anode corner pins of the DFN (pins 1, 18, 19 & 36)
  - Pairs of 1 nF 100 V ceramic capacitors are recommended for systems where dynamic switching of bias is required
  - Higher capacitance can be used when static bias voltage is used eg 10 nF 100 V
- Use the EPAD contact to reduce the inductance of the bias supply connection to the SiPM array by using multiple plugged vias from the EPAD to the bias plane
- Decoupling capacitors should also be used on the back side of the PCB from the EPAD vias to GND when possible

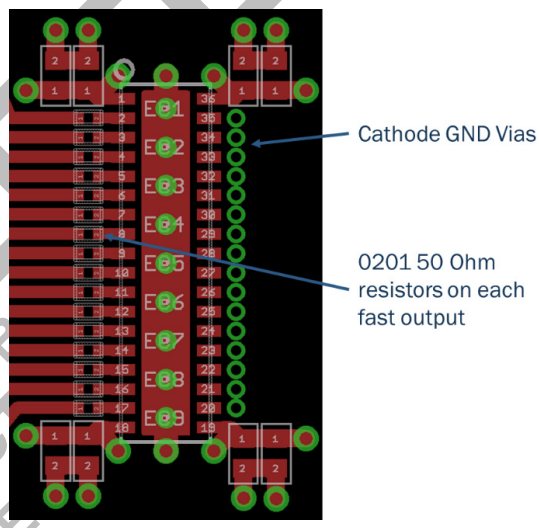


Figure 5.

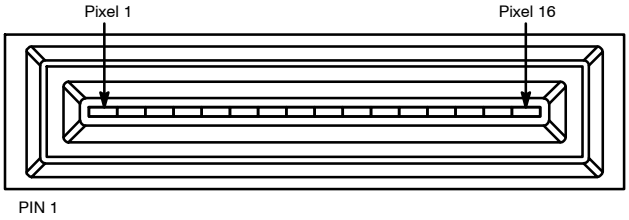
Recommendations for fast output:

- **Unused fast outputs should be directly connected to GND or terminated using a 50 Ω resistor to GND**. This is to avoid noise pickup and reflections from floating unterminated tracks.
- Avoid using only a capacitor to couple to fast outputs as this can lead to unwanted DC bias on the fast terminal network. At the input of the readout amplifier stage use resistive coupling to ground (50 Ω to 1 kΩ recommended) to avoid the floating condition of the fast output.
- Use series termination resistors close to the fast output pins (pins 2 to 17) of the Array (see Figure 5)
  - Helps to match the source impedance of the SiPM pixels to the PCB and amplifier load
  - Helps to reduce reflections of the high speed signals
  - 0201 package size resistors fit neatly beside each fast output pin
- GND cathodes near to each cathode pin (pins 20 to 35) using vias to GND plane when standard readout is not required

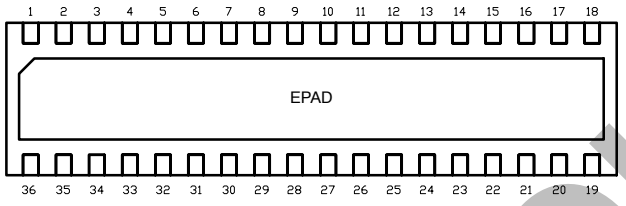
Recommendations for Signal Track Impedance:

- Match impedance of signal tracks to 50 Ω
- E.g. Use microstrip impedance where signals on the top layer of the PCB are above a ground plane on an internal layer of the PCB

PIN ASSIGNMENT



TOP VIEW



BOTTOM VIEW

Pin #	Pin Assignment	Pin #	Pin Assignment
1	Anode	19	Anode
2	Fast output 1	20	Cathode 16
3	Fast output 2	21	Cathode 15
4	Fast output 3	22	Cathode 14
5	Fast output 4	23	Cathode 13
6	Fast output 5	24	Cathode 12
7	Fast output 6	25	Cathode 11
8	Fast output 7	26	Cathode 10
9	Fast output 8	27	Cathode 9
10	Fast output 9	28	Cathode 8
11	Fast output 10	29	Cathode 7
12	Fast output 11	30	Cathode 6
13	Fast output 12	31	Cathode 5
14	Fast output 13	32	Cathode 4
15	Fast output 14	33	Cathode 3
16	Fast output 15	34	Cathode 2
17	Fast output 16	35	Cathode 1
18	Anode	36	Anode
EPAD	Anode		

Note that any unused fast outputs should be connected to GND or terminated via 50 Ω to GND.

EVALUATION BOARD

The ArrayRDM−0116A10−GEVB evaluation board is shown in Figure 6 and schematically (with pin outs) in Figure 7. The full drawing can be found on page 8. It consists of:

- ArrayRDM−0116A10−DFN 16−channel SiPM array
- 32 U.FL connectors for access to each pixel cathode and fast output for signal readout
- An SMA connector for applying the bias to the common anode
- Bias filtering circuit
- Decoupling capacitors (14 x 10 nF and 4 x 100 nF decoupling capacitors from anode to ground − not shown)

This product allows a user to quickly and easily set up an evaluation of the array product.

Note that a negative bias supply should be supplied via the SMA connector (J33), and the U.FL connectors (J1 to J32) should be 50 Ω terminated. Note that any unused fast outputs should be connected to GND or terminated using an 50 Ω resistor to GND, for example with an SMA terminator.

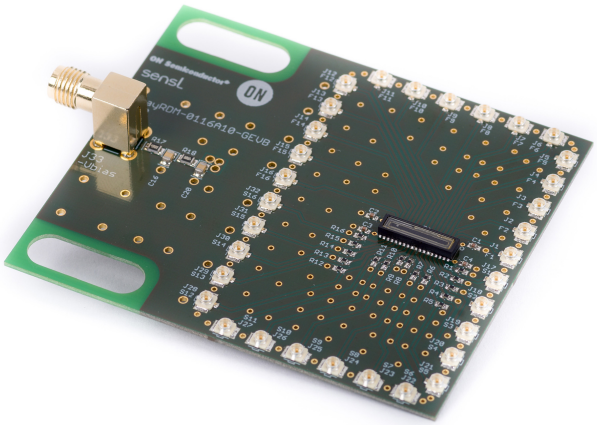
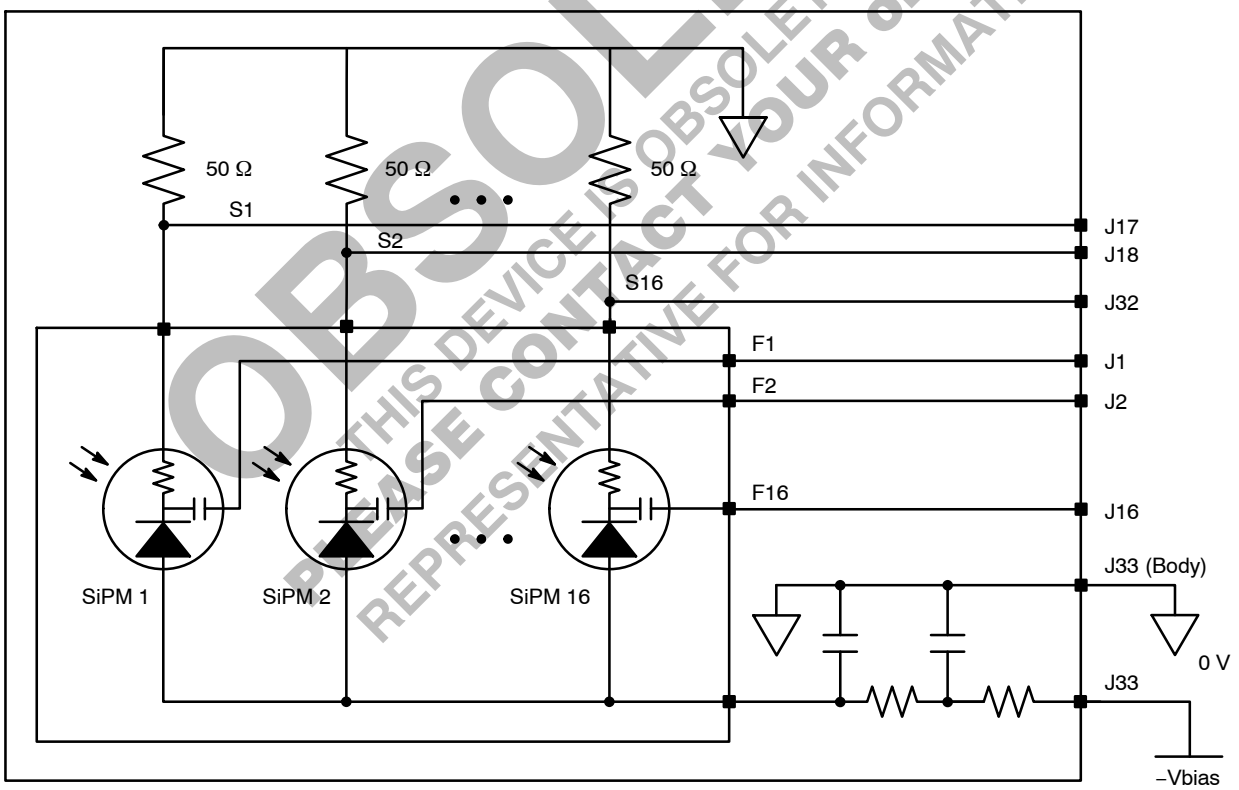


Figure 6. ArrayRDM−0116A10−GEVB Top Side View Showing the 1x16 Sensor Placement



Connector	Style
J1−J32	U.FL Receptacle (Hirose U.FL−R−SMT)
J33	SMA Jack (F)

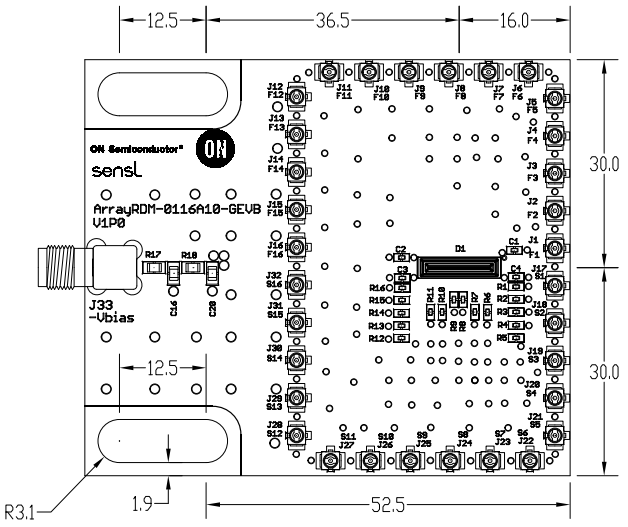
Figure 7. ArrayRDM−0116A10−GEVB Board Schematic

ORDERING INFORMATION

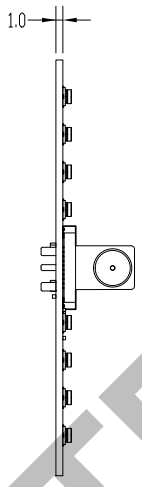
Part Number	Product Description	Shipping Format
ArrayRDM−0116A10−DFN−TR	Monolithic 1 × 16 array of NIR sensitive SiPM pixels formed using the RDM process. Individual cathode and fast output connection per pixel and a common anode available via the 36−pin DFN package.	Tape and Reel
ArrayRDM−0116A10−DFN−TR1		Cut Tape
ArrayRDM−0116A10−GEVB	Evaluation board consisting of an ArrayRDM−0116A10−DFN mounted onto PCB. A U.FL connector gives access to each pixel cathode and fast output. The bias is supplied via an SMA connector to the common anode.	ESD Package

For any queries please visit https://www.onsemi.com/support/technical−support

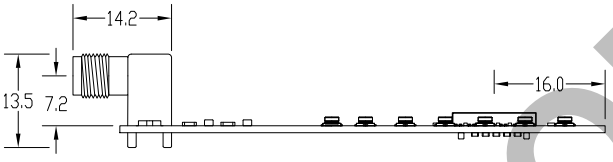
EVALUATION BOARD DIMENSIONS



Front View



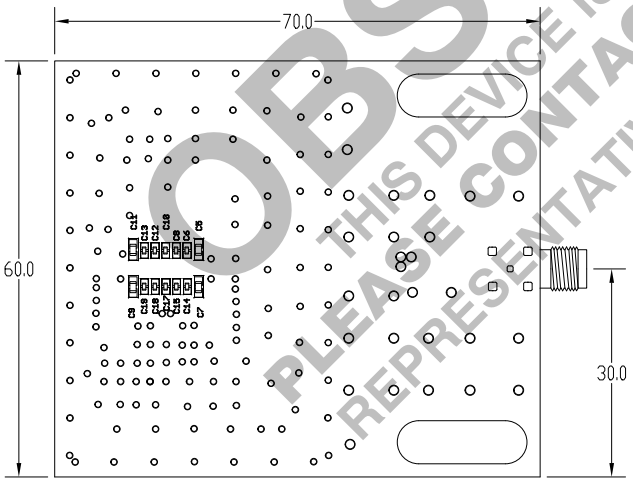
Side View



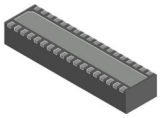
Side View

Connector	Signal Name	Description	Connector	Signal Name	Description
J1	F1	Fast Output 1	J17	S1	Standard Output 1
J2	F2	Fast Output 2	J18	S2	Standard Output 2
J3	F3	Fast Output 3	J19	S3	Standard Output 3
J4	F4	Fast Output 4	J20	S4	Standard Output 4
J5	F5	Fast Output 5	J21	S5	Standard Output 5
J6	F6	Fast Output 6	J22	S6	Standard Output 6
J7	F7	Fast Output 7	J23	S7	Standard Output 7
J8	F8	Fast Output 8	J24	S8	Standard Output 8
J9	F9	Fast Output 9	J25	S9	Standard Output 9
J10	F10	Fast Output 10	J26	S10	Standard Output 10
J11	F11	Fast Output 11	J27	S11	Standard Output 11
J12	F12	Fast Output 12	J28	S12	Standard Output 12
J13	F13	Fast Output 13	J29	S13	Standard Output 13
J14	F14	Fast Output 14	J30	S14	Standard Output 14
J15	F15	Fast Output 15	J31	S15	Standard Output 15
J16	F16	Fast Output 16	J32	S16	Standard Output 16
			J33	-Vbias	Negative Bias Supply

Pinout Table

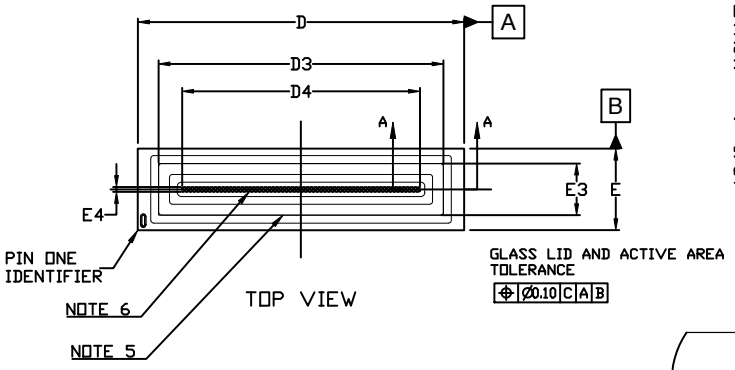


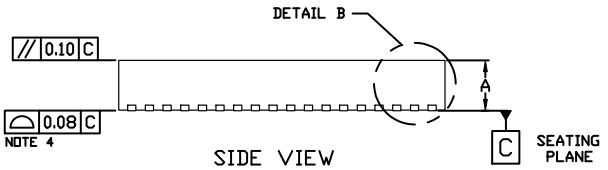
Back View

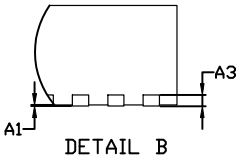


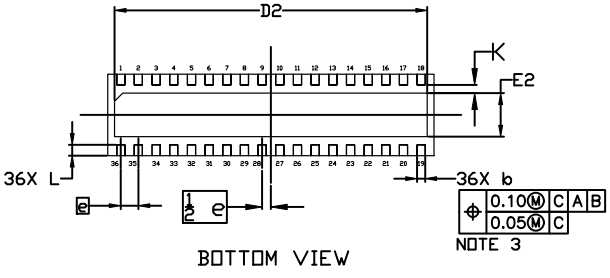
DFN36 12x3, 0.65P
CASE 506EV
ISSUE A

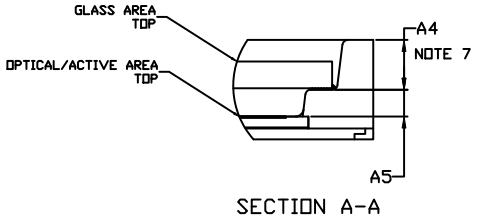
DATE 11 DEC 2020





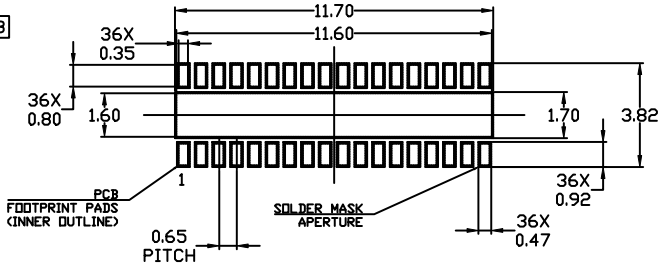






NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. GLASS LID AREA, 0.4mm THICKNESS. DEFINED BY D3 & E3.
6. OPTICAL/ACTIVE AREA IS CENTERED.
7. GLASS LID PLACEMENT. OUTER FLAT AREA APPROXIMATELY SIMILAR TO LID WIDTH AND LENGTH.

	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	1.75	1.85	1.95
A1	0.00	---	0.05
A3		0.203 REF	
A4		0.927 REF	
A5		0.500 REF	
b	0.25	0.30	0.35
D	11.90	12.00	12.10
D2	11.40	11.50	11.60
D3		10.47 REF	
D4		8.753 REF	
E	2.90	3.00	3.10
E2	1.50	1.60	1.70
E3		1.90 REF	
E4		0.18 REF	
e		0.65 BSC	
K	0.10	---	---
L	0.35	0.40	0.45



* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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DESCRIPTION:	**DFN36 12x3, 0.65P**	**PAGE 1 OF 1**

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