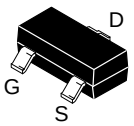
Field Effect Transistor – N-Channel, Logic Level, Enhancement Mode

BSS138L



SOT−23 (TO−236)
CASE 318

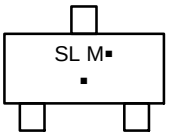
Description

This N−channel enhancement mode field effect transistor is produced using high cell density, trench MOSFET technology. This product minimizes on−state resistance while providing rugged, reliable, and fast switching performance. This product is particularly suited for low−voltage, low−current applications such as small servo motor control, power MOSFET gate drivers, logic level translator, high speed line drivers, power management/power supply and switching applications.

Features

- High Density Cell Design for Low $R_{DS(ON)}$
- Rugged and Reliable
- Compact Industry Standard SOT−23 Surface Mount Package
- Very Low Capacitance
- Fast Switching Speed
- This Device is Pb−Free, Halide Free and is RoHS Compliant

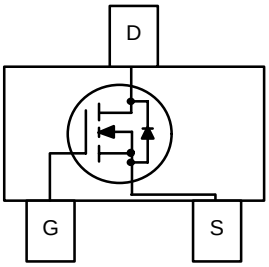
MARKING DIAGRAM



SL = Specific Device Code
M = Date Code*
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*Date Code orientation and/or overbar may vary depending upon manufacturing location.



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter		Value	Unit
V_{DSS}	Drain−Source Voltage		50	V
V_{GSS}	Gate−Source Voltage		±20	V
I_D	Maximum Drain Current	Continuous	0.20	A
		Pulsed	0.80	A
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C
T_L	Maximum Lead Temperature for Soldering Purposes, 1/16 inch from Case for 10 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS (T_A = 25°C, unless otherwise noted)

Symbol	Parameter	Value	Unit
P_D	Maximum Power Dissipation (Note 1)	0.35	W
	Derate Above 25°C	2.8	mW/°C
$R_{\theta JA}$	Thermal Resistance, Junction−to−Ambient (Note 1)	380	°C/W

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

a) 380°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

ORDERING INFORMATION

Device	Package	Shipping†
BSS138L	SOT−23 (TO−236) (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

ESD RATING (Note 2)

Symbol	Parameter	Value	Unit
HBM	Human Body Model per ANSI/ESDA/JEDEC JS−001−2012	50	V
CDM	Charged Device Model per JEDEC C101C	>2000	

2. ESD values are in typical, no over−voltage rating is implied, ESD CDM zap voltage is 2000 V maximum.

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain−Source Breakdown Voltage	V_{GS} = 0 V, I_D = 250 μA	50.0	65.4	−	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	−	58	−	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 50 V, V_{GS} = 0 V	−	0.263	500	nA
		V_{DS} = 50 V, V_{GS} = 0 V, T_J = 125°C	−	0.109	5	μA
		V_{DS} = 30 V, V_{GS} = 0 V	−	0.062	100	nA
I_{GSSF}	Gate−Body Leakage, Forward	V_{GS} = 20 V, V_{DS} = 0 V	−	0.058	100	nA
I_{GSSR}	Gate−Body Leakage, Reverse	V_{GS} = −20 V, V_{DS} = 0 V	−	−0.06	−100	
ON CHARACTERISTICS (Note 3)						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = 1 mA	0.80	1.25	1.50	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate Threshold Voltage Temperature Coefficient	I_D = 1 mA, Referenced to 25°C	−	−2.42	−	mV/°C
$R_{DS(ON)}$	Static Drain−Source On−Resistance	V_{GS} = 5 V, I_D = 0.20 A	−	2.78	3.50	Ω
		V_{GS} = 2.75 V, I_D = 0.20 A	−	3.78	10	
$I_{D(ON)}$	On−State Drain Current	V_{GS} = 10 V, V_{DS} = 5 V	0.20	0.67	−	A
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 0.22 A	0.12	0.35	−	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1.0 MHz	−	12.2	50	pF
C_{oss}	Output Capacitance		−	3.04	25	pF
C_{rss}	Reverse Transfer Capacitance		−	1.43	5	pF
R_G	Gate Resistance	V_{GS} = 15 V, V_{GS} = 1.0 MHz	−	26.6	−	Ω
SWITCHING CHARACTERISTICS (Note 3)						
$t_{d(on)}$	Turn−On Delay	V_{DD} = 30 V, I_D = 0.29 A, V_{GS} = 10 V	−	2.2	5	ns
t_r	Turn−On Rise Time		−	1.8	18	ns
$t_{d(off)}$	Turn−Off Delay		−	5.3	36	ns
t_f	Turn−Off Fall Time		−	5.1	14	ns
Q_g	Total Gate Charge	V_{DS} = 25 V, I_D = 0.22 A, V_{GS} = 10 V, I_G = 0.1 mA	−	0.549	2.4	nC
Q_{gs}	Gate−Source Charge		−	0.075	−	nC
Q_{gd}	Gate−Drain Charge		−	0.117	−	nC
DRAIN−SOURCE CHARACTERISTICS AND MAXIMUM RATINGS						
I_S	Maximum Continuous Drain−Source Diode Forward Current		−	−	0.22	A
V_{SD}	Drain−Source Diode Forward Voltage	V_{GS} = 0 V, I_S = 115 mA	−	0.93	1.4	V

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2.0%.

TYPICAL PERFORMANCE CHARACTERISTICS

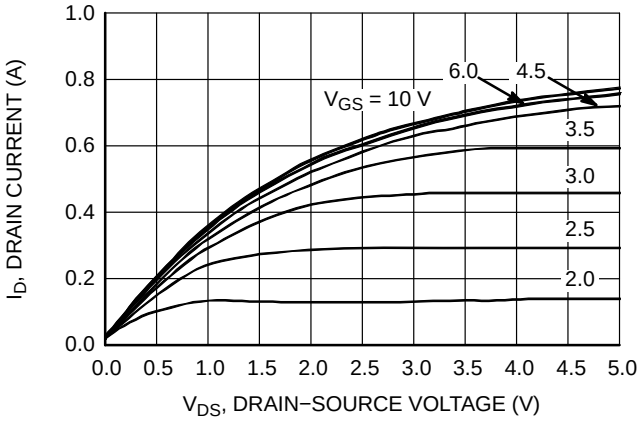


Figure 1. On−Region Characteristics

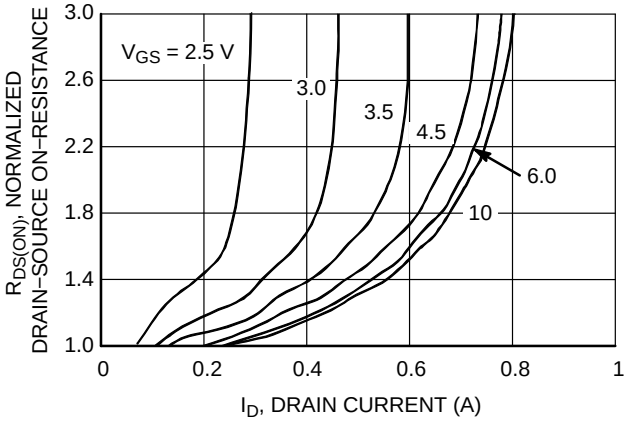


Figure 2. On−Resistance Variation with Gate Voltage and Drain Current

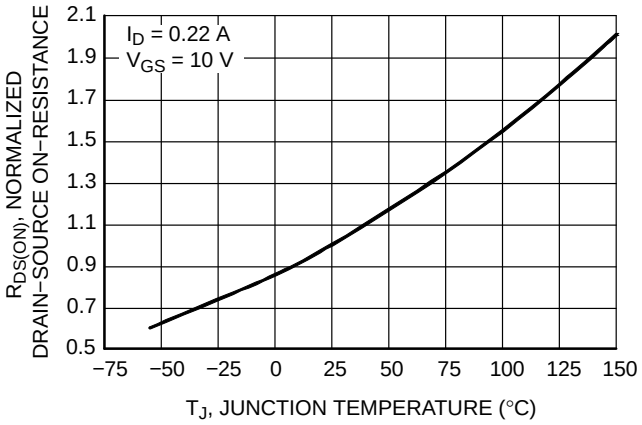


Figure 3. On−Resistance Variation with Temperature

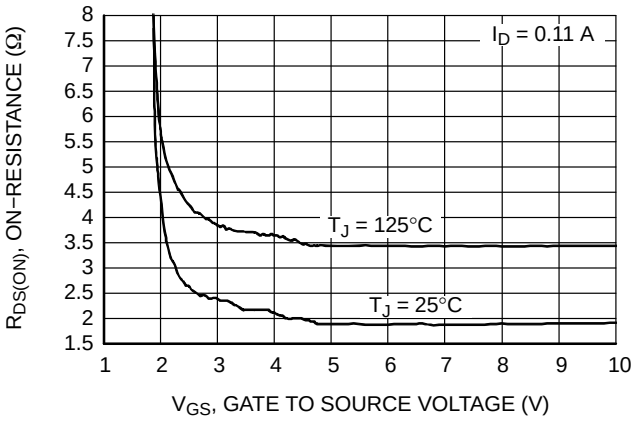


Figure 4. On−Resistance Variation with Gate−to−Source Voltage

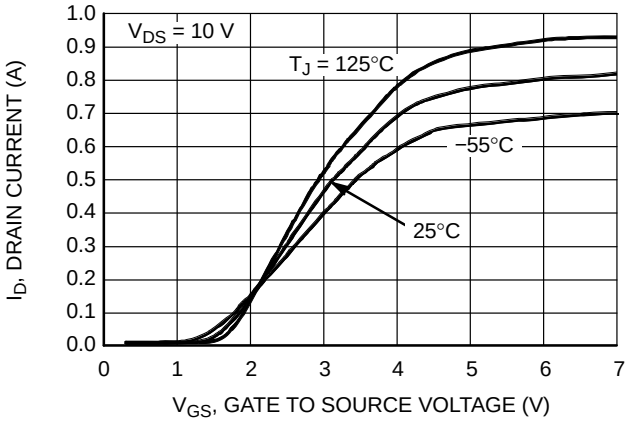


Figure 5. Transfer Characteristics

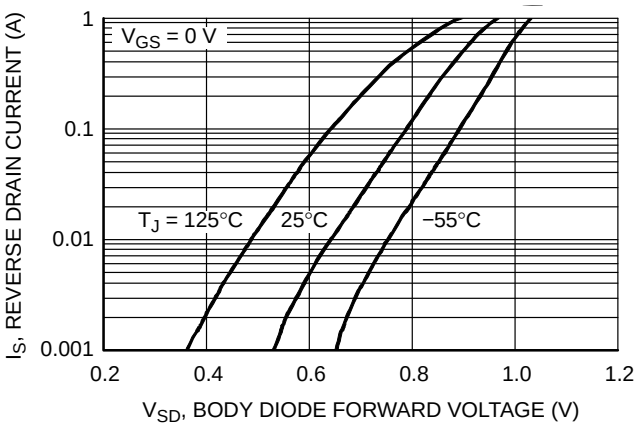


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

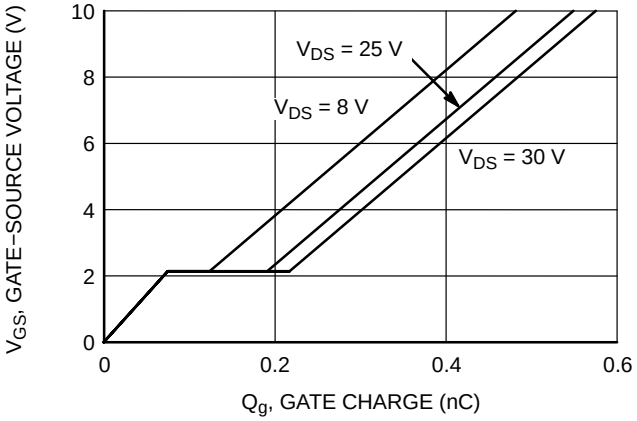


Figure 7. Gate Charge Characteristics

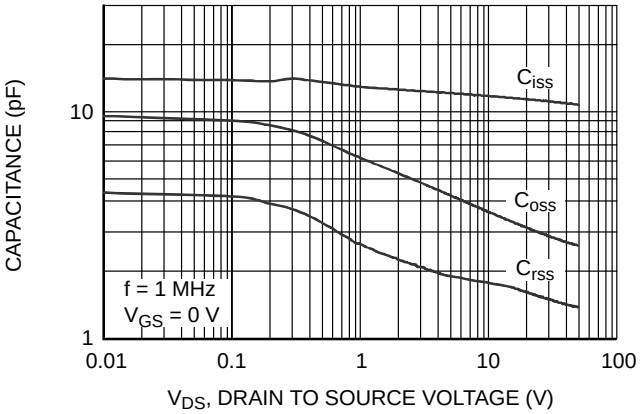


Figure 8. Capacitance Characteristics

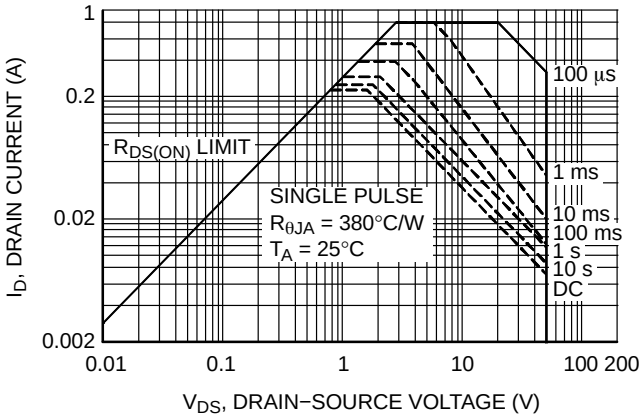


Figure 9. Maximum Safe Operating Area

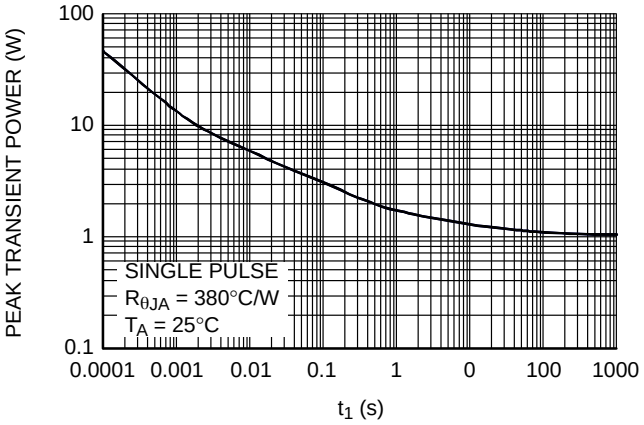


Figure 10. Single Pulse Maximum Power Dissipation

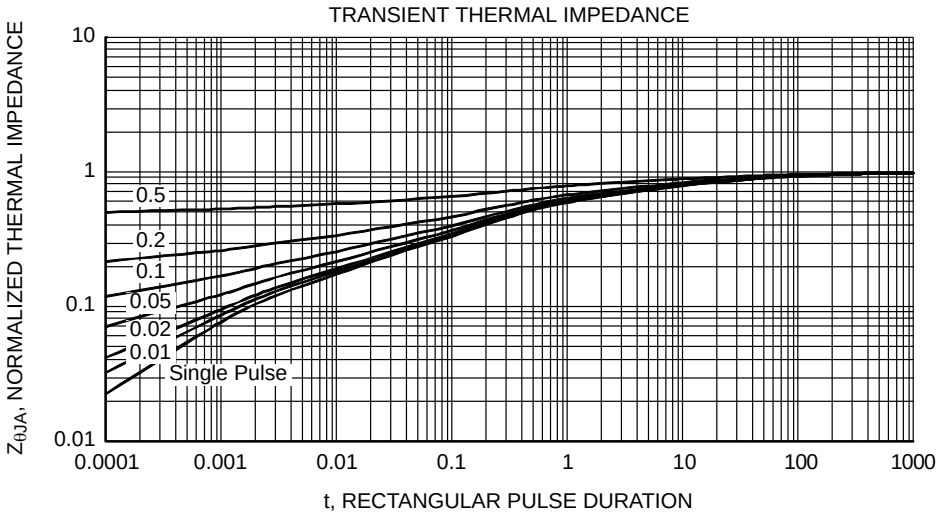


Figure 11. Transient Thermal Response Curve

ADDITIONAL INFORMATION

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