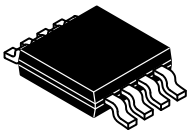
Single Channel 256 Tap Digital Potentiometer (POT) with Integrated EEPROM and I²C Control

CAT5140



MSOP8 3x3
Z SUFFIX
CASE 846AQ

The CAT5140 is a single channel non-volatile 256-tap digital POT. This digital POT is comprised of a series of equal value resistor elements connected between two externally accessible end points. The tap points between each resistive element can be selectively connected to the wiper output via internal CMOS switches forming a linear taper electronic potentiometer.

The CAT5140 contains a volatile wiper register (WR) and an 8-bit non-volatile EEPROM for wiper position and 5 additional non-volatile registers for general purpose data storage. Programming of the registers is controlled via I²C interface. On power up, the wiper position is reset to the most recent value stored in the non-volatile memory register (IVR).

The CAT5140 is available in an Pb free, RoHS compliant 8-lead MSOP package, and operates over the industrial temperature range of −40°C to +85°C.

Features

- 400 kHz I²C Compatible Interface
- 256 Position Linear Taper Potentiometer
- End-to-End Resistance = 50 kΩ / 100 kΩ
- TCR = 100 ppm/°C (typical)
- Standby Current = 2 μA (max)
- Typical Wiper Resistance = 70 Ω @ 3.3 V
- Operating Voltage = 2.5 V to 5.5 V
- 6 Registers 8-bit Non-volatile EEPROM
- 2,000,000 Data Write Stores
- 100 Year Data Retention
- 8-lead MSOP Package
- NiPdAu Plating
- These Devices are Pb-Free and are RoHS Compliant

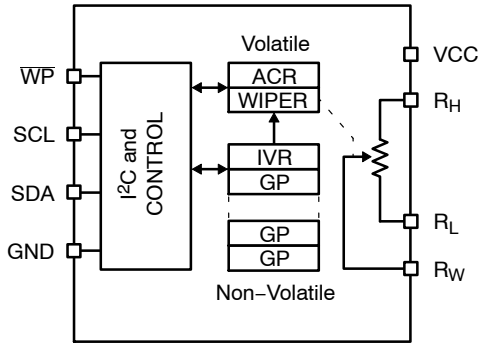
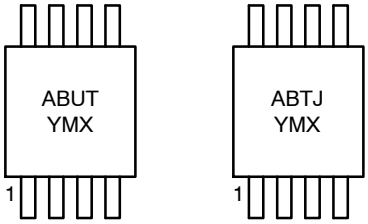


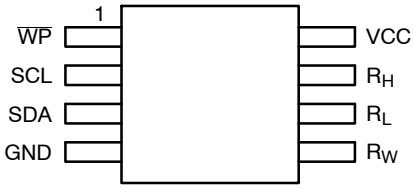
Figure 1. Functional Block Diagram

MARKING DIAGRAM



ABUT = 100 kΩ Resistance
ABTJ = 50 kΩ Resistance
Y = Production Year
(Last Digit)
M = Production Month
(1 – 9, A, B, C)
X = Production Revision

PIN CONNECTIONS



(Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

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Table 1. ORDERING INFORMATION

Part Number	Resistance	Temperature Range	Package	Shipping†
CAT5140ZI−50−GT3	50 kΩ	−40°C to 85°C	MSOP−8 3x3 (Pb-Free)	3000/Tape & Reel
CAT5140ZI−00−GT3	100 kΩ			3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

1. For detailed information and a breakdown of device nomenclature and numbering systems, please see the ON Semiconductor Device Nomenclature document, TND310/D, available at www.onsemi.com.

Table 2. PIN FUNCTION DESCRIPTION

Pin No.	Pin Name	Description
1	$\overline{WP}$	Memory Write Protect: Active Low
2	SCL	Serial Clock
3	SDA	Serial Data
4	GND	Ground
5	R_W	Wiper Terminal
6	R_L	Potentiometer Low Terminal
7	R_H	Potentiometer High Terminal
8	V_{CC}	Supply Voltage

$\overline{WP}$: Write Protect Input

The $\overline{WP}$ pin when tied low prevents any write operations within the device.

SCL: Serial Clock

The CAT5140 serial clock input pin is used to clock all data transfers into or out of the device.

SDA: Serial Data

The CAT5140 bidirectional serial data pin is used to transfer data into and out of the device. The SDA pin is an open drain output and can be wire-Ored with the other open drain or open collector I/Os.

R_H, R_L: Resistor End Points

The set of R_H and R_L pins is equivalent to the terminal connections on a mechanical potentiometer.

R_W: Wiper

The R_W pin is equivalent to the wiper terminal of a mechanical potentiometer and its position is controlled by the WR register.

Table 3. ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
V_{IN} Supply Voltage V_{CC} to Ground (Note 2)	−0.5 to +7	V
Terminal voltages: R_H, R_L, R_W , SDA, SCL, $\overline{WP}$	−0.5 to V_{CC} + 0.5	V
Wiper Current	±6.0	mA
Storage Temperature Range	−65 to +150	°C
Junction Temperature Range	−40 to +150	°C
Lead Soldering Temperature (10 seconds)	300	°C
ESD Rating HBM (Human Body Model)	2000	V
ESD Rating MM (Machine Model)	200	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. The minimum DC input voltage is −0.5 V. During transitions, inputs may undershoot to −2.0 V for periods of less than 20 ns. Maximum DC voltage on output pins is V_{CC} +0.5 V, which may overshoot to V_{CC} +2.0 V for periods of less than 20 ns.

Table 4. RECOMMENDED OPERATING CONDITIONS

Parameter	Rating	Unit
V_{CC}	2.5 to 5.5	V
Wiper Current	±3	mA
Temperature Range	−40 to +85	°C

Table 5. POTENTIOMETER CHARACTERISTICS (Note 3) (V_{CC} = +2.5 V to +5.5 V, −40°C to +85°C unless otherwise specified.)

Parameter	Test Conditions	Symbol	Limits			Units
			Min	Typ	Max	
Potentiometer Resistance '−50'		R_{POT}		50		kΩ
Potentiometer Resistance '−00'		R_{POT}		100		kΩ
Potentiometer Resistance Tolerance					±20	%
Power Rating	25°C				50	mW
Wiper Current		I_W			±3	mA
Wiper Resistance	I_W = ±3 mA V_{CC} = 3.3 V	R_W		70	200	Ω
Integral Non-Linearity	Voltage Divider Mode	INL			±1	LSB (Note 4)
Differential Non-Linearity		DNL			±0.5	LSB (Note 4)
Integral Non-Linearity	Resistor Mode	RINL			±1	LSB (Note 4)
Differential Non-Linearity		RDNL			±0.5	LSB (Note 4)
Voltage on R_H or R_L	V_{SS} = 0 V	V_{TERM}	V_{SS}		V_{CC}	V
Resolution				0.4		%
Zero Scale Error			0	0.5	2	LSB (Note 5)
Full Scale Error			−2	−0.5	0	LSB (Note 5)
Temperature Coefficient of R_{POT}	(Notes 6, 7)	TC_{RPOT}		±100		ppm/°C
Ratiometric Temp. Coefficient	(Notes 6, 7)	TC_{RATIO}			20	ppm/°C
Potentiometer Capacitances	(Notes 6, 7)	$C_H/C_L/C_W$		10/10/25		pF
Frequency Response	R_{POT} = 50 kΩ (Note 8)	fc		0.4		MHz

3. Latch-up protection is provided for stresses up to 100 mA on address and data pins from −1 V to V_{CC} +1 V.
4. LSB = R_{TOT} / 255 or (R_H − R_L) / 255, single pot.
5. $V(R_W)_{255}-V(R_W)_0]/255$ $(R_W)_{255}$ = 0xFF, $(R_W)_0$ = 0x00.
6. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
7. Relative linearity is a measure of the error in step size. It is determined by the actual change in voltage between two successive tap positions when used as a potentiometer.
8. This parameter is tested initially and after a design or process change that affects the parameter.

Table 6. D.C. OPERATING CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V, −40°C to +85°C unless otherwise specified.)

Parameter	Test Conditions	Symbol	Min	Max	Units
Power Supply Current Volatile Write & Read	f_{SCL} = 400 kHz V_{CC} = 5.5 V, Inputs = GND	I_{CC1}		1	mA
Power Supply Current Non-volatile Write	f_{SCL} = 400 kHz V_{CC} = 5.5 V, Inputs = GND	I_{CC2}		3	mA
Standby Current	V_{CC} = 5.0 V	I_{SB}		2	μA
Input Leakage Current	V_{IN} = GND to V_{CC}	I_{LI}	−10	+10	μA
Output Leakage Current	V_{OUT} = GND to V_{CC}	I_{LO}		10	μA
Input Low Voltage		V_{IL}	−1	V_{CC} x 0.3	V
Input High Voltage		V_{IH}	V_{CC} x 0.7	V_{CC} + 1.0	V
SDA Output Buffer Low Voltage	V_{CC} = 2.5 V, I_{OL} = 4 mA	V_{OL1}		0.4	V
Power-On Recall	Minimum V_{CC} for memory recall	V_{POR}	1.4	2.0	V

Table 7. CAPACITANCE (T_A = 25°C, f = 1.0 MHz, V_{CC} = 5 V)

Test	Test Conditions	Symbol	Max	Units
Input/Output Capacitance (SDA)	$V_{I/O}$ = 0 V	$C_{I/O}$ (Note 9)	8	pF
Input Capacitance (SCL, $\overline{WP}$)	V_{IN} = 0 V	C_{IN} (Note 9)	6	pF

Table 8. POWER UP TIMING (Notes 9 and 10)

Parameter	Symbol	Max	Units
Power-up to Read Operation	t_{PUR}	1	ms
Power-up to Write Operation	t_{PUW}	1	ms

9. This parameter is tested initially and after a design or process change that affects the parameter.
10. t_{PUR} and t_{PUW} are delays required from the time V_{CC} is stable until the specified operation can be initiated.

Table 9. DIGITAL POT TIMING

Parameter	Symbol	Min	Max	Units
Wiper Response Time After Power Supply Stable	t_{WRPO}		50	μs
Wiper Response Time: SCL falling edge after last bit of wiper position data byte to wiper change	t_{WR}		20	μs

Table 10. ENDURANCE

Parameter	Reference Test Method	Symbol	Min	Max	Units
Endurance	MIL−STD−883, Test Method 1033	N_{END}	2,000,000		Cycles
Data Retention	MIL−STD−883, Test Method 1008	T_{DR}	100		Years

Table 11. A.C. CHARACTERISTICS (V_{CC} = +2.5 V to +5.5 V, −40°C to +85°C unless otherwise specified.)

Parameter	Symbol	Min	Typ	Max	Units
Clock Frequency	f_{SCL}			400	kHz
Clock High Period	t_{HIGH}	600			ns
Clock Low Period	t_{LOW}	1300			ns
Start Condition Setup Time (for a Repeated Start Condition)	$t_{SU:STA}$	600			ns
Start Condition Hold Time	$t_{HD:STA}$	600			ns
Data in Setup Time	$t_{SU:DAT}$	100			ns
Data in Hold Time	$t_{HD:DAT}$	0			ns
Stop Condition Setup Time	$t_{SU:STO}$	600			ns
Time the bus must be free before a new transmission can start	t_{BUF}	1300			ns
$\overline{WP}$ Setup Time	$t_{SU:WP}$	0			μs
$\overline{WP}$ Hold Time	$t_{HD:WP}$	2.5			μs
SDA and SCL Rise Time	t_R			300	ns
SDA and SCL Fall Time	t_F			300	ns
Data Out Hold Time	t_{DH}		100		ns
Noise Suppression Time Constant at SCL, SDA Inputs	T_I			50	ns
SLC Low to SDA Data Out and ACK Out	t_{AA}			1	μs
Non-Volatile Write Cycle Time	t_{WR}		4	10	ms

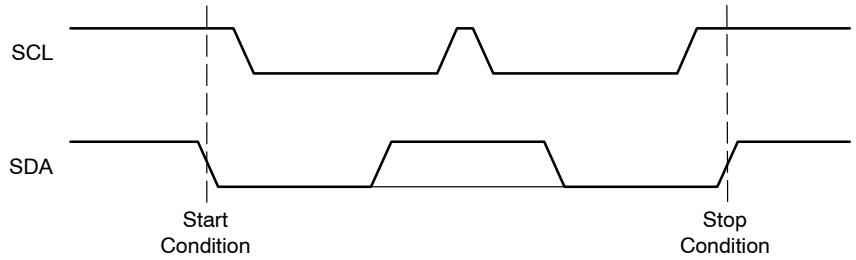


Figure 2. Start and STOP Timing

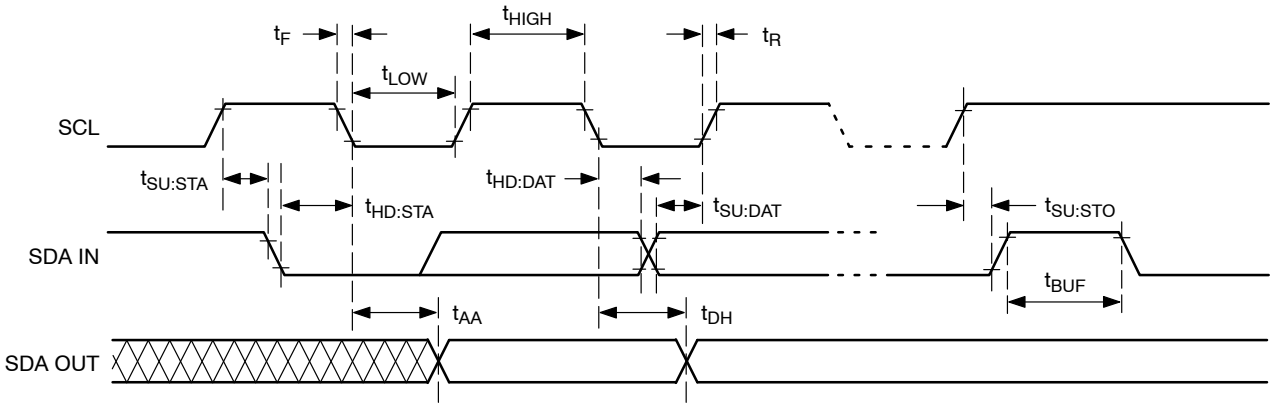


Figure 3. Bus Timing

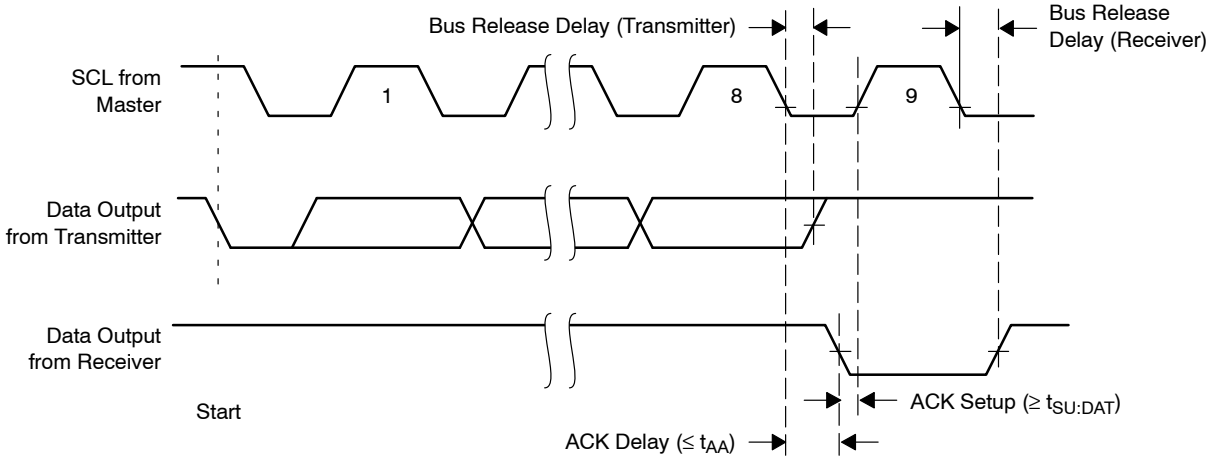


Figure 4. Acknowledge Timing

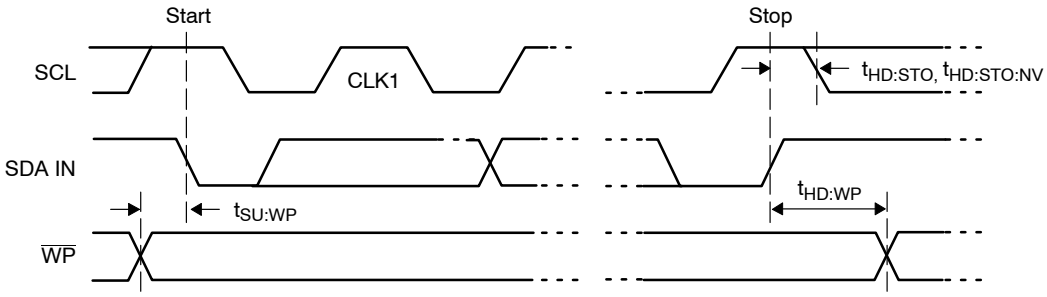
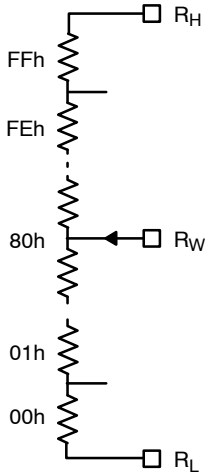


Figure 5. $\overline{WP}$ Timing

Device Operation

The CAT5140 is a resistor array integrated with a I^2C serial interface logic, an 8-bit volatile wiper register, and six 8-bit, non-volatile memory data registers. The resistor array contains 255 separate resistive elements connected in series. The physical ends of the array are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L). The tap positions between and at the ends of the series resistors are connected to the output wiper terminal (R_W) by CMOS transistor switches. Only one tap point for the potentiometer is connected to the wiper terminal at a time and is determined by the value of an 8-bit Wiper Register (WR).



When power is first applied to CAT5140 the wiper is set to midscale; Wiper Register = 80h. When the power supply becomes sufficient to read the non-volatile memory the value stored in the Initial Value Register (IVR) is transferred into the Wiper Register and the wiper moves to this new position. Five additional 8-bit non-volatile memory data registers are provided for general purpose data storage. Data can be read or written to the volatile or the non-volatile memory data registers via the I^2C bus.

Serial Bus Protocol

The following defines the features of the 2-wire bus protocol:

1. Data transfer may be initiated only when the bus is not busy.
2. During a data transfer, the data line must remain stable whenever the clock line is high. Any changes in the data line while the clock is high will be interpreted as a START or STOP condition.

The device controlling the transfer is a master, typically a processor or controller, and the device being controlled is the slave. The master will always initiate data transfers and provide the clock for both transmit and receive operations. Therefore, the CAT5140 will be considered a slave device in all applications.

START Condition

The START condition precedes all commands to the device, and is defined as a HIGH to LOW transition of SDA when SCL is HIGH. The CAT5140 monitors the SDA and SCL lines and will not respond until this condition is met.

STOP Condition

A LOW to HIGH transition of SDA when SCL is HIGH determines the STOP condition. All operations must end with a STOP condition.

Device Addressing

The bus Master begins a transmission by sending a START condition. The Master then sends the address of the particular slave device it is requesting. CAT5140 has a fixed 7 bit slave address: 0101000. The 8th bit (LSB) is the Read/Write instruction bit. For a Read the value is “1” and for Write the value is “0”.

After the Master sends a START condition and the slave address byte, the CAT5140 monitors the bus and responds with an acknowledge (on the SDA line) when its address matches the transmitted slave address.

Table 12. SALVE ADDRESS BIT FORMAT

MSB							LSB
0	1	0	1	0	0	0	R/$\overline{W}$

Acknowledge (ACK)

After a successful data transfer, each receiving device is required to generate an acknowledge. The Acknowledging device pulls down the SDA line during the ninth clock cycle, signaling that it received the 8 bits of data.

CAT5140 responds with an acknowledge after receiving a START condition and its slave address. If the device has been selected along with a write operation, it responds with an acknowledge after receiving each 8-bit byte. When the CAT5140 is in a READ mode it transmits 8 bits of data, releases the SDA line, and monitors the line for an acknowledge. Once it receives this acknowledge, the CAT5140 will continue to transmit data. If no acknowledge is sent by the Master, the device terminates data transmission and waits for a STOP condition.

WRITE Operation

In the Write mode, the Master device sends the START condition and the slave address information to the Slave device. In CAT5140’s case the slave address also contains a Read/Write command (R/$\overline{W}$) on the last bit of the 1st byte. After receiving an acknowledge from the Slave, the Master device transmits a second byte containing a Memory Address to select an available register. After a second acknowledge is received from the Slave, the Master device sends the data to be written into the selected register. The

CAT5140 acknowledges once more and the Master generates the STOP condition, at which time if a nonvolatile data register is being selected, the device begins an internal programming cycle to non-volatile memory. If the STOP condition is not sent immediately after the last ACK the internal non-volatile programming cycle doesn't start. While this internal cycle is in progress, the device will not respond to any request from the Master device.

Write operations to volatile memory are completed during the last bit of the data byte before the slave's acknowledge. The device will be ready for another command only after a STOP condition sent by Master.

Acknowledge Polling

The disabling of the inputs can be used to take advantage of the typical write cycle time. Once the stop condition is issued to indicate the end of the host's write operation, the CAT5140 initiates the internal write cycle. ACK polling can be initiated immediately. This involves issuing the start condition followed by the slave address. If the CAT5140 is still busy with the write operation, no ACK will be returned. If the CAT5140 has completed the write operation, an acknowledge will be returned and the host can then proceed with the next instruction operation.

WRITE Protection

The Write Protection feature allows the user to protect against inadvertent programming of the non-volatile data registers. If the $\overline{WP}$ pin is tied to LOW, the data registers are protected and become read only. Similarly, the $\overline{WP}$ pin going low after start will interrupt a nonvolatile write to data registers, while the $\overline{WP}$ pin going low after an internal write cycle has started will have no effect on any write operation. CAT5140 will accept slave addresses but the data registers are protected from programming, which the device indicates by failing to send an acknowledge after data is received.

READ Operation

A Read operation with a designated address consists of a three byte instruction followed by one or more Data Bytes (See Figure 3). The master initiates the operation issuing a START, an Identification byte with the R/$\overline{W}$ bit set to "0", an Address Byte. Then the master sends a second START, and a second Identification byte with the R/$\overline{W}$ bit set to "1". After each of the three bytes, the CAT5140 responds with an ACK. Then CAT5140 transmits the Data Byte. The master then can continue the read operation with the content of the next register by sending acknowledge or can terminate the read operation by issuing a NoACK followed by a STOP condition after the last bit of a Data Byte.

Table 13. MEMORY MAP

Address	Non-volatile Register	Non-volatile Default Value	Volatile Register
8	ACR		
7	Reserved		
6	General Purpose	00h	N/A
5	General Purpose	00h	N/A
4	General Purpose	00h	N/A
3	General Purpose	00h	N/A
2	General Purpose	00h	N/A
1	Device ID (read only)	D0h	N/A
0	IVR	80h	WR

If the master sends address 07h or addresses greater than 08h the slave responds with NoACK after the Memory Address byte.

Address 8: Volatile Access Control Register – ACR (I/O)

The ACR bit 7 (VOL) toggles between Non-volatile and volatile registers accessed at address 00h. When VOL is Low (0), the non-volatile IVR is accessed at address 00h. When VOL is high (1), the volatile Wiper Register is accessed at address 00h. The initial default value for VOL = 0.

Bit	7	6	5	4	3	2	1	0
Name	0/1 VOL	0	0	0	0	0	0	0

00h and 80h are the only values that should be written to address 08h. For any other value written to address 08h the slave will load only bit 7 but it will answer with a NoACK.

Address 7: RESERVED

The user should not read or write to this address. CAT5140 will respond with NoACK and it will take no action. Address 07h can be accessed only in a sequential read and its content is FFh.

Address 6–2: Non-volatile General Purpose Memory (I/O)

8-bit Non-volatile Memory

Bit	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–

General Purpose Memories are preprogrammed at the factory to a default value of "00h".

Address 1: Device ID (Read Only)

Bit 7 defines the Digital POT device manufacturer; **onsemi** = high (1)

Bit	7	6	5	4	3	2	1	0
Name	1	1	0	1	0	0	0	0

A writing to address 1 has no effect. Attempts to do so will return an ACK but no data will be written.

Address 0: IVR/WR Register (I/O)

Address 00h accesses one of two memory registers: the initial value register (IVR) or the wiper register (WR) depending upon the value of bit 7 in Access Control Register (ACR) which is at address 08h, above.

WR controls the wiper's position and is a volatile memory while IVR is non-volatile and retains its data after the chip has been powered down. Writes to IVR automatically update the WR while writes to WR leave IVR unaffected.

WR: Wiper Register = Volatile.

IVR: Initial Value Register = Non-volatile.

Writing and Reading operations:

1. If Bit 7 from ACR is 0 (non-volatile):
   - A write operation to address 00h will write the same value in WR and IVR.
   - A read operation to address 00h will output the content of IVR.
2. If bit 7 from ACR is 1 (volatile):
   - A write operation to address 00h will write in WR only.
   - A read operation to address 00h will output the content of WR.

All changes to the wiper's position are immediate. There is no delay the wiper's movement when writing to non-volatile memory.

Bit	7	6	5	4	3	2	1	0
Name	–	–	–	–	–	–	–	–

IVR is preprogrammed at the factory to a default value of "80h".

I²C SERIAL BUS INSTRUCTION FORMAT

Table 14. I²C SLAVE ADDRESS BITS

	Transfer Data	Slave Address							R/$\overline{W}$ bit
		bit 7	bit 6	bit 5	bit 4	bit 3	bit 2	bit 1	bit 0
Read	51h	0	1	0	1	0	0	0	1 (R)
Write	50h								0 ($\overline{W}$)

If the Slave Address Byte sent by the host is different the device will send a NoACK.

I²C PROTOCOL:

(A) Write data procedure with designated address. (See Table 15)

1. Host transfers the start condition
2. Host transfers the device slave address with the write mode R/$\overline{W}$ bit (0).
3. Device sends ACK
4. Host transfers the corresponding memory address to the device
5. Device sends ACK
6. Host transfers the write data to the designated address
7. Device sends ACK
8. Routines (6) and (7) are repeated based on the transfer data, and the designated address is automatically incremented*
9. Host transfers the stop condition.

*Automatically incremented writes are not possible after a non-volatile write.

Single write to either a volatile or non-volatile register. Note that Bit 7 of ACR determines which memory type is being written.

Table 15. SINGLE WRITE

(1)	(2)		(3)	(4)	(5)	(6)	(7)	(9)
Start	Slave Address	0 R/$\overline{W}$	0 ACK	Memory Address	0 ACK	Write Data	0 ACK	Stop

A single write to either a volatile or non-volatile register. At address 00h bit 7 of ACR determines which memory type is being written.

Table 16. MULTIPLE WRITES

(1)	(2)		(3)	(4)	(5)	(6)	(7)	(8)		(9)
Start	Slave Address	0 R/$\overline{W}$	0 ACK	Memory Address	0 ACK	Write Data	0 ACK	Write Data	0 ACK	Stop

Multiple writes are possible only if the starting address is 08h and it should be stopped with the first nonvolatile data byte. If a nonvolatile write does not end with a STOP procedure the register is not written.

(B) Read data procedure with designated address.

1. Host transfers the start condition
2. Host transfers the device slave address with the write mode R/$\overline{W}$ bit (0)
3. ACK signal recognition from the device
4. Host transfers the read address
5. ACK signal recognition from the device
6. Host transfers the re-start condition
7. Host transfers the slave address with the read mode R/$\overline{W}$ bit (1).
8. ACK signal recognition from the device
9. The device transfers the read data from the designated address
10. Host transfers ACK signal
11. The (9) & (10) routines above are repeated if needed, and the read address is auto-incremented
12. Host transfers ACK ‘H’ to the device
13. Host transfers the stop condition

Table 17. READ DATA

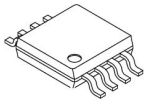
(1)	(2)		(3)	(4)	(5)	(6)	(7)		(8)	(9)	(10)	(11)	(12)	(13)
Start	Slave Address	0 R/$\overline{W}$	0 ACK	Memory Address	0 ACK	Restart	Slave Address	1 R/$\overline{W}$	0 ACK	Read Data	0 ACK	Read Data	1 ACK	Stop

(C) Read data procedure <u>without</u> a designated address.

1. Host transfers the start condition
2. Host transfers the device slave address with the read mode R/$\overline{W}$ bit =1
3. ACK signal recognition from the device. (Host then changes to receiver)
4. The device transfers data from the previous access address +1
5. Host transfers ACK signal
6. The (4) & (5) routines above are repeated if needed
7. Host transfers ACK ‘H’
8. Host transfers the stop condition

Table 18. Read Data w/o Designated Address

(1)	(2)		(3)	(4)	(5)	(6)	(7)	(8)
Start	Slave Address	1 R/$\overline{W}$	0 ACK	Read Data	0 ACK	Read Data	1 ACK	Stop



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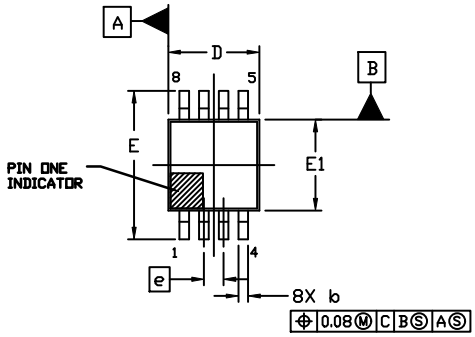
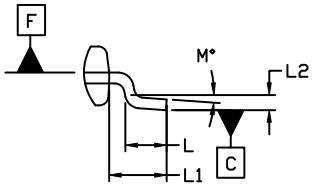
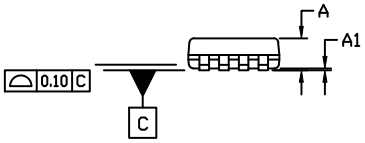


TOP VIEW

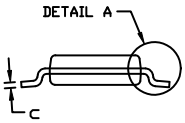


DETAIL A

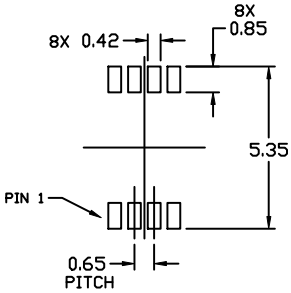
DIM	MILLIMETERS MIN.	NOM.	MAX.
A	---	---	1.10
A1	0.03	0.08	0.18
b	0.22	0.30	0.38
c	0.105	0.125	0.195
D	2.90	3.00	3.10
E	4.65	4.90	5.15
E1	2.90	3.00	3.10
e	0.65 BSC		
L	0.30	---	---
L1	0.95 REF		
L2	0.25 REF		
M	0°	---	10°



SIDE VIEW



END VIEW



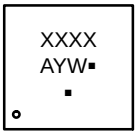
RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.10 mm IN EXCESS OF MAXIMUM MATERIAL CONDITION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.15 mm PER SIDE. DIMENSION E DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 mm PER SIDE. DIMENSIONS D AND E ARE DETERMINED AT DATUM F.
5. DATUMS A AND B ARE TO BE DETERMINED AT DATUM F.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
7. PIN 1 INDICATOR IS LOCATED HERE. MAY APPEAR AS A LASER MARKED, OR A MOLDED (CIRCLE OR HALF MOON), INDENT.

GENERIC MARKING DIAGRAM*



XXXX = Specific Device Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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