ESD5381 Series

ESD Protection Diode

Micro−Packaged Diodes for ESD Protection

The ESD5381 series are designed to protect voltage sensitive components from ESD. Excellent clamping capability, low leakage, and fast response time provide best in class protection on designs that are exposed to ESD. Because of their small size, they are suited for use in cellular phones, MP3 players, digital cameras and many other portable applications where board space comes at a premium.

Specification Features

- Low Capacitance
- Low Clamping Voltage
- Small Body Outline Dimensions: 0.60 mm x 0.30 mm
- Low Body Height: 0.3 mm
- Low Leakage
- Response Time is < 1 ns
- IEC61000−4−2 Level 4 ESD Protection
- IEC61000−4−4 Level 4 EFT Protection
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

Mechanical Characteristics

QUALIFIED MAX REFLOW TEMPERATURE: 260°C
Device Meets MSL 1 Requirements

MAXIMUM RATINGS

Rating		Symbol	Value	Unit
IEC 61000−4−2 (ESD)	Contact Air		8	kV
Total Power Dissipation on FR−5 Board (Note 1) @ T_A = 25°C Thermal Resistance, Junction−to−Ambient		P_D $R_{\theta JA}$	300 400	mW °C/W
Junction and Storage Temperature Range		T_J, T_{stg}	−55 to +150	°C
Lead Solder Temperature − Maximum (10 Second Duration)		T_L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
1. FR−5 = 1.0 x 0.75 x 0.62 in.

See Application Note AND8308/D for further description of survivability specs.

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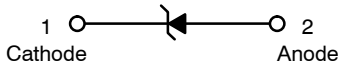
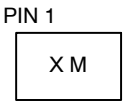


X3DFN2
CASE 152AF

MARKING DIAGRAM



X = Specific Device Code
M = Date Code
(Specific marking on following page)

ORDERING INFORMATION

Device	Package	Shipping†
ESD5381MUT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel
ESD5382MUT5G	X3DFN2 (Pb−Free)	10000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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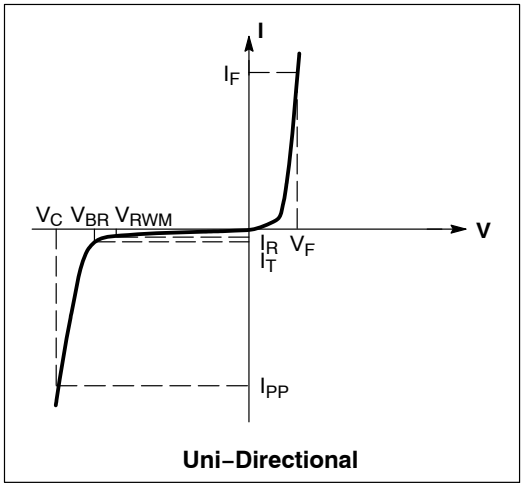
ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise noted)

Symbol	Parameter
I_{PP}	Maximum Reverse Peak Pulse Current
V_C	Clamping Voltage @ I_{PP}
V_{RWM}	Working Peak Reverse Voltage
I_R	Maximum Reverse Leakage Current @ V_{RWM}
V_{BR}	Breakdown Voltage @ I_T
I_T	Test Current

*See Application Note AND8308/D for detailed explanations of datasheet parameters.



Uni−Directional

ELECTRICAL CHARACTERISTICS (T_A = 25°C unless otherwise noted)

Device	Device Marking	V_{RWM} (V)	I_R (nA) @ V_{RWM}	V_{BR} (V) @ I_T (Note 2)	I_T	C (pF)		V_C (V) @ I_{PP} = 1 A	V_C
		Max	Max	Min	mA	Typ	Max	Max (Note 3)	Per IEC61000−4−2 (Note 4)
ESD5381MUT5G	J	3.0	100	6.1	1.0	12	13	10.5	Figures 1 and 2 See Below
ESD5382MUT5G	K	3.0	50	14.2	1.0	6	8	26.0	Figures 3 and 4 See Below

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

2. V_{BR} is measured with a pulse test current I_T at an ambient temperature of 25°C.
3. Surge current waveforms per Figure 7.
4. For test procedure see Figures 5 and 6 and Application Note AND8307/D.

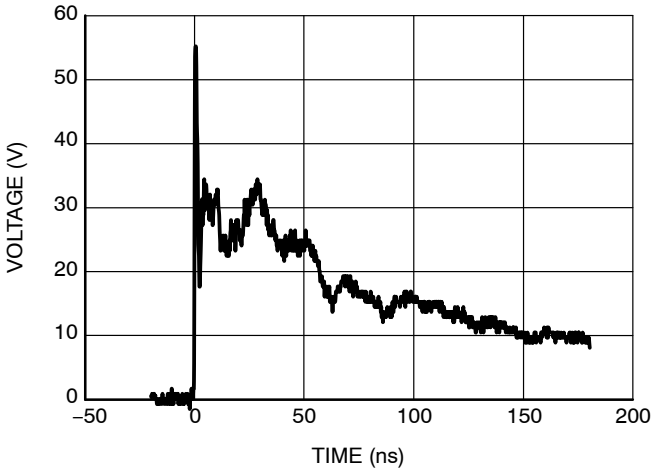


Figure 1. ESD5381MUT5G Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

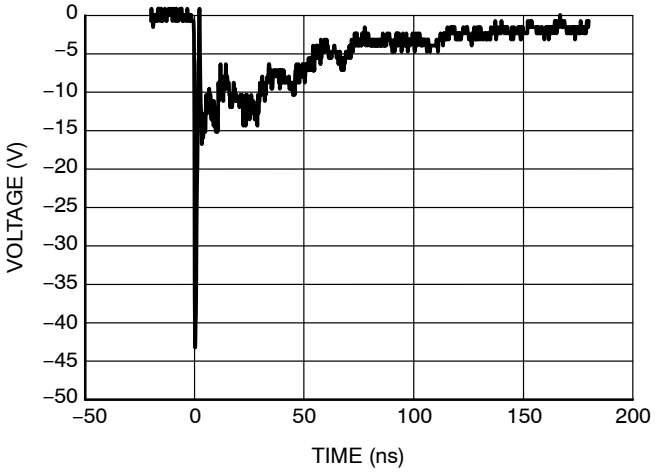


Figure 2. ESD5381MUT5G Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

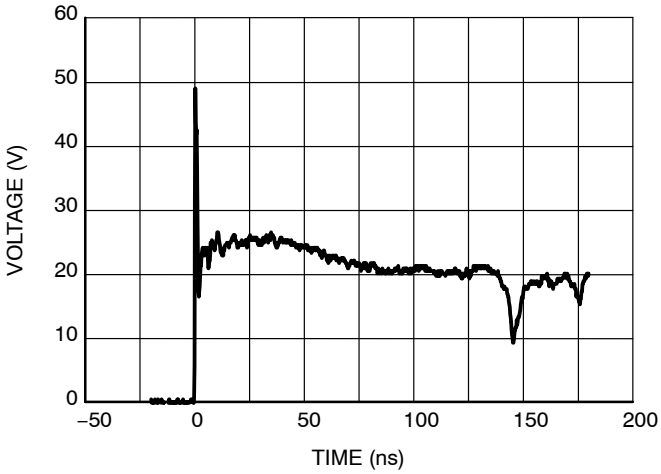


Figure 3. ESD5382MUT5G Clamping Voltage Screenshot Positive 8 kV Contact per IEC61000−4−2

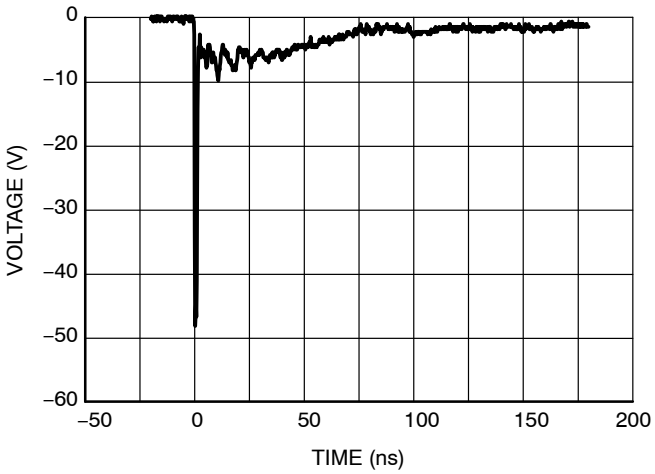


Figure 4. ESD5382MUT5G Clamping Voltage Screenshot Negative 8 kV Contact per IEC61000−4−2

IEC 61000−4−2 Spec.

Level	Test Voltage (kV)	First Peak Current (A)	Current at 30 ns (A)	Current at 60 ns (A)
1	2	7.5	4	2
2	4	15	8	4
3	6	22.5	12	6
4	8	30	16	8

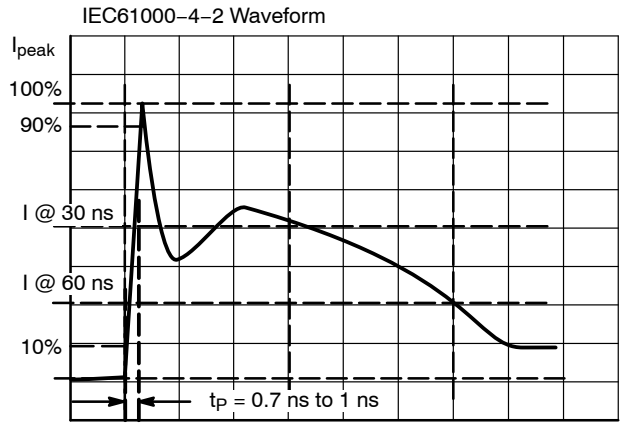


Figure 5. IEC61000−4−2 Spec

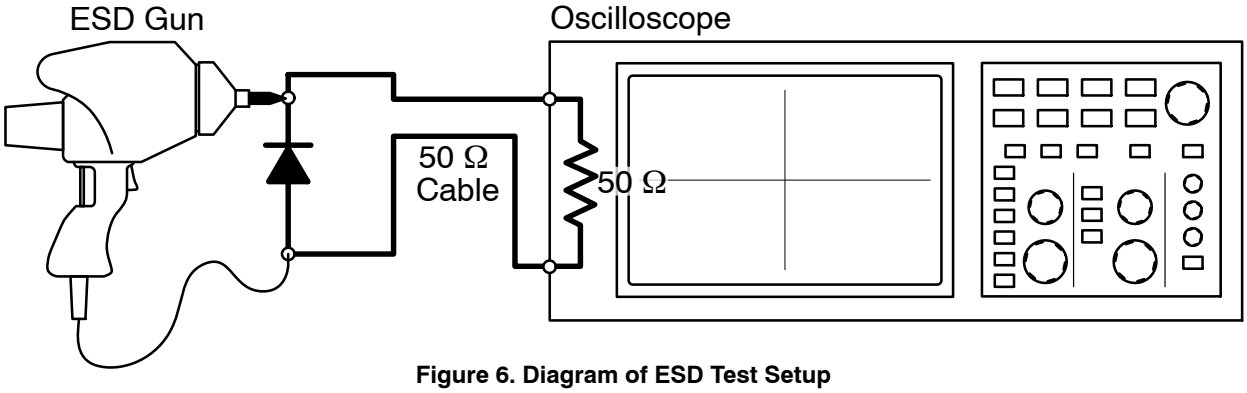


Figure 6. Diagram of ESD Test Setup

The following is taken from Application Note AND8308/D − Interpretation of Datasheet Parameters for ESD Devices.

ESD Voltage Clamping

For sensitive circuit elements it is important to limit the voltage that an IC will be exposed to during an ESD event to as low a voltage as possible. The ESD clamping voltage is the voltage drop across the ESD protection diode during an ESD event per the IEC61000−4−2 waveform. Since the IEC61000−4−2 was written as a pass/fail spec for larger systems such as cell phones or laptop computers it is not clearly defined in the spec how to specify a clamping voltage at the device level. ON Semiconductor has developed a way to examine the entire voltage waveform across the ESD protection diode over the time domain of an ESD pulse in the form of an oscilloscope screenshot, which can be found on the datasheets for all ESD protection diodes. For more information on how ON Semiconductor creates these screenshots and how to interpret them please refer to AND8307/D.

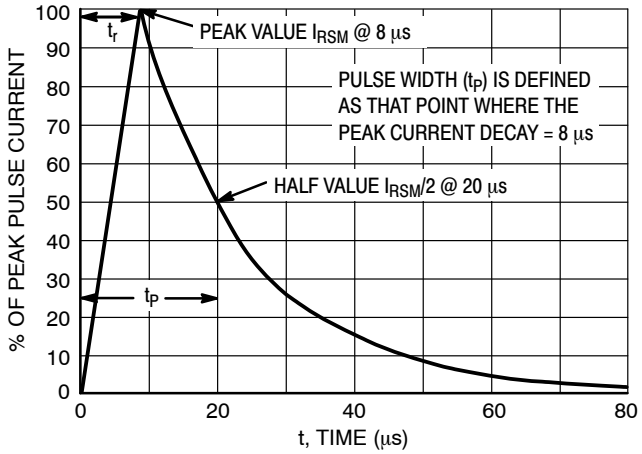
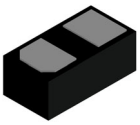


Figure 7. 8 X 20 μs Pulse Waveform



X3DFN2 0.62x0.32x0.24, 0.35P
CASE 152AF
ISSUE C

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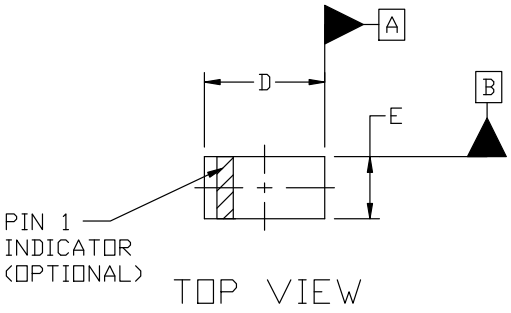
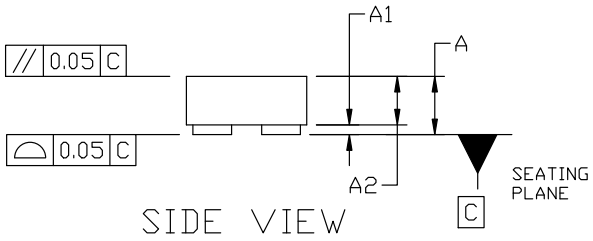
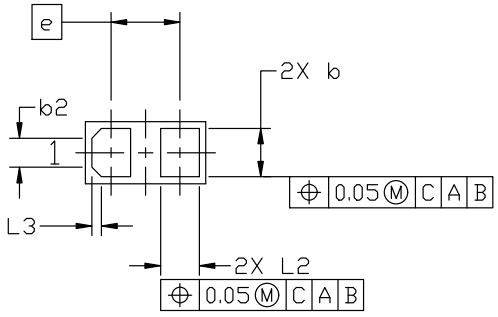


TOP VIEW



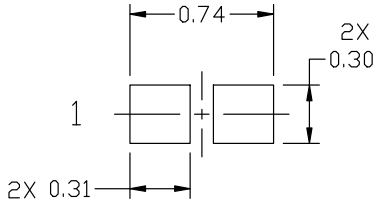
SIDE VIEW



BOTTOM VIEW

NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. 0201

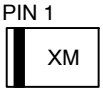
	MILLIMETERS		
DIM	MIN.	NOM.	MAX.
A	0.25	0.29	0.33
A1	0.00	---	0.05
A2	0.14	0.24	0.34
b	0.22	0.25	0.28
b2	0.150 REF		
D	0.58	0.62	0.66
E	0.28	0.32	0.36
e	0.355 BSC		
L2	0.17	0.20	0.23
L3	0.050 REF		



RECOMMENDED
MOUNTING FOOTPRINT*

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC
MARKING DIAGRAM*



X = Specific Device Code
M = Date Code

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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