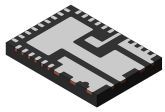
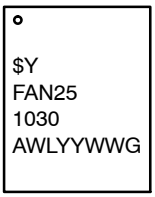
# Synchronous Buck Regulator with PMBus™, 35 A

# FAN251030



**WQFN34 5x7, 0.5P**
**CASE 510CL**

## MARKING DIAGRAM




| | |
|---|---|
| FAN251030 | = Specific Device Code |
| $Y | = **onsemi** Logo |
| A | = Assembly Location |
| WL | = Wafer Lot |
| YY | = Year |
| WW | = Work Week |
| G | = Pb−Free Designator |

## ORDERING INFORMATION

See detailed ordering and shipping information on page 49 of this data sheet.

### Description

The FAN251030 is a highly efficient synchronous buck regulator with digital interface, capable of operating with an input range from 4.5 V to 18 V and supporting up to 35 A load currents.

The FAN2510xx utilizes a fixed−frequency voltage−mode control architecture to provide a synchronized constant switching frequency while ensuring fast transient response.

Switching frequency and over−current protection can be programmed to provide a flexible solution for various applications. Output over−voltage, under−voltage, over−current, and thermal shutdown protections help prevent damage to the device during fault conditions.

### Features

- VIN Range: 4.5 V to 18 V
- Output Accuracy: ±0.7% at 3.3 V
- PMBUS 1.3.1 Compatible
- Accurate Voltage, Current and Thermal Telemetry Reporting
- High Efficiency: Over 96% Peak
- Continuous Output Current: 35 A
- Internal Linear Bias Regulator
- Output Voltage Range: 0.5 V to 5.5 V
- Adjustable Frequency: 200 kHz to 1.8 MHz
- Programmable Soft−Start
- Low Shutdown Current
- Internal Boot Diode
- Thermal Shutdown
- This Device is Pb−Free, Halogen Free/BFR Free, and is RoHS Compliant

### Typical Applications

- Server and Desktop Computers, Notebooks, Gaming
- Telecommunications
- High Density Power Solutions

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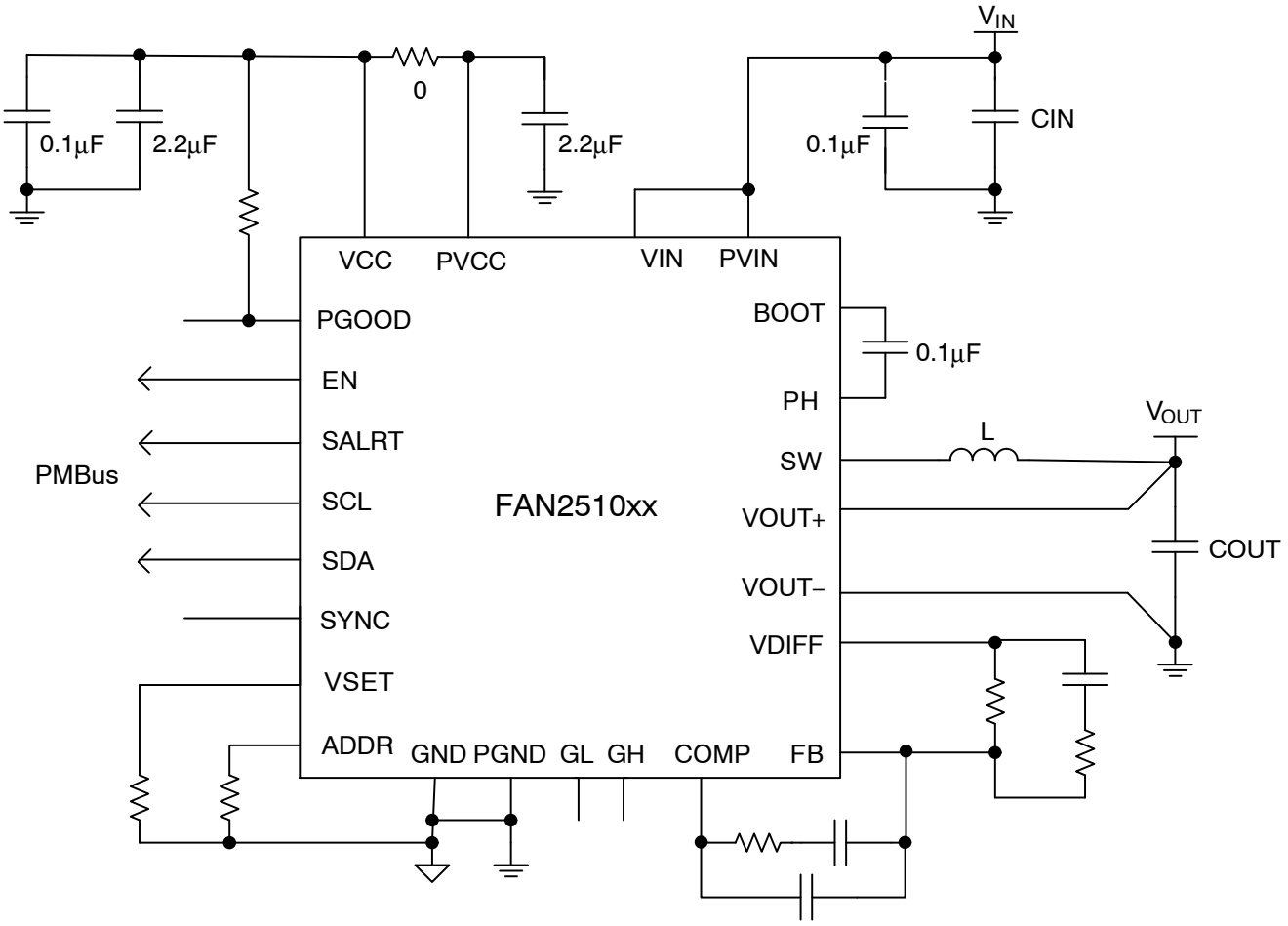


**Figure 1. Application Circuit**

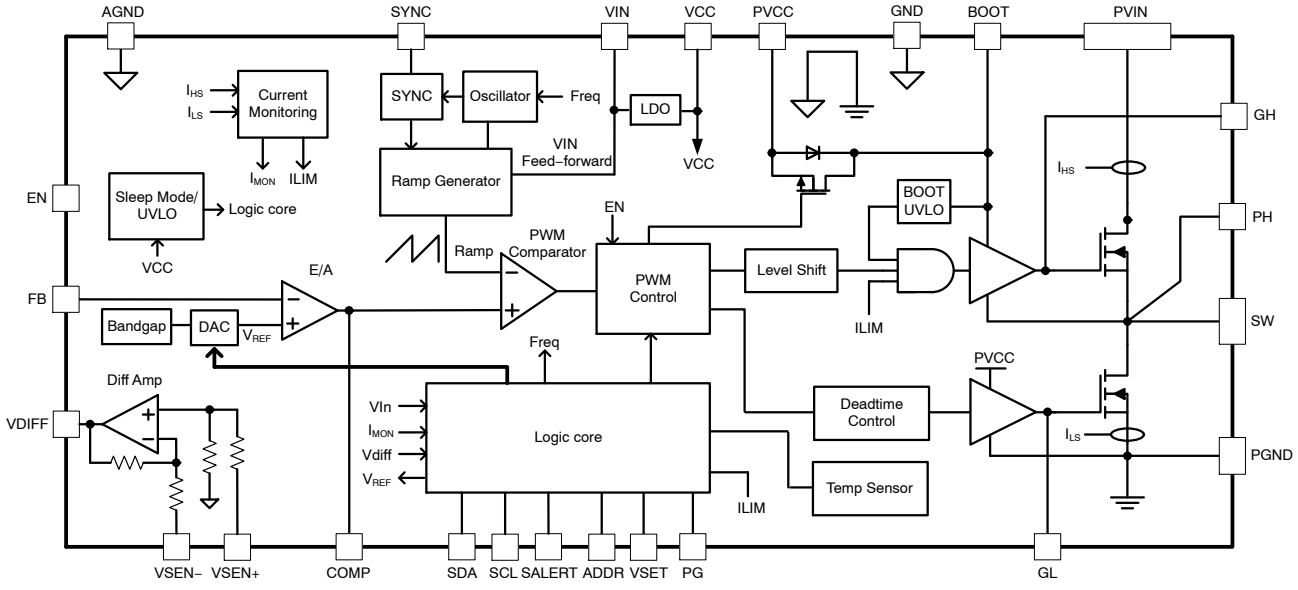


**Figure 2. Block Diagram**



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## PIN CONNECTIONS

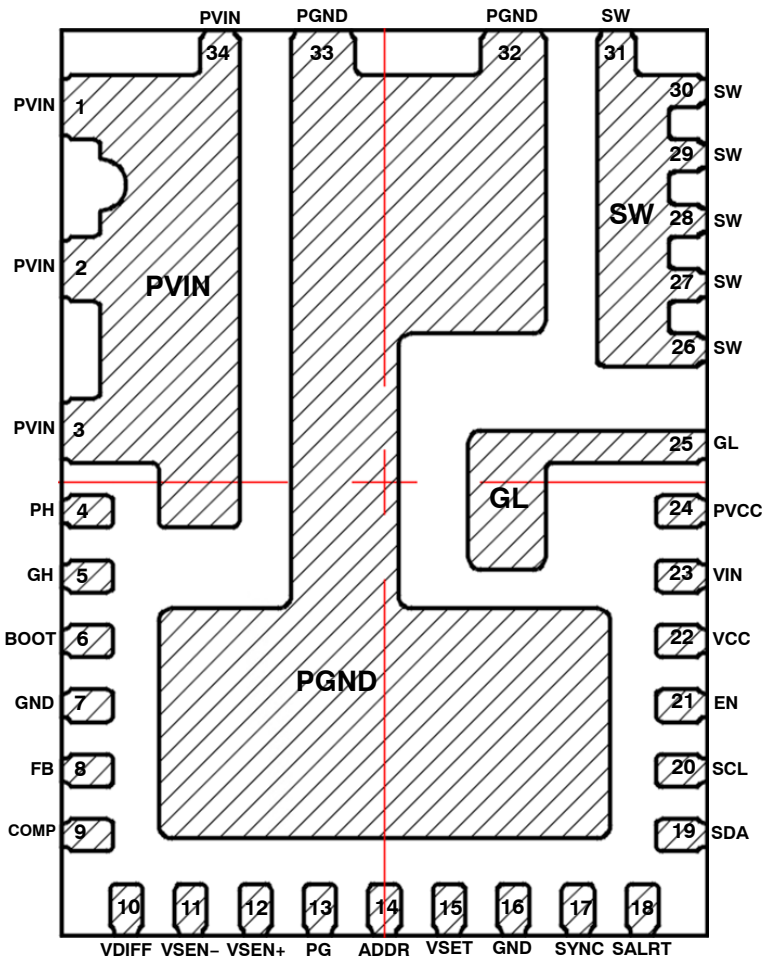


**Figure 3. Pin Assignment, Top Transparent View (5x7 mm, 0.5 mm Pin Pitch)**



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## PIN FUNCTION DESCRIPTION

| Pad/Pin | Name | Type | Description |
|---|---|---|---|
| 1, 2, 3, 34 | PVIN | Power | Power Input for the Power stage (High−side MOSFET Drain Connection). Apply Vin voltage always with Vcc capacitor |
| 4 | PH | Power | Return connection for the boot capacitor, internally connected to SW |
| 5 | GH | I/O | High−side MOSFET gate monitor (do not connect anything to this pin) |
| 6 | BOOT | Power | Supply for high−side MOSFET gate driver. A capacitor from BOOT to PH supplies the charge to turn on the N−channel high−side MOSFET. During the freewheeling interval (low−side MOSFET on), the high−side capacitor is recharged by an internal diode connected to PVCC |
| 7, 16 | GND | Ground | Analog Ground |
| 8 | FB | I/O | Inverting input to the voltage error amplifier |
| 9 | COMP | I/O | Output of the voltage error amplifier |
| 10 | VDIFF | I/O | Output of the VOUT sensing differential amplifier |
| 11 | VSEN− | I/O | Negative Input of the VOUT sensing differential amplifier |
| 12 | VSEN+ | I/O | Positive Input of the VOUT sensing differential amplifier |
| 13 | PG | I/O | Power GOOD; open−drain output indicating VOUT is within set limits |
| 14 | ADDR | I/O | PMBUS address programming pin. Use a resistor (with up to 1% tolerance) to set the address |
| 15 | VSET | I/O | VOUT pre−setting pin. Use a resistor (with up to 1% tolerance) to pre−set the output voltage (PMBUS command can override) |
| 17 | SYNC | I/O | Synchronization input or output |
| 18 | SALRT | I/O | PMBUS Alert pin |
| 19 | SDA | I/O | PMBUS Data pin |
| 20 | SCL | I/O | PMBUS Clock pin |
| 21 | EN | I/O | Enable input (and PMBUS Control pin) |
| 22 | VCC | Power | Output of the linear regulator; Supply pin for the controller. Can NOT be separated from PVCC. The capacitor should be always connected to this pin |
| 23 | VIN | Power | Power input to the linear regulator; also used in the modulator for input voltage feed−forward. Must always be connected even if the LDO is not used |
| 24 | PVCC | Power | Directly supplies power for the low−side gate driver and boot diode. This pin and VCC can NOT be separated, or connected to the external power supply |
| 25 | GL | I/O | Low−side MOSFET gate monitor (do not connect anything to this pin) |
| 26−31 | SW | Power | Switching Node; Internally Connected to the High−side MOSFET Source and Low−side MOSFET Drain |
| 32, 33 | PGND | Ground | Power Ground (Low−side MOSFET Source Connection), internally connected to GND |



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## MAXIMUM RATINGS

All voltages with respect to GND, unless otherwise specified.

| Rating (Note 1) | | Symbol | Value | Unit |
|---|---|---|---|---|
| Input Voltage Range | referenced to GND (Note 2) | $V_{PVIN}$, $V_{IN}$ | −0.3 to 25 | V |
| BOOT voltage range: | referenced to PVCC<br>referenced to PVCC, < 20 ns<br>referenced to SW, PH<br>referenced to PGND | $V_{BOOT}$ | −0.3 to 26<br>−0.3 to 30<br>−0.3 to 6<br>−0.3 to 30 | V |
| SW voltage range: | referenced to PGND<br>referenced to PGND, <10 ns | $V_{SW}$, $V_{PH}$ | −1 to 25<br>−5 to 28 | V |
| High−Side MOSFET Gate voltage range: | referenced to SW, PH<br>referenced to PGND | $V_{GH}$ | −0.3 to 6<br>−0.3 to 30 | V |
| Low−Side MOSFET Gate voltage range: | referenced to PGND | $V_{GL}$ | −0.3 to 6 | V |
| Driver Supply Input voltage range | referenced to PGND | $V_{PVCC}$ | −0.3 to 6 | V |
| Controller Supply Input voltage range | | $V_{VCC}$ | −0.3 to 6 | V |
| Output Voltage Sense voltage range | | $V_{SEN+}$, $V_{SEN−}$ | −0.3 to 6 | V |
| Differential Amplifier Output voltage range | | $V_{DIFF}$ | −0.3 to 6 | V |
| Error Amplifier Input voltage range | | $V_{FB}$ | −0.3 to 6 | V |
| Error Amplifier Output voltage range | | $V_{COMP}$ | −0.3 to 6 | V |
| SYNC voltage range | | $V_{SYNC}$ | −0.3 to 6 | V |
| Power Good Output voltage range | | $V_{PG}$ | −0.3 to 6 | V |
| Enable Input voltage range | | $V_{EN}$ | −0.3 to 6 | V |
| Vout Setting Input voltage range | | $V_{VSET}$ | −0.3 to 6 | V |
| PMBUS Data pin voltage range | | $V_{SDA}$ | −0.3 to 6 | V |
| PMBUS Clock input voltage range | | $V_{SCL}$ | −0.3 to 6 | V |
| PMBUS Alert Output voltage range | | $V_{SALERT}$ | −0.3 to 6 | V |
| PMBUS Address Input voltage range | | $V_{ADDR}$ | −0.3 to 6 | V |
| Maximum Junction Temperature | | $T_{J(max)}$ | 150 | °C |
| Storage Temperature Range | | $T_{STG}$ | −55 to 150 | °C |
| Lead Temperature Soldering Reflow (Note 3) | | $T_{SLD}$ | 260 | °C |
| ESD, Human Body Model per ANSI / ESDA / JEDEC JS−001 | | $ESD_{HBM}$ | 2.0 | kV |
| ESD, Charge Device Model per ANSI / ESDA / JEDEC JS−002 | | $ESD_{CDM}$ | 1.0 | kV |
| Latch−Up Current Rating, 100°C, per JEDEC JESD78, class II | | $I_{LU}$ | ±100 | mA |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Refer to ELECTRICAL CHARACTERISTICS, RECOMMENDED OPERATING RANGES and/or APPLICATION INFORMATION for Safe Operating parameters.
2. PGND is internally connected to GND.
3. For information, please refer to our Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

## THERMAL CHARACTERISTICS

| Rating | Symbol | Value | Unit |
|---|---|---|---|
| Thermal Resistance, Junction−to−Air (Note 4) | $R_{\theta JA}$ | 14.6 | °C/W |
| Thermal Reference, Junction−to− Case (Note 4) | $R_{\Psi JC}$ | 1.5 | °C/W |

4. Values are based on **onsemi** Evaluation Board of 2 oz copper thickness, No airflow and FR4 PCB substrate.



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## RECOMMENDED OPERATING RANGE

| Rating | Symbol | Min | Max | Unit |
|---|---|---|---|---|
| Input Voltage | $V_{in}$ | 4.5 | 18 | V |
| Output Voltage | $V_{out}$ | 0.5 | 5.5 | V |
| Continuous Output Current | $I_{out}$ | 0 | 35 | A |
| Adjustable Output Voltage | $V_{out}$ | 0.5 | 5.5 | V |
| EN Pin Voltage | $V_{EN}$ | 0 | 5 | V |
| Junction Temperature | $T_J$ | −40 | 125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

## ELECTRICAL CHARACTERISTICS

$V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = $T_J$ = −40°C to 125°C; unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **SUPPLY CURRENT** | | | | | | |
| Quiescent Current | EN Low, not switching | $I_{VIN,Q}$ | – | 2.8 | – | mA |
| **LINEAR REGULATOR** | | | | | | |
| Regulator Output Voltage | | $V_{REG}$ | 4.75 | 5 | 5.25 | V |
| Regulator Current Limit | Not for external use | $I_{REG}$ | 60 | – | – | mA |
| Regulator Drop Out Voltage | $I_{LDO}$ = 40 mA, $V_{IN}$ = 5 V | $V_{DROPOUT}$ | – | – | 0.3 | V |
| **INTERNAL MOSFET RDS−ON** (Note 5) | | | | | | |
| High Side MOSFET | $V_{GS}$= 5 V | $HS-RDS_{ON}$ | – | 2.8 | – | mΩ |
| Low Side MOSFET | | $LS-RDS_{ON}$ | – | 1.3 | – | mΩ |
| **DIFFERENTIAL AMPLIFIER** | | | | | | |
| $V_{SEN+}$ Pin Input Impedance | | $R_{SEN+}$ | – | 100 | – | kΩ |
| $V_{SEN−}$ Pin Input Impedance | G = 1<br>G = 0.5<br>G = 0.25 | $R_{SEN−}$ | –<br>–<br>– | 50<br>66<br>78 | –<br>–<br>– | kΩ |
| Output Sinking current capability | | $I_{DIFF(sink)}$ | 3 | – | – | mA |
| Output Sourcing current capability | | $I_{DIFF(source)}$ | 3 | – | – | mA |
| Closed−Loop Bandwidth (Note 5) | | $BW_{DIFF}$ | 2 | – | – | MHz |
| Closed−Loop Gain | G = 1, for $V_{OUT} \le 1.99$ | | – | 1 | – | V / V |
| | G = 0.5 for $1.99 \le V_{OUT} \le 3.99$ | | – | 0.5 | – | |
| | G = 0.25, for $V_{OUT} \ge 3.99$ | | – | 0.25 | – | |
| Closed−Loop Accuracy | G = 1, $V_{OUT}$ = 600 mV, no load | $V_{err}$ | −1 | – | 1 | % |
| | G = 0.5, $V_{OUT}$ = 3.3 V, no load | | −1 | – | 1 | |
| | G = 0.5, $V_{OUT}$ = 3.3 V, 25°C, no load | | −0.7 | – | 0.7 | |
| | G = 0.25, $V_{OUT}$ = 5 V, no load | | −1 | – | 1 | |
| **REFERENCE, $V_{OUT}$ SETTING AND MARGINING** | | | | | | |
| FB Pin Voltage Accuracy | 0°C ≤ $T_J$ ≤ 125°C, $V_{FB}$ = 0.6 V, 1.65 V | $V_{REF}$ | −1 | – | 1 | % |
| $V_{OUT}$ Setting Range (Note 5) | | $V_{OUT,RNG}$ | 0.5 | – | 5.5 | V |
| $V_{OUT}$ Setting and Margin Step (Note 5) | | $V_{TM,S}$ | – | 1.953 | – | mV |
| Margin Low Default Value | | $V_{MGL}$ | – | 3.1 | – | V |



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## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = $T_J$ = −40°C to 125°C; unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **REFERENCE, $V_{OUT}$ SETTING AND MARGINING** | | | | | | |
| Margin Low Default Value Range (Note 5) | | $V_{MGL}$ | 0.5 | – | 5.5 | V |
| Margin High Default Value | | $V_{MGH}$ | – | 3.4 | – | V |
| Margin High Default Value Range (Note 5) | | $V_{MGH}$ | 0.5 | – | 5.5 | V |
| Default Transition Rate | | $k_{TRAN}$ | – | 0.203 | – | mV/μs |
| Transition Rate Range (Note 5) | | $k_{TRAN,RNG}$ | 0.203 | – | 9.375 | mV/μs |
| Transition Rate Accuracy | | $k_{TRAN,ACC}$ | – | ±10 | – | % |
| **OSCILLATOR** | | | | | | |
| Default Switching Frequency | | $F_{SW}$ | 540 | 600 | 660 | kHz |
| Switching Frequency Setting Range (Note 5) | | $F_{SW,RNG}$ | 200 | – | 1800 | kHz |
| Switching Frequency Step Size (Note 5) | 200 ≤ $F_{SW}$ ≤ 1200 kHz | $F_{SW,ST}$ | – | 50 | – | kHz |
| | 1200 < $F_{SW}$ ≤ 1800 kHz | | – | 100 | – | |
| Switching Frequency Accuracy | | $F_{SW,ACC}$ | −10 | – | 10 | % |
| **FREQUENCY SYNCHRONIZATION** | | | | | | |
| SYNC Input Logic HIGH | | $V_{SYNC_IN_H}$ | 2 | – | – | V |
| SYNC Input Logic LOW | | $V_{SYNC_IN_L}$ | – | – | 0.8 | V |
| Input HIGH Level Pulse Width | | $t_{HIGH_IN_MIN}$ | 135 | – | – | ns |
| Input LOW Level Pulse Width | | $t_{LOW_IN_MIN}$ | 150 | – | – | ns |
| Synchronize Frequency (Note 5) | Percentage of the oscillator frequency | $F_{SYNC}$ | 80 | – | 120 | % |
| Transition Delay before Synchronizing to SYNC frequency | In Number of oscillator Clock Cycles per 2 ms time period | $t_{SYNC_DL}$ | – | 64 | – | Cycles |
| SYNC Pin Pull down Resistance | | $R_{SYNC_PD}$ | – | 100 | – | kΩ |
| SYNC Output Driver Pull−up Resistance | | $R_{SYNCDRPU}$ | – | 10 | – | Ω |
| SYNC Output Driver Pull−down Resistance | | $R_{SYNCDRPD}$ | – | 12 | – | Ω |
| SYNC Output Duty Cycle | | $D_{SYNC_OUT}$ | – | 45 | – | % |
| SYNC Pin Lead Capacitance | $V_{OUT}$ = 0 V (Note 5) | $C_{L_SYNC}$ | – | – | 200 | pF |
| **RAMP AND PWM MODULATOR** | | | | | | |
| PWM Modulator Feed−forward(Vin) Gain, $V_{IN}/\Delta V_{RAMP}$ | | $k_{PWM}$ | – | 10 | – | |
| PWM Minimum ON Time | | $t_{ON_MIN}$ | 30 | 50 | 70 | ns |
| PWM Minimum OFF Time | | $t_{OFF_MIN}$ | 100 | 150 | 200 | ns |
| **ERROR AMPLIFIER** | | | | | | |
| Unity Gain Bandwidth (Note 5) | | $G_{BW}$ | 5 | 10 | – | MHz |
| DC Gain (Note 5) | $V_{FB}$ = 0.6 V | G | 78 | 100 | – | dB |
| COMP Source Current | | $I_{COMP_SRC}$ | 2 | 10 | – | mA |
| COMP Sink Current | | $I_{COMP_SNK}$ | 2 | 9 | – | mA |
| **SOFT−START** (Low side FET turns ON after $V_{OUT}$ > 300 mV) | | | | | | |
| Default TON−Rise | | $t_{SST}$ | – | 5 | – | ms |
| TON−Rise Range (Note 5) | | $t_{SST,RNG}$ | 1 | – | 20 | ms |



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## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = $T_J$ = −40°C to 125°C; unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **SOFT−START** (Low side FET turns ON after $V_{OUT}$ > 300 mV) | | | | | | |
| Default TON Delay | | $t_{ONDLY}$ | − | 1 | − | ms |
| TON Delay Range (Note 5) | | $t_{ONDLY,RNG}$ | 1 | − | 10 | ms |
| Default TOFF−Fall | | $t_{SSP}$ | − | 5 | − | ms |
| TOFF−Fall Range (Note 5) | | $t_{SSP,RNG}$ | 1 | − | 20 | ms |
| Default TOFF Delay | | $t_{OFFDLY}$ | − | 1 | − | ms |
| TOFF Delay Range (Note 5) | | $t_{OFFDLY,RNG}$ | 0 | − | 10 | ms |
| Default TON MAX FAULT LIMIT | | $t_{maxFLT}$ | − | 12 | − | ms |
| TON MAX FAULT LIMIT Range (Note 5) | | $t_{maxFLT,RNG}$ | 0 | − | 50 | ms |
| **CYCLE−BY−CYCLE CURRENT LIMIT** | | | | | | |
| High−Side Current Limit Blanking Time (Note 5) | | $t_{LIMPKBLNK}$ | − | 50 | − | ns |
| Peak (High−Side) Current Limit Default | | $I_{LIMPK}$ | − | 54 | − | A |
| Peak (High−Side) Current Limit Range | | $I_{LIMPK,RNG}$ | 2 | − | 62 | A |
| Peak (High−Side) Current Limit Accuracy | $I_{LIMPK}$ = 40 A | $I_{LIMPK,ACC}$ | −15 | − | 15 | % |
| Low− Side Current Limit Blanking Time (Note 5) | | $t_{LIMNEGBLNK}$ | − | 60 | − | ns |
| Negative (Low−Side) Current Limit Default | | $I_{LIMNEG}$ | − | 14 | − | A |
| Negative (Low−Side) Current Limit Range | | $I_{LIMNEG,RNG}$ | 10 | − | 24 | A |
| **AVERAGE OUTPUT CURRENT** | | | | | | |
| Output Current Warning | | | − | 32 | − | A |
| Output Current Warning Range (Note 5) | | | 1 | − | 64 | A |
| Output Current Fault | | | − | 45 | − | A |
| Output Current Fault Range (Note 5) | | | 1 | − | 64 | A |
| Average Fault Response Time Range (Note 5) | | | 0 | − | 10 | ms |
| **ENABLE** | | | | | | |
| Enable Threshold | EN voltage rising | $V_{EN}$ | 1.12 | 1.22 | 1.32 | V |
| Disable Threshold | EN voltage falling | $V_{DIS}$ | 1.00 | 1.105 | 1.195 | V |
| Hysteresis | | $V_{EN,HYS}$ | − | 115 | − | mV |
| EN Pin Internal Pull−down Resistor | | $R_{EN}$ | − | 900 | − | kΩ |
| EN Pin Internal Clamp Resistance | $V_{EN}$ = 5 V | $R_{ENCLMP}$ | − | 250 | − | kΩ |
| **VCC UVLO** | | | | | | |
| VCC UVLO Enable Threshold | VCC voltage rising | $V_{CC,EN}$ | − | 4 | 4.35 | V |
| VCC UVLO Disable Threshold | VCC voltage falling | $V_{CC,DIS}$ | 3.58 | 3.8 | − | V |
| VCC UVLO Hysteresis | | $V_{CCHYS}$ | − | 175 | − | mV |
| **INPUT VOLTAGE PROTECTIONS** | | | | | | |
| Default VIN Turn−on Threshold | $V_{IN}$ rising | $V_{ON}$ | − | 6 | − | V |
| VIN Turn−on Threshold Range | | $V_{ON,RNG}$ | 3 | − | 10.5 | V |
| VIN Turn−on Threshold Accuracy | | $V_{ON,ACC}$ | −8 | − | 8 | % |



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## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = $T_J$ = −40°C to 125°C; unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **INPUT VOLTAGE PROTECTIONS** | | | | | | |
| Default VIN Turn−off Threshold | $V_{IN}$ falling | $V_{OFF}$ | − | 5.5 | − | V |
| VIN Turn−off Threshold Range | | $V_{OFF,RNG}$ | 2.5 | − | 10 | V |
| VIN Turn−off Threshold Accuracy | | $V_{OFF,ACC}$ | −10 | − | 8 | % |
| Default VIN Overvoltage Threshold | $V_{IN}$ rising | $V_{INOV}$ | − | 20 | − | V |
| VIN Overvoltage Threshold Range | | $V_{INOV,RNG}$ | 18 | − | 24 | V |
| VIN Overvoltage Threshold Accuracy | | $V_{INOV,ACC}$ | −8 | − | 5 | % |
| **OUTPUT VOLTAGE PROTECTIONS** (as a percentage of $V_{OUT}$) | | | | | | |
| Default VOUT Overvoltage Threshold | $V_{OUT}$ rising | $V_{OOV}$ | − | 116 | − | % |
| VOUT Overvoltage Threshold Setting Range | | $V_{OOV,RNG}$ | 110 | − | 124 | % |
| VOUT Overvoltage Threshold Setting Step | | | − | 2 | − | % |
| Default VOUT Warning Threshold | $V_{OUT}$ rising | $V_{OWRN}$ | − | 108 | − | % |
| VOUT Warning Threshold Setting Range | | $V_{OWRN,RNG}$ | 106 | − | 116 | % |
| VOUT Overvoltage Threshold Setting Step | | | − | 2 | − | % |
| Default VOUT Under−voltage Threshold | $V_{OUT}$ falling | $V_{OUV}$ | − | 75 | − | % |
| VOUT Under−voltage Threshold Setting Range | | $V_{OUV,RNG}$ | 55 | − | 90 | % |
| VOUT Under−voltage Threshold Setting Step | | | − | 5 | − | % |
| **OUTPUT POWER GOOD (AS A PERCENTAGE OF $V_{OUT}$)** | | | | | | |
| Default PG Asserting Threshold | $V_{OUT}$ rising | $V_{PGON}$ | − | 90 | − | % |
| PG Asserting Threshold Range (Note 5) | | $V_{PGON,RNG}$ | 84 | − | 98 | % |
| PG Asserting Threshold Accuracy | | $V_{PGON,ACC}$ | −2 | − | 2 | % |
| Default PG de−asserting Threshold | $V_{OUT}$ falling | $V_{PGOF}$ | − | 84 | − | % |
| PG De−asserting Threshold Range | | $V_{PGOF,RNG}$ | 82 | − | 96 | % |
| PG De−asserting Threshold Accuracy | | $V_{PGOF,ACC}$ | −2 | − | 2 | % |
| PG Leakage Current | | $I_{PG,LEAK}$ | − | − | 1 | μA |
| PG De−glitch Filter Duration | | $t_{PG_FLT}$ | − | 5 | − | μs |
| PG Rising Delay | | | − | 560 | − | μs |
| PG Falling Delay | | | − | 10 | − | μs |
| PG Output Low Voltage | $V_{OUT}$ = 70% $V_{OUTREF}$, $I_{PG}$ = −1 mA | $V_{PG_L}$ | − | 6 | 12 | mV |
| **INTERNAL BOOTSTRAP DIODE** | | | | | | |
| Forward Voltage | $I_F$ = 10 mA | $V_{FBOOT}$ | − | − | 0.3 | V |
| Bootstrap Voltage UVLO | $V_{BOOT}$ falling | $V_{BTUV}$ | 2.9 | 3.2 | − | V |
| Bootstrap Voltage UVLO Hysteresis | $V_{BOOT}$ rising | $V_{BTUVHYS}$ | − | 0.35 | − | V |
| **THERMAL PROTECTION** | | | | | | |
| Default Thermal Fault Threshold | $T_J$ rising | $T_{OFF}$ | − | 140 | − | °C |
| Thermal Fault Threshold Setting Range | | $T_{OFF,RNG}$ | 80 | − | 160 | °C |
| Default Thermal Warning Threshold | $T_J$ rising | $T_{OFF}$ | − | 115 | − | °C |



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## ELECTRICAL CHARACTERISTICS (continued)

$V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, for typical values $T_A$ = 25°C, for min/max values $T_A$ = $T_J$ = −40°C to 125°C; unless otherwise specified.

| Parameter | Test Conditions | Symbol | Min | Typical | Max | Unit |
|---|---|---|---|---|---|---|
| **THERMAL PROTECTION** | | | | | | |
| Thermal Warning Threshold Range | | $T_{OFF,RNG}$ | 70 | – | 150 | °C |
| Thermal Shutdown Threshold Umbrella | $T_J$ rising | $T_{SHDN}$ | – | 160 | – | °C |
| Thermal Shutdown Hysteresis | | $T_{SHDN,HYS}$ | – | 15 | – | °C |
| **TELEMETRY REPORTING** | | | | | | |
| Telemetry Refresh Time Interval (Note 5) | | $t_{telemetry}$ | – | 900 | – | μs |
| VIN Voltage Accuracy | EN = 0 | $V_{IN,ACC}$ | −5 | – | 5 | % |
| VOUT Voltage Accuracy | G = 1, VSET = AGND | $V_{OUT,ACC}$ | −2 | – | 2 | % |
| Output Current Accuracy | $I_{OUT}$ = 6 A to 35 A | $I_{OUT,ACC}$ | – | ±10 | – | % |
| Input Current Accuracy | $F_{SW}$ = 600 kHz, For $I_{OUT}$ = 6 A to 35 A | $I_{OUT,ACC}$ | – | ±10 | – | % |
| Temperature Accuracy (Note 5) | 0°C – 125°C | $T_{ACC}$ | −5 | – | 5 | °C |
| **PMBUS INTERFACE** (Note 5) | | | | | | |
| Pin Capacitance (SCL, SDA) | | | – | – | 10 | pF |
| PMBUS Operating Frequency Range | | | 10 | – | 400 | kHz |
| Bus Free Time between START and Stop | | | 1.3 | – | – | μs |
| Hold Time after Repeated START | | | 0.6 | – | – | μs |
| Repeated START Setup Time | | | 0.6 | – | – | μs |
| Data Hold Time (receive & transmit modes) | | | 0 | – | – | ns |
| Data Setup Time | | | 100 | – | – | ns |
| Detect Clock Low Timeout | | | 25 | – | 35 | ms |
| Cumulative Clock Low Master Extend Time | | | – | – | 10 | ms |
| Cumulative Clock Low Slave Extend Time | | | – | – | 25 | ms |
| Clock Low Time | | | 1.3 | – | – | μs |
| Clock High Time | | | 0.6 | – | 50 | μs |
| SCL/SDA Fall Time | | | – | – | 120 | ns |
| SCL/SDA Rise Time | | | – | – | 120 | ns |
| SCL/SDA High/Rising Threshold | | | 1.95 | – | – | V |
| SCL/SDA Low/Falling Threshold | | | – | – | 0.8 | V |
| SCL/SDA Threshold Hysteresis | | | – | 0.6 | – | V |
| Noise Spike Suppression Time | | | 0 | – | 50 | ns |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Performance guaranteed over the indicated operating temperature range by design and/or characterization tested at $T_J$ = $T_A$ = 25°C. Low duty cycle pulse techniques are used during testing to maintain the junction temperature as close to ambient as possible.



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## TYPICAL PERFORMANCE CHARACTERISTICS

$V_{IN}$ = 12 V, $V_{OUT}$ = 3.3 V, $F_{sw}$ = 600 kHz, L = 1 μH (Note 6), $C_{OUT}$ = 1000 μF, $T_A$ = 25°C, unless otherwise indicated.

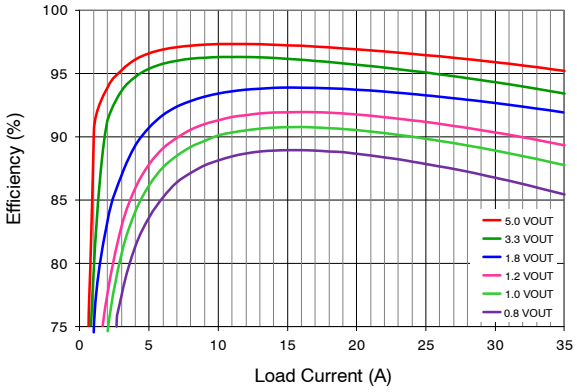


**Figure 4. Efficiency**

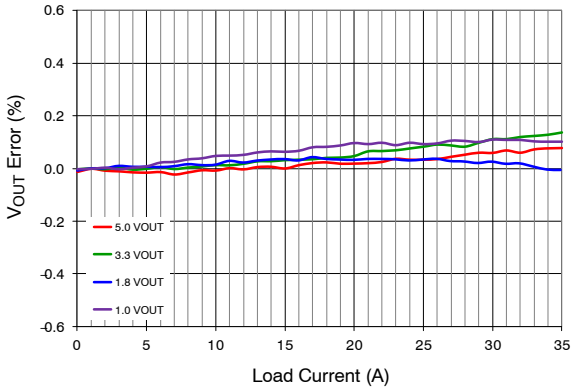


**Figure 5. Load Regulation**

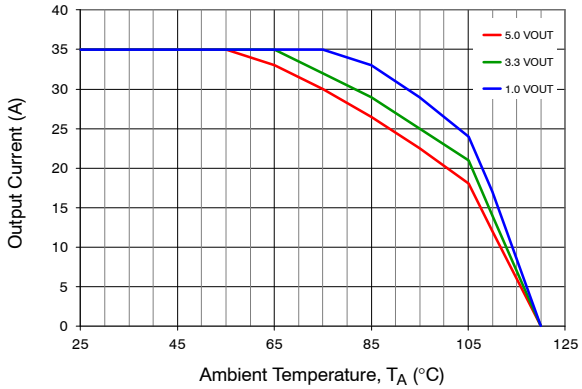


**Figure 6. Thermal Safe Operating Area, No Airflow, PCB: 2 oz. Cu**

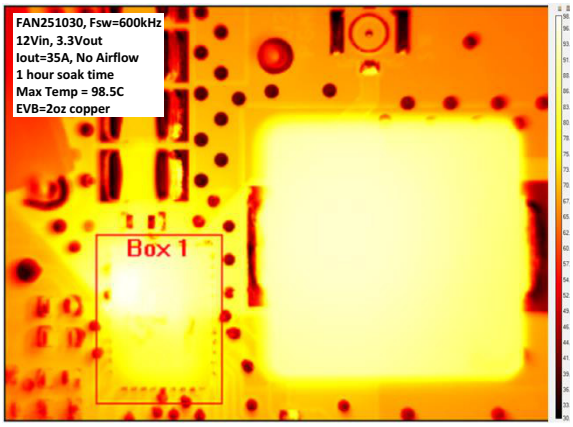


**Figure 7. Thermal Image, No Airflow, $I_{OUT}$ = 35 A**

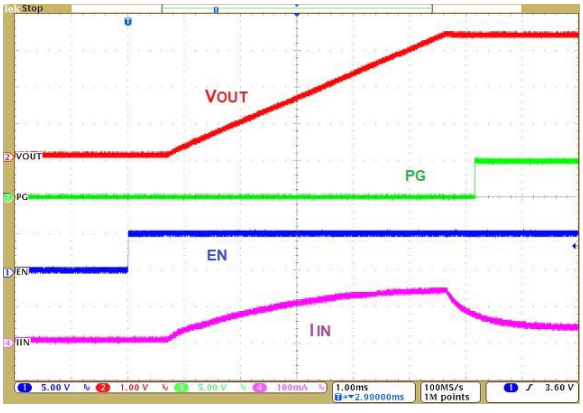


**Figure 8. 5 msec Start−Up, No Load**

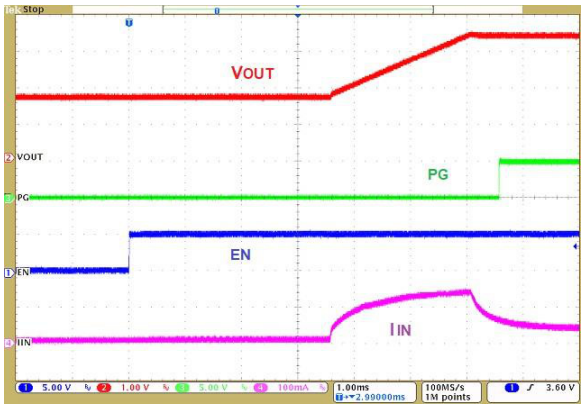


**Figure 9. 5 msec Start−Up with 50% Pre−Bias**



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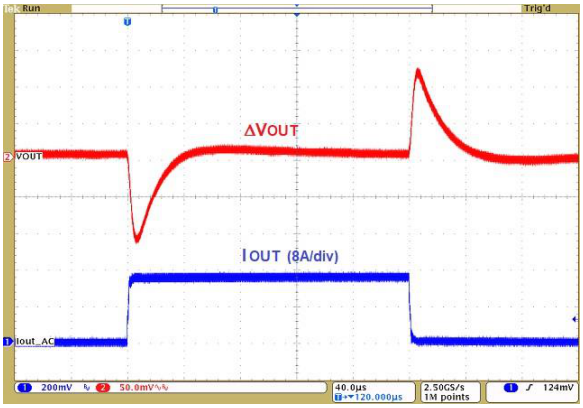


**Figure 10. Load Transient 0−15 A, 10 A/μs**

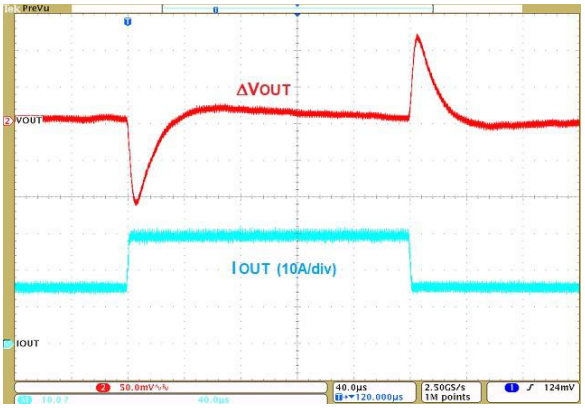


**Figure 11. Load Transient 15−30 A, 10 A/μs**

6. Tests conducted using L = 1.0 μH (Pulse PA4343.102NLT)



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## APPLICATION INFORMATION

The FAN2510xx is a high−efficiency synchronous buck converter with integrated controller, driver and two power MOSFETs. It can operate over a 4.5 V to 18 V input voltage range, and delivers up to 35 A continuous load current.

FAN2510xx uses a voltage mode PWM control scheme with input voltage feed−forward feature for wide input voltage range. A differential amplifier monitors the output voltage and feeds the high bandwidth error amplifier that generates the control signal for the pulse width modulation block. By adjusting the external compensation network, the system performance can be optimized based on the application parameters. The Low−Side FET turns ON after $V_{OUT}$ > 300 mV.

The switching frequency is set by PMBUS programming and can be synchronized to an external clock signal.

The high−side MOSFET current is sensed for the peak current limiting function and the output voltage is reduced in current limiting condition. Other protection functions include over temperature warning and shut−down, output voltage under− and over−voltage protections and warning, output over−current warning, and input over−voltage (all adjustable by PMBUS).

At the beginning of each switching cycle, the clock signal initiates a PWM signal to turn on the high−side MOSFET, and at the same time, the ramp signal starts to rise up. A reset pulse is generated by the comparator when the ramp signal intercepts the COMP signal. This reset pulse turns off the high−side MOSFET and turns on the low−side MOSFET until the next clock cycle comes. If the current limit is hit, the high− side MOSFET is turned off until the next PWM signal (cycle by cycle current limit protection). When certain fault conditions are met, the device can enter a protection mode (hiccup or latch−off) to further protect itself.

### PMBUS Address

A resistor between the ADDR pin and GND (with up to 1% tolerance) sets the PMBUS offset address, enabling 14 different possible addresses (see Table 1 for details). The offset address is added to an adjustable base address with PMBUS. The base section is programmable through MTP.

**Table 1. PMBUS™ ADDRESS SETTING**

| ADDR Resistor Value (kΩ) | Offset Address (h) | PMBUS Address (h) |
|---|---|---|
| 0 (short) | – | 0F |
| 0.845 | 00 | Base+00 |
| 1.3 | 01 | Base+01 |
| 1.78 | 02 | Base+02 |
| 2.32 | 03 | Base+03 |
| 2.87 | 04 | Base+04 |
| 3.48 | 05 | Base+05 |
| 4.12 | 06 | Base+06 |
| 4.75 | 07 | Base+07 |
| 5.49 | 08 | Base+08 |
| 6.19 | 09 | Base+09 |
| 6.98 | 0A | Base+0A |
| 7.87 | 0B | Base+0B |
| 8.87 | 0C | Base+0C |
| 10 | 0D | Base+0D |
| ≥12.4 | – | 0F |

### $V_{OUT}$ Voltage Pre−set

A resistor between the VSET pin and GND (with up to 1% tolerance) sets the output voltage without having to program it through PMBUS. It offers 15 different values (see table 2 for details). The $V_{OUT}$ setting can be overridden through PMBUS programming. The $V_{OUT}$ Voltage Pre−set feature can be enabled/disabled using MFR MODE (C8h) bit 0, which is enabled (0) by default.

**Table 2. $V_{OUT}$ PRESET SETTING**

| VSET Resistor Value (kΩ) | $V_{OUT}$ preset value (V) |
|---|---|
| Short | 0.6 |
| 0.845 | 0.6 |
| 1.3 | 0.9 |
| 1.78 | 0.95 |
| 2.32 | 1 |
| 2.87 | 1.05 |
| 3.48 | 1.2 |
| 4.12 | 1.25 |
| 4.75 | 1.5 |
| 5.49 | 1.8 |
| 6.19 | 2.1 |
| 6.98 | 2.5 |
| 7.87 | 3.3 |
| 8.87 | 5 |
| 10 & greater value | 0.8 |



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*Output Over−current Protection*

The FAN2510xx monitors the current in both the high−side and low−side MOSFETs, and offers several different sets of protections and warning:

*High−side FET Positive Cycle−by−cycle Peak Current Limit with Programmable Delay and Response*

- Limits the peak current in the high−side FET at each cycle to a level adjustable between 2 A and 62 A (using the IOUT_OC_FAULT_LIMIT command)
- The duration during which it is allowed to run in cycle−by− cycle current limitation before going into fault protection mode is adjustable from 0 to 10ms (using the IOUT_OC_FAULT_RESPONSE command)
- The fault protection mode is programmable, and can be chosen between “ignore without VOUT UVLO”, “ignore with VOUT UVLO”, “1−second hiccup” or “latch−off” (using the IOUT_OC_FAULT_RESPONSE command)
- An additional limit equal to 130% of the level set by IOUT_OC_FAULT_LIMIT immediately terminates switching if reached. This fault can be ignored: the FAN2510xx is latched off if IOUT_OC_FAULT_RESPONSE is “latch−off”, otherwise a 1−second hiccup is applied.

*Average Output Current Fault with Programmable Delay and Response*

- Based on the output current measured by the telemetry
- Does not limit the cycle−by−cycle current
- The threshold is adjustable between 1 A and 50 A (using the IOUT_AVG_FAULT_LIMIT command)
- The duration during which the FAN2510xx is allowed to run above the threshold before going into fault protection mode is adjustable from 0 to 10ms (using the IOUT_AVG_FAULT_RESPONSE command)
- The fault protection mode is programmable, and can be chosen between “ignore”, “1−second hiccup” or “latch−off” (using the IOUT_AVG_FAULT_RESPONSE command)

*Average Output Current Warning*

- Based on the output current measured by the telemetry
- The threshold is adjustable between 1 A and 64 A (using the IOUT_OC_WARN_LIMIT command)

*Low−side FET Negative Cycle−by−cycle Current Limit*

- Limits the negative low−side FET peak current at each cycle to a level adjustable between 10 A and 24 A (using the IOUT_UC_FAULT_LIMIT command)

*Output Voltage Monitoring and Protection*

The FAN2510xx monitors the output voltage and offers several different sets of protections and warnings:

*Under−voltage Protection*

- The threshold is adjustable as a percentage of the regulated output voltage, between 55% and 90% (using the PCT_VOUT_LIMIT command)
- The amount of filtering is adjustable (between 5μs and 10μs) and the fault response is programmable (between “ignore”, “1−second hiccup” or “latch−off”) using the VOUT_UV_FAULT_RESPONSE command

*Under−voltage Warning*

- Based on the output voltage measured by the telemetry
- The threshold is adjustable between 0.1 V and 5.5 V (using the VOUT_UV_WARN_LIMIT command)

*Over−voltage Protection*

- The threshold is adjustable as a percentage of the regulated output voltage, between 110% and 124% (using the PCT_VOUT_LIMIT command)
- The amount of filtering is adjustable (between 5μs and 10 μs) and the fault response is programmable (between “ignore”, “1−second hiccup” or “latch−off”) using the VOUT_OV_FAULT_RESPONSE command

*Over−voltage Warning*

- Switching stops when $V_{OUT}$ goes above this warning threshold, and resumes when back in regulation
- The threshold is adjustable as a percentage of the regulated output voltage, between 106% and 116% (using the PCT_VOUT_LIMIT command), and should be always set to the less than over−voltage protection threshold
- The behavior can be changed to turn on the low−side FET to actively pull $V_{OUT}$ down (by using MFR_MODE_SETTINGS).

*Power GOOD Signal and Pin*

- The PGOOD signal is held low during soft−start and soft−shutdown.
- The power good signal is high whenever $V_{OUT}$ is in regulation, after the end of soft−start
- The rising threshold is adjustable as a percentage of the regulated output voltage, between 84% and 98% (using the PCT_VOUT_PGOOD command)
- The falling threshold is adjustable as a percentage of the regulated output voltage, between 82% and 96% (using the PCT_VOUT_ PGOOD command)
- The power Good signal also goes low when $V_{OUT}$ is above the over−voltage protection threshold

*Output Voltage Margining*

FAN2510xx can be set for output voltage margin by applying positive (margin_high) or negative (margin_low) offset commands during operation.



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Scale loop changes and back to back margining for the output changes are not supported in FAN2510xx. New offset can be applied long enough until the previous margining is completed. In the same scale loop, the big output voltage changes with the highest slew rate is not recommended if OVP option is enabled during the margining.

*Input SYNC Function*

Two parts can be synchronized from an input source as master/slave with 0° (in phase) or 180° (out phase) phase shift. When device acts as master, it sends out a 45% duty cycle clock through SYNC pin with rising edge sync'd with its own switching cycle. Slave device switching node's rising edge lags behind either SYNC CLK's rising edge (in phase) or falling edge (out of phase) by 200 ns.

The slave is synchronized to SYNC CLK after it's validated over 64 clock cycles. Then, SYNC_CLK is compared to the internal clock. If outside the ±20% frequency window when compared to the internal clock, the device exits slave mode and relies on its internal clock rate. Refer to INTERLEAVE (Reg37h) section for additional setting details.

## Input Voltage Monitoring and Protection

The FAN2510xx monitors the input voltage and offers several different sets of protections and warnings:

*Over−voltage protection*

- The threshold is adjustable between 18 V and 24 V (using the VIN_OV_FAULT_LIMIT command)
- The amount of filtering is adjustable (between 5 µs and 10 µs) and the fault response is programmable (between "ignore", "recovery", "1−second hiccup" or "latch−off") using the VIN_OV_FAULT_RESPONSE command

*Turn−on Threshold*

The FAN2510xx only starts switching if VIN is above this threshold, adjustable between 4.5 V and 10.5 V (using the VIN_ON command). For less than 4.5 V, down to 3 V, external $V_{CC}$ should be used.

*Turn−off Threshold*

The FAN2510xx shuts down if VIN is below this threshold, adjustable between 4 V and 10 V (using the VIN_OFF command). For less than 4 V, down to 3 V, external $V_{CC}$ should be used.

*Temperature Monitoring and Protection*

The FAN2510xx monitors its die temperature and offers several different sets of protections and warnings:

*Over−temperature Protection*

- Based on the temperature measured by the telemetry
- The threshold is adjustable between 80°C and 160°C (using the OT_FAULT_LIMIT command)
- The fault protection mode is programmable, and can be chosen between "ignore", "recovery", "1−second hiccup" or "latch−off" (using the OT_FAULT_RESPONSE command)
- In case the die temperature reaches $T_{SHDN}$ (based on the analog sensor reading), the FAN2510xx immediately shuts of (including the LDO regulator), even if the fault response is set to "ignore"

*Over−temperature Warning*

- Based on the temperature measured by the telemetry
- The threshold is adjustable between 70°C and 150°C (using the OT_WARN_LIMIT command)

## Protection Summary

The FAN2510xx includes various protection features, with different behaviors and options. See Table 3 for a summary, and dedicated sections for more details about each one.



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**Table 3. SUMMARY OF PROTECTION FUNCTIONS**

| Protection name | Adjustability | Default Behavior | Options |
|---|---|---|---|
| Output overvoltage warning | PMBUS | HS FET and LS FET both turn off until back in regulation | HS FET turns off but LS FET turns on until back in regulation |
| Output overvoltage fault | PMBUS | Switching stops, then enters protection mode | Ignore, hiccup or latch−off; delay |
| Output under−voltage fault | PMBUS | Switching stops, then enters protection mode | Ignore, hiccup or latch−off; delay |
| Input overvoltage fault | PMBUS | Switching stops until back in range | Ignore, resume when back in range, hiccup or latch−off |
| Input under−voltage | PMBUS | Switching stops, part is reset | no |
| VCC under−voltage | no | Switching stops, part is reset | no |
| BOOT under−voltage | no | HS FET turns off, LS FET turns on regularly to refresh $V_{BOOT}$, until the fault clears | no |
| Average output current fault | PMBUS | Switching stops, then enters protection mode | Ignore, hiccup or latch−off; delay |
| Peak HS FET current fault | PMBUS | Cycle−by−cycle current limit, enters protection mode after delay | Ignore, hiccup or latch−off; delay |
| Peak HS FET current extreme fault | PMBUS | Enters protection mode | Ignore, hiccup or latch−off |
| Peak negative LS FET current fault | PMBUS | Cycle−by−cycle current limit | no |
| Switch node fault | no | Switching stops, then enters protection mode | Trim option to change to latch off |
| Over temperature Fault | PMBUS | Switching stops until back in range | Ignore, resume when back in range or latch−off |
| Umbrella Thermal shutdown | no | Switching stops and VCC LDO turns off, until back in range | no |
| Start−up fault (VOUT UV not met at the end of timer) | PMBUS | Switching stops, then enters protection mode | Ignore, hiccup or latch−off |



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### Telemetry

The FAN2510xx constantly measures its input voltage, input current, output voltage, output current and die temperature and reports it in dedicated PMBUS registers. Each measured value is refreshed every 900 μs.

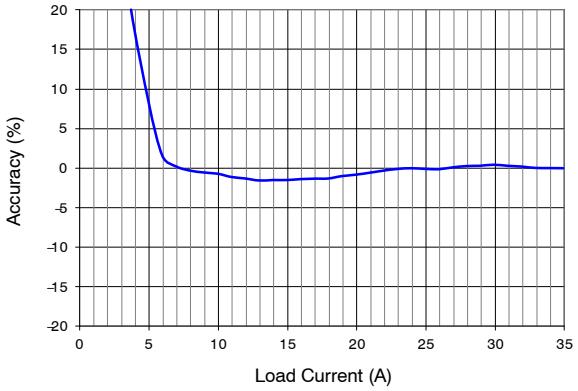


**Figure 12. Typical $I_{OUT}$ Telemetry Accuracy**

*PMBUS General Description*

The PMBUS specification can be found at www.pmbus.org. FAN2510xx support both the 100 kHz and 400 kHz bus timing requirements. Communication over the PMBUS interface supports Packet Error Checking (PEC). If the master provides the clock pulses for the PEC byte, PED is used. If the additional clock pulses are not present before a STOP, the PEC is not used. PMBUS has several transaction formats. The formats that are supported in FAN2510xx are listed below:

*PMBUS Send Byte*

The send byte transaction is used to send a simple command to the device. A send byte transaction transfers a command with no data. The CLEAR_FAULTS command that clears the current fault flags present in the system is an example of such a command. A start bit, followed by the 7−bit slave address and finished by a write bit (0−value) to indicate a write make up the first stage of the transaction. If the slave ACKs the address, then the host sends the 8−bit command followed by a stop condition. The format is given below.

PMBUS Send Byte

| 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | P |

*PMBUS Write Byte*

The write byte transaction is used to send single byte data to the chip. The OPERATION command that configures the operation of the device is an example of this type of transaction. Similar to the send byte transaction above, the series of start bit, 7−bit slave address with write bit (0−value), command byte, and finally the 8−bit data byte. The format is given below.

PMBUS Write Byte

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | DATA_BYTE | A | P |

*PMBUS Write Word*

The write word transaction is used to send a single word of data (two bytes) to the chip. The TON_DELAY command is an example of such a transaction. Similar to the write byte command, the only difference is that after the third acknowledge (the low data byte) the high byte is sent in addition.

PMBUS Write Word

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | DATA_BYTE LOW | A | DATA_BYTE HIGH | A | P |



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*PMBUS Read Byte*

The read byte starts out like a normal I2C write transaction by sending the address and the write bit. The second byte contains the command code, then a repeated start is sent, and following that is the address and read bit send the signal to the device to return data for the specified command code. The slave responds by transmitting the byte value requested.

PMBUS Read Byte

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | Sr | SLAVE ADDRESS | Rd | A | DATA BYTE | N | P |

*PMBUS Read Word*

The read word transaction also starts out like a normal I 2C write transaction by sending the address and the write bit. The second byte contains the command code, then a repeated start is sent, and following that is the address and read bit signaling the device to return data for the specified command code. The slave responds by transmitting the value requested low byte first and high byte last.

PMBUS Read Word

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | Sr | SLAVE ADDRESS | RD | A | DATA BYTE | A | DATA BYTE HIGH | N | P |

*PMBUS Block Write*

The Block Write begins with a slave address and a write condition. After the command code the host issues a byte count which describes how many more bytes will follow in the message. FAN2510xx allows only 1 byte. The byte count field can only have the value 01, followed by the one byte of data.

PMBUS Block Write

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | BYTE COUNT = 1 | A | DATA BYTE | A | P |

*PMBUS Block Read*

A Block Read differs from a block write in that the repeated START condition exists to satisfy the requirement for a change in the transfer direction. A NACK immediately preceding the STOP condition signifies the end of the read transfer.

FAN2510xx allows only 1 byte. The byte count field can only have the value 01, followed by the one byte of data.

PMBUS Block Read

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COM-MAND_CODE | A | Sr | SLAVE ADDRESS | RD | A | BYTE COUNT = 1 | A | DATA BYTE | A | P |

*Packet Error Checking (PEC)*

PEC is optionally implemented in PMBUS devices, but is highly recommended due to the critical nature of data validity in power−management systems. Packet Error Code (also PEC) bytes are generated using the popular CRC−8 algorithm that is based on performing XOR operations on the input bit stream with a fixed CRC polynomial. The PEC byte is calculated on all bytes in the I2C transaction including device address and read/write. PEC does not include start, stop, ACK/NACK, and repeated start bits.

*PMBUS Send byte with PEC:*

PMBUS Send Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | PEC BYTE | A | P |

*PMBUS Write Byte with PEC:*

PMBUS Write Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | DATA_BYTE | A | PEC BYTE | A | P |



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*PMBUS Write Word with PEC:*

PMBUS Write Word with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | DATA_BYTE LOW | A | DATA_BYTE HIGH | A | PEC BYTE | A | P |

*PMBUS Read Byte with PEC:*

PMBUS Read Byte with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | Sr | SLAVE ADDRESS | RD | A | DATA BYTE | A | PEC BYTE | A | P |

*PMBUS Read Word with PEC:*

PMBUS Read Word with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | Sr | SLAVE ADDRESS | RD | A | DATA BYTE LOW | A | DATA BYTE HIGH | A | PEC BYTE | A | P |

*PMBUS Block Write with PEC:*

PMBUS Block Write with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | BYTE COUNT =1 | A | DATA BYTE | A | PEC BYTE | A | P |

*PMBUS Block Read with PEC:*

PMBUS Block Read with PEC

| 1 | 7 | 1 | 1 | 8 | 1 | 1 | 7 | 1 | 1 | 8 | 1 | 8 | 1 | 8 | 1 | 1 |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| S | SLAVE ADDRESS | WR | A | COMMAND_CODE | A | Sr | SLAVE ADDRESS | RD | A | BLOCK COUNT = 1 | A | DATA BYTE | A | PEC BYTE | A | P |



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**PMBUS COMMAND LIST** (Note 7)

| Address | PMBUS Command Name | Type | Range | Step | Default Value | Default | Comments |
|---|---|---|---|---|---|---|---|
| 01h | OPERATION | R/W | – | – | 0 | Immediate off | |
| 02h | ON_OFF_CONFIG | R/W | – | – | 8'h 17 | Turn on with enable pin | |
| 03h | CLEAR_FAULTS | Write | – | – | | – | |
| 10h | WRITE_PROTECT | R/W | – | – | 8'h 00 | Enable all writes | |
| 15h | STORE_USER_ALL | Write | – | – | | – | |
| 16h | RESTORE_USER_ALL | Write | – | – | | – | |
| 19h | CAPABILITY | Read | – | – | | B0h | PEC supported, 400 kHz max, SMBALERT# supported, linear formats, AVSBUS not supported |
| 1Bh | SMBALERT_MASK | Write | – | – | | No alert masked | All faults can be individually masked |
| 20h | VOUT_MODE | Read | – | 1.953 mV | | 17h | |
| 21h | VOUT_COMMAND | R/W | 0.5 V to 5.5 V | 1.953 mV | | – | |
| 24h | VOUT_MAX | R/W | 0.5 V to 5.5 V | 1.953 mV | 16'h 0B00 | 5.5 V | |
| 25h | VOUT_MARGIN_ HIGH | R/W | 0.5 V to 5.5 V | 1.953 mV | 16'h 06CD | 3.4 V | |
| 26h | VOUT_MARGIN_ LOW | R/W | 0.5 V to 5.5 V | 1.953 mV | 16'h 0667 | 3.2 V | |
| 27h | VOUT_TRANSI-TION_RATE | R/W | 0.203 to 9.375 mV/μs | 1.953 mV | 16'h D00D | 0.203 mV/μs | 4 options allowed: 0.203, 1.953, 2.9218, 9.375 mV/μs |
| 29h | VOUT_SCALE_LOOP | R/W | 0.25 to 1 | 0.25 | 16'h F002 | 0.5 | 3 options allowed: 0.25, 0.5, 1 |
| 33h | FREQUENCY_SWITCH | R/W | 200 kHz to 1.8 MHz | 50−100 kHz | 16'h 092C | 600 kHz | |
| 35h | VIN_ON | R/W | 3 V to 10.5 V | 0.5 V | 16'h F80C | 6 V | |
| 36h | VIN_OFF | R/W | 2.5 V to 10 V | 0.5 V | 16'h F80B | 5.5 V | |
| 37h | INTERLEAVE | R/W | 4 options | | 16'h 0000 | Standalone | Standalone, Master, Slave 0°, Slave 180° |
| 41h | VOUT_OV_FAULT_ RESPONSE | R/W | ignore, latch−off, hiccup | – | 8'h 40 | Latch−off | Adjustable filter |
| 43h | VOUT_UV_WARN_LIMIT | R/W | 0.1 V to 5.5 V | 1.953 mV | 16'h 0067 | 0.2 V | |
| 45h | VOUT_UV_FAULT_ RE-SPONSE | R/W | Ignore, latch−off, hiccup | – | 8'h 40 | Latch−off | Adjustable filter |
| 46h | IOUT_OC_FAULT_LIMIT | R/W | 2 A to 62 A | 2 A | 16'h 081B | 54 A | Sets cycle−by−cycle peak current limit in HSFET |
| 47h | IOUT_OC_FAULT_ RE-SPONSE | R/W | 4 options | – | 8'h 80 | Latch−off | Ignore w/o $V_{OUT}$ uv, ignore with $V_{OUT}$ uv, latch−off, hiccup |
| 4Ah | IOUT_OC_WARN_LIMIT | R/W | 1 A to 64 A | 62.5 mA | 16'h E200 | 32 A | Sets average output current warn |
| 4Bh | IOUT_UC_FAULT_LIMIT | R/W | 10 A to 24 A | 2 A | 16'h 000E | 14 A | Sets negative cycle−by−cycle peak current limit in LSFET |
| 4Fh | OT_FAULT_LIMIT | R/W | 80°C to 160°C | 1°C | 16'h 008C | 140°C | |
| 50h | OT_FAULT_RESPONSE | R/W | Ignore, hiccup, latch−off, recovery | – | 8'h C0 | recovery | Adjustable filter |
| 51h | OT_WARN_LIMIT | R/W | 70°C to 150°C | 1°C | 16'h 0073 | 115°C | |
| 55h | VIN_OV_FAULT_LIMIT | R/W | 18 V to 24 V | 2 V | 16'h 080A | 20 V | |
| 56h | VIN_OV_FAULT_ RESPONSE | R/W | ignore, hiccup, latch−off, recovery | – | 8'h C0 | recovery | Adjustable filter |
| 60h | TON_DELAY | R/W | 1 ms to 10 ms | 1 ms | 16'h 0001 | 1 ms | |
| 61h | TON_RISE | R/W | 1 ms to 20 ms | 1 ms | 16'h 0005 | 5 ms | |
| 62h | TON_MAX_FAULT_LIMIT | R/W | 0 ms to 50 ms | 2 ms | 16'h 0806 | 12 ms | |



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**PMBUS COMMAND LIST** (Note 7) (continued)

| Address | PMBUS Command Name | Type | Range | Step | Default Value | Default | Comments |
|---|---|---|---|---|---|---|---|
| 63h | TON_MAX_FAULT_RESPONSE | R/W | ignore, latch−off, hiccup | | 8'h 80 | Latch−off | |
| 64h | TOFF_DELAY | R/W | 0 ms to 10 ms | 1 ms | 16'h 0000 | 0 ms | |
| 65h | TOFF_FALL | R/W | 1 ms to 20 ms | 1 ms | 16'h 0005 | 5 ms | |
| 78h | STATUS_BYTE | Read | – | – | | – | |
| 79h | STATUS_WORD | Read | – | – | | – | |
| 7Ah | STATUS_VOUT | Read | – | – | | – | |
| 7Bh | STATUS_IOUT | Read | – | – | | – | |
| 7Ch | STATUS_INPUT | Read | – | – | | – | |
| 7Dh | STATUS_TEMPERATURE | Read | – | – | | – | |
| 7Eh | STATUS_CML | Read | – | – | | – | |
| 80h | STATUS_MFR_SPECIFIC | Read | – | – | | – | |
| 88h | READ_VIN | Read | 0 to 25 V | 31.25 mV | | – | |
| 89h | READ_IIN | Read | 0 to 64 A | 62.5 mA | | – | |
| 8Bh | READ_VOUT | Read | 0 to 5.5 V | 1.953 mV | | – | |
| 8Ch | READ_IOUT | Read | 0 to 64 A | 62.5 mA | | – | |
| 8Dh | READ_TEMPERATURE | Read | −40°C to 175°C | 1°C | | – | |
| 95h | READ_FREQ | Read | 200 kHz to 2.5 MHz | 1 kHz | | | |
| 98h | PMBUS_REVISION | Read | – | – | 8'h 33 | 33h | PMBUS rev 1.3 |
| 99h | MFR_ID | Block R/W | – | – | 16'h 3001 | 3001h | Block R/W format,<br>The LSB byte can only be 01(h) |
| 9Ah | MFR_MODEL | Block R/W | – | – | 16'h 3001 | 3001h | Block R/W format,<br>The LSB byte can only be 01(h) |
| 9Bh | MFR_REVISION | Block Read | – | – | 16'h 4X01 | 4X01h | Block R/W format,<br>The LSB byte can only be 01(h) |
| 9Eh | MFR_SERIAL | Block R/W | – | – | 16'h 0001 | 0001h | Block R/W format,<br>The LSB byte can only be 01(h) |
| A4h | MFR_VOUT_MIN | Read | – | – | 16'h 0100 | 0.5 | |
| A5h | MFR_VOUT_MAX | Read | – | – | 16'h 0B01 | 5.5 | |
| ADh | IC_DEVICE_ID | Block Read | – | – | 16'h 4001 | 4001h | Block R format,<br>The LSB byte can only be 01(h) |
| AEh | IC_DEVICE_REV | Block Read | – | – | 16'h 4001 | 4001h | Block R format,<br>The LSB byte can only be 01(h) |
| C4h | IOUT_AVG_FAULT_RESPONSE | R/W | ignore, hiccup, latch−off | | 8'h 80 | Latch−off | Adjustable delay |
| C5h | IOUT_AVG_FAULT_LIMIT | R/W | 1 A to 64 A | 62.5 mA | 16'h E2D0 | 45 A | Sets OCP average current limit |
| C6h | PCT_VOUT_LIMIT | R/W | 110% to 124% | 2% | 16'h 06E0 | 116% | Replaces VOUT_OV_FAULT_LIMIT |
| | | R/W | 106% to 116% | 2% | | 108% | Replaces VOUT_OV_WARN_LIMIT |
| | | R/W | 55% to 90% | 5% | | 75% | Replaces VOUT_UV_FAULT_LIMIT |
| C7h | PCT_VOUT_PGOOD | R/W | 84% to 98% | 2% | 8'h 19 | 90% | Replaces POWER_GOOD_ON |
| | | R/W | 82% to 96% | 2% | | 84% | Replaces POWER_GOOD_OFF |



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**PMBUS COMMAND LIST** (Note 7) (continued)

| Address | PMBUS Command Name | Type | Range | Step | Default Value | Default | Comments |
|---|---|---|---|---|---|---|---|
| C8h | MFR_MODE_SETTINGS | R/W | CCM, Enable/Disable VSET pin, turn on/off LS FET at OV_WARN | – | 8'h A0 | CCM, Enable VSET pin, LS FET OFF at OV_WARN | Enables VSET pin setting for VOUT, and enables LSFET turn–on at OV_WARN.<br>Bits 7:4 are used for IMON HSD RIIN programmability. |
| C9h | MFR_PMBUS_BASE | R/W | | | 7'h10 | 10h | Sets the PMBUS base address |
| CAh | MFR_ID2 | R/W | | | 16'h 4F4E | 4F4Eh | R/W Word format,<br>MFR_ID2 register is added for customers who need 16 bits of MFR ID. MTP bits allocated for all 16 bits |

7. The regulation should be always disabled when:
   – Writing commands that change device settings.
   – Accessing the MTP using STORE_USER_ALL & RESTORE_USER_ALL commands.
   – The device should be discarded, if #ALERTB pad is pulled low during startup and indicates the MTP programming Fault (Bit#1 of STATUS_MFR_SPECIFIC).

## PMBUS Commands Details

### OPERATION (01h)

The OPERATION command is one byte command used to configure the operational state of the converter, in conjunction with input from the ENABLE pin.

The OPERATION command is used to:

- Turn the PMBUS device output on and off with commands sent over the PMBUS
- Select the margin state of the device (margin off, margin high, margin low)
- Select whether fault conditions caused by margining are ignored or acted upon
- Select whether the converter powers down immediately or follows the programmed TOFF_DELAY and TOFF_FALL commands when commanded to turn off the output

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

| Operation Command Bit Number | | | | | Device State/Response | | | |
|---|---|---|---|---|---|---|---|---|
| Bit 7 ON/ OFF Behavior | Bit 6 Turn OFF Behavior | Bit <5:4> Voltage Command Source | Bit <3:2> Margin Fault Response | Bit < 1:0> Not Used | On/Off | Power OFF Behavior | Output Voltage Command Source | Device Response |
| R/W | R/W | R/W | R/W | R (reads 00 only) | | | | |
| 0 | 0 | XX | XX | XX | Off | Immediate Off | N/A | Immediate OFF |
| 0 | 1 | XX | XX | XX | Off | Power down sequencing | N/A | Use TOFF_DELAY & TOFF_FALL for shutdown |
| 1 | X | 01 | 01 | XX | On | | VOUT_MARGIN_LOW | Ignore faults when margined |
| 1 | X | 01 | 10 | XX | On | N/A | VOUT_MARGIN_LOW | Act on faults when margined |
| 1 | X | 10 | 01 | XX | On | N/A | VOUT_MARGIN_HIGH | Ignore faults when margined |
| 1 | X | 10 | 10 | XX | | | VOUT_MARGIN_HIGH | Act on faults when margined |
| 1 | X | 00 | XX | XX | | | VOUT_COMMAND | Regulate to VOUT commanded value |

| List if all Invalid Data Operation Bits<7:2> |
|---|
| 100100 |



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| |
|---|
| 110100 |
| 100111 |
| 110111 |
| 101000 |
| 111000 |
| 101011 |
| 111011 |

NOTE: Invalid data fault flag gets set if invalid data is sent. Any data other than the data listed above is accepted.

### ON_OFF_CONFIG (02h)

The ON_OFF_CONFIG command is one byte command. This command configures the combination of ENABLE pin input and serial bus commands needed to turn the unit on and off. This includes how the unit responds when power is applied. The default response for any PMBUS device is specified by the device manufacturer.

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

**GENERIC STRADDLE TABLE**

| Default | R/W access | Bit Number | Purpose | Bit Value | Meaning |
|---|---|---|---|---|---|
| 000 | R/W | [7:5] | | 0 | Reserved |
| 1 | R/W | 4 | Sets the default to either operate any time power is present or for the on/off to be controlled by ENABLE pin and serial bus commands | 0 | Chip turns on when VCC is present |
| | | | | 1 | Chip does not turn on until commanded by the ENABLE pin and OPERATION command (as programmed in bits [3:0]) |
| 0 | R/W | 3 | Controls how the unit responds to commands received via the serial bus | 0 | Bit [7] of OPERATION command is ignored |
| | | | | 1 | Bit[7] of the OPERATION command needs to be high and depending on Bit [2] of ON_OFF_CONFIG, the unit may also require the ENABLE pin to be asserted for the chip to start. |
| 1 | R/W | 2 | Controls how the unit responds to the ENABLE pin | 0 | Unit ignores the ENABLE pin (on/off controlled only by the OPERATION command) |
| | | | | 1 | The ENABLE pin needs to be asserted to start the unit.<br>Depending on Bit [3] of ON_OFF_CONFIG, the OPERATION command may also be required to instruct the chip to start |
| 1 | R/W | 1 | Polarity of the ENABLE pin | 0 | Active low (Pull pin low to turn on the chip) – Not Supported |
| | | | | 1 | Active high (Pull high to turn on the chip) |
| 1 | R/W | 0 | ENABLE pin action when commanding the unit to turn off | 0 | Use the programmed turn off delay (TOFF_DELAY) and fall time (TOFF_FALL) |
| | | | | 1 | Turn off the output immediately |

| ON_OFF_CONFIG Valid data Bits<4:1> | Turn on behavior |
|---|---|
| 0XX1 | Turn on any time power is up |
| 1011 | Turn on with ENABLE pin ( Default setting) |
| 1101 | Turn on with the PMBus bit (Bit 7 OPERATION command) |
| 1111 | Tunr on when both ENABLE pin and PMBus bit #7 of OPERATION command are high |



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### CLEAR_FAULTS (03h)

The CLEAR_FAULTS command is used to clear any fault bits that have been set. This command clears all bits in all status registers simultaneously. At the same time, the device negates (clears, releases) its SMBALERT# signal output if the device is asserting the SMBALERT# signal.

The CLEAR_FAULTS command does not cause a unit that has latched off for a fault condition to restart. Any device that has shut down due to a fault condition remains off until:

- A RESET signal (if one exists) is asserted,
- The output is commanded through the CONTROL pin, the OPERATION command, or the combined action of the CONTROL pin and OPERATION command, to turn off and then to turn back on, or
- Bias power (VCC) is removed from the PMBUS device

If the fault is still present when the bit is cleared, the fault bit shall immediately be set again and the host notified by the usual means.

#### Clearing Individual Bits

Any or all of the bits in any status register except STATUS_BYTE and STATUS_WORD can be directly cleared by issuing the status command with one data byte that is written. The data byte is a binary value. A 1 in any bit position indicates that bit is to be cleared, if set, and unchanged if not set. Examples of data bytes:

- 00010000b indicates that bit [4] is to be cleared and all other bits are to be unchanged,
- 01100010b indicates that bits [6], [5], and [1] are to be cleared and all other bits are to be unchanged
- 11111111b, or FFh, indicates all bits are to be cleared

### WRITE_PROTECT (10h)

The WRITE_PROTECT command is used to control writing to the PMBUS device. The intent of this command is to provide protection against accidental changes. This command is not intended to provide protection against deliberate or malicious changes to a device's configuration or operation. All supported commands may have their parameters read, regardless of the WRITE_PROTECT settings. This command has one data byte, described in below table.

If a device receives a data byte that is not listed in the table, then the device shall treat this as invalid data, declare a communications fault. If a PMBUS device receives unsupported data, the response is that the device shall:

- Flush or ignore the received command code and any received data,
- Set the CML bit in the STATUS_BYTE,
- Set the Invalid or Unsupported Data Received bit in the STATUS_CML register

| Data Byte Value | Meaning |
|---|---|
| 1000_0000 | Disable all writes except to the WRITE_PROTECT command |
| 0100_0000 | Disable all writes except to the WRITE_PROTECT and OPERATION commands |
| 0010_0000 | Disable all writes except to the WRITE_PROTECT, OPERATION, ON_OFF_CONFIG and VOUT_COMMAND commands |
| 0000_0000 | Enable writes to all commands (default) |

Any other data other than given in the above table will cause an invalid data fault. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

### STORE_USER_ALL (15h)

The STORE_USER_ALL command instructs the PMBUS device to copy the entire contents of the Operating Memory to the matching locations in the non−volatile User Store memory (MTP). It is permitted to use the STORE_USER_ALL command while the device is operating. However, the device may be unresponsive during the copy operation with unpredictable, undesirable or even catastrophic results. This command is not allowed until the initial MTP reading is done during startup. This command, once received, takes ~110 ms to complete successfully.

This command has no data bytes, and it is write only.


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### RESTORE_USER_ALL (16h)

The RESTORE_USER_ALL command instructs the PMBUS device to copy the entire contents of the non−volatile User Store memory (MTP) to the matching locations in the Operating Memory. The values in the Operating Memory are overwritten by the value retrieved from the User Store. This command is allowed only when output is disabled. This command is not allowed until the initial MTP reading is done during startup. This command once received takes ~2.5 ms to complete successfully.

This command has no data bytes, and it is write only.

### CAPABILITY (19h)

This command provides a way for a host system to determine some key capabilities of a PMBUS device. There is one data byte formatted as shown in the below Table. This command is read only and returns 1011_0000.

| Bits | R/W Access | Default | Description | Value | Meaning |
|---|---|---|---|---|---|
| 7 | Read only | 1 | Packet Error Checking | 0 | Packet Error Checking not supported |
| | | | | 1 | Packet Error Checking is supported |
| 6:5 | Read only | 01 | Maximum Bus Speed | 00 | Maximum supported bus speed is 100 kHz |
| | | | | 01 | Maximum supported bus speed is 400 kHz |
| | | | | 10 | Maximum supported bus speed is 1 MHz |
| | | | | 11 | Reserved |
| 4 | Read only | 1 | ALERT# | 0 | The device does not have a ALERT# pin and does not support the PMBus Alert Response Protocol |
| | | | | 1 | The device does have a ALERT# pin and supports the PMBus Alert Response Protocol and ARA if base address ≥40h. With multiple slaves responding during arbitration, the device does not release the SDA signal if a lower address slave responds. |
| 3 | Read only | 0 | Numeric Format | 0 | Numeric data is in LINEAR11, ULINEAR16, SLINEAR16 or DIRECT format |
| | | | | 1 | Numeric data is in IEEE Half precision Floating Point Format |
| 2 | Read only | 0 | AVS Bus Support | 0 | AVS Bus not supported |
| | | | | 1 | AVS Bus supported |
| 1:0 | Read only | 00 | Reserved | | Reserved |

### SMBALERT_MASK (1Bh)

The SMBALERT_MASK command may be used to prevent a warning or fault condition from asserting the SMBALERT# signal. The command format used to block a status bit or bits from causing the SMBALERT# signal to be asserted. The bits in the mask byte align with the bits in the corresponding status register. For example if the STATUS_TEMPERATURE command code were sent with the mask byte 01000000b, then an Over temperature Warning condition would be blocked from asserting SMBALERT#.

### VOUT_MODE (20h)

Supports Linear Mode only: ULINEAR16 Format. The ULINEAR16 format is given below

| Mode | Bit[7] | Bit[6:5] | Bit[4:0] (Parameter) |
|---|---|---|---|
| ULINEAR16 | X | 00b | Five bit two's compliment exponent for the mantissa delivered as the data bytes for an output voltage related command |

VOUT_MODE command is used for VOUT_COMMAND, VOUT_MAX, VOUT_MARGIN_HIGH, VOUT_MARGIN_LOW, VOUT_UV_WARN_LIMIT, and READ_VOUT commands.



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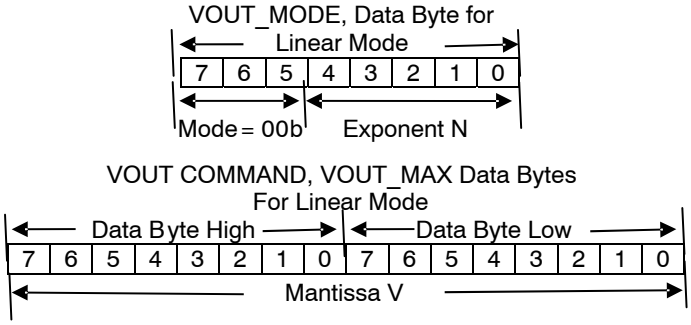


The Mode bits are set to 000b. The Voltage, in Volts is calculated from the equation: $Voltage = V\,X\,2^{N}$

Where, Voltage is the parameter of interest in Volts; V is a 16 bit unsigned binary integer, and N is a 5 bit two's compliment binary integer. The exponent N is fixed −9, VOUT step size = 1.953 mV with 10 bit DAC. Attempt to write to VOUT_MODE command will cause an invalid data fault. VOUT_MODE Read back is 17(hex).

### VOUT_COMMAND (21h)

Sets the value of VOUT when the OPERATION command is configured for PMBUS nominal operation. The VOUT_COMMAND follows the ULINEAR16 format. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

| Range | Resolution | Default |
|---|---|---|
| 0.5–5.5 V | 1.953 mV | – V |

### RECOMMENDED VOUT_SCALE_LOOP SETTING

| VOUT Range | VOUT_SCALE_LOOP |
|---|---|
| 0.5–1.99 V | F004 |
| 1.992–3.99 V | F002 |
| 4.0–5.5 V | F001 |

Exponent is FIXED −9 and Mantissa Range is 256 to 2816. Any data outside this range flags is an invalid data fault. If MFR_MODE(C7hex) Bit#0 is set low the VSET pin sets the default value of this register. Some Examples for setting the VOUT are given below.

| VOUT Voltage | PMBUS DATA |
|---|---|
| 0.8 V | 019A(hex) |
| 1.0 V | 0200(hex) |
| 1.5 V | 0300(hex) |
| 2.0 V | 0400(hex) |
| 3.3 V | 069A(hex) |
| 5.0 V | 0A00(hex) |
| 5.5 V | 0B00(hex) |

### VOUT_MAX (24h)

Sets the maximum allowed VOUT target regardless of any other commands or combinations. The VOUT_MAX follows the ULINEAR16 format. If mantissa is not within the range 256 to 2817(d), it flags an invalid data fault. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

| Range | Resolution | Default |
|---|---|---|
| 0.5–5.5 V | 1.953 mV | 5.5 V |

### VOUT_MARGIN_HIGH (25h)

Sets the value of VOUT when the OPERATION command is configured for margin high. The VOUT_MARGIN_HIGH follows the ULINEAR16 format. If the data is lower or equal to VOUT_MARGIN_LOW setting, it flags an invalid data fault. Also if mantissa is not within the range 256 to 2816, it flags an invalid data fault. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

| Range | Resolution | Default |
|---|---|---|
| 0.5–5.5 V | 1.953 mV | 3.4 V |

### VOUT_MARGIN_LOW (26h)

Sets the value of VOUT when the OPERATION command is configured for margin low. The VOUT_MARGIN_LOW follows the ULINEAR16 format. If the data is higher or equal to VOUT_MARGIN_HIGH setting, it flags an invalid data fault. Also if mantissa is not within the range 256 to 2816, it flags an invalid data fault. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

| Range | Resolution | Default |
|---|---|---|
| 0.5–5.5 V | 1.953 mV | 3.2 V |



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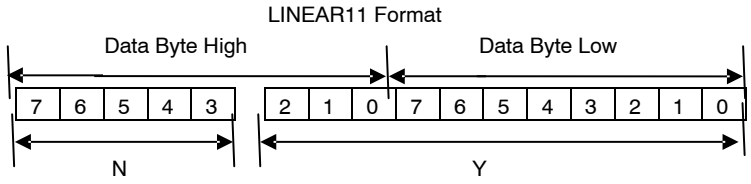
### VOUT_TRANSITION_RATE (27h)

When a PMBUS device receives either a VOUT_COMMAND or OPERATION (Margin High, Margin Low, Margin Off) that causes the output voltage to change, this command sets the rate in mV/µs at which the output should change voltage. This commanded rate of change does not apply when the unit is commanded to turn on or to turn off.

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The VOUT_TRANSITION_RATE command has two data bytes encoded in LINEAR11 format as shown below (5bits signed exponent and 11 bits mantissa)




The relation between Y, N and the real world value is

$X = Y \bullet 2^N$

Where X is the real world value; Y is the 11 bit, two's compliment integer, and N is a 5 bit, two's compliment integer Exponent N is Fixed −6 ⇒11010(b) (Equivalent LSB = 15.625 µV/µs)

Mantissa Y: Only 4 options allowed 00D, 07D, 0BB, 258(hex).

All the options allowed are given below. The default is 0.203 mV/µs. Attempting to write a value other than the values listed in the below table will cause an invalid data fault.

| Transition Rate in mV/µs | PMBUS Data(hex) |
|---|---|
| 0.203 | D00D |
| 1.953 | D07D |
| 2.9218 | D0BB |
| 9.375 | D258 |

### VOUT_SCALE_LOOP (29h)

The VOUT_SCALE_LOOP sets the output sense scaling ratio for the main control loop. FAN2510xx supports only 3 options/ratios: 1, 0.5, 0.25. Attempting to write a value other than the values listed in the below table will cause an invalid data fault.

| PMBUS Data(hex) | Gain |
|---|---|
| F001 | 0.25 |
| F002 | 0.5 |
| F004 | 1 |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The VOUT_SCALE_LOOP command has two data bytes encoded in LINEAR11 format:

- Exponent N is Fixed 11110(b) (Equivalent LSB = 0.25)
- Mantissa Y: Only 3 options allowed 01, 02, 04(hex)

### FREQUENCY_SWITCH (33h)

The FREQUENCY_SWITCH command sets the switching frequency in kHz. This command has two data bytes encoded in LINEAR11 format. Exponent N is Fixed 00001(b) (Equivalent LSB = 2 kHz)

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

| Range | Resolution | Default |
|---|---|---|
| 200−1800 kHz | 2 kHz | 600 kHz |



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All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault.

| Frequency (kHz) | PMBUS Data (hex) |
|---|---|
| 200 | 0864 |
| 250 | 087D |
| 300 | 0896 |
| 350 | 08AF |
| 400 | 08C8 |
| 450 | 08E1 |
| 500 | 08FA |
| 550 | 0913 |
| 600 | 092C |
| 650 | 0945 |
| 700 | 095E |
| 750 | 0977 |
| 800 | 0990 |
| 850 | 09A9 |
| 900 | 09C2 |
| 950 | 09DB |
| 1000 | 09F4 |
| 1050 | 0A0D |
| 1100 | 0A26 |
| 1150 | 0A3F |
| 1200 | 0A58 |
| 1300 | 0A8A |
| 1400 | 0ABC |
| 1500 | 0AEE |
| 1600 | 0B20 |
| 1700 | 0B52 |
| 1800 | 0B84 |


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**VIN_ON (35h)**

The VIN_ON command sets the value of $V_{IN}$ in Volts at which the chip should start the power conversion. The two data bytes are encoded in LINEAR11 format as shown below. Exponent is in 2's compliment format and mantissa is unsigned binary. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The format, supported range and resolution are given in the below table.

| Data Byte High | | | | | | | | Data Byte Low | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|---|
| 5 Bit Exponent | | | | | 11 Bit Unsigned Mantissa | | | | | | | | | | |
| 4 | 3 | 2 | 1 | 0 | 10 | 9 | 8 | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| R | R | R | R | R | R | R | R | R | R | R | R/W | R/W | R/W | R/W | R/W |
| Default Exponent | | | | | Default Mantissa | | | | | | | | | | |
| 1 | 1 | 1 | 1 | 1 | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 1 | 0 | 0 | 0 |

Default VIN UVLO Rising Threshold: 6 V

VIN UVLO Rising Threshold Range: 3.0 V to 10.5 V VIN_IN Exponent: Fixed −1 (Equivalent LSB = 0.5 V)

All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault. If $V_{IN}$ "on" data is lower or equal to $V_{IN}$ "off"; the invalid data flag is set. If the input voltage does not reach the rising VIN UVLO Threshold after the VCC Enable Threshold is crossed, a VIN UVLO Fault will trigger.

| PMBUS data | VIN ON Threshold (V) |
|---|---|
| F806 | 3 |
| F807 | 3.5 |
| F808 | 4 |
| F809 | 4.5 |
| F80A | 5 |
| F80B | 5.5 |
| F80C | 6 |
| F80D | 6.5 |
| F80E | 7 |
| F80F | 7.5 |
| F810 | 8 |
| F811 | 8.5 |
| F812 | 9 |
| F813 | 9.5 |
| F814 | 10 |
| F815 | 10.5 |

**VIN_OFF (36h)**

The VIN_OFF command sets the value of the input voltage in volts at which the unit once operation has started should stop power conversion. The two data bytes are encoded in LINEAR11 format. Exponent is in 2's compliment format and mantissa is unsigned binary. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The format is same as VIN_ON command. The range and resolution are given in the below table.

| Range | Resolution | Default |
|---|---|---|
| 2.5–10.0 V | 0.5 V | 6 V(F80C (hex)) |

All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault. If Vin_off data is higher than Vin_on the invalid data flag is set.

| PMBUS data | VIN OFF Threshold (V) |
|---|---|
| F805 | 2.5 |
| F806 | 3 |
| F807 | 3.5 |
| F808 | 4 |
| F809 | 4.5 |
| F80A | 5 |
| F80B | 5.5 |
| F80C | 6 |
| F80D | 6.5 |
| F80E | 7 |
| F80F | 7.5 |
| F810 | 8 |
| F811 | 8.5 |
| F812 | 9 |
| F813 | 9.5 |
| F814 | 10 |



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### INTERLEAVE (37h)

The INTERLEAVE command is used to arrange multiple units to facilitate paralleling of multiple units. The Interleave is a 16− bit command with 3 components (plus 4 unused bits in front):

- Group ID (4 bits)
- Number of units in the group (4 bits)
- Interleave order of the unit in the group (4 bits)

The following options are supported by FAN251030:

*Standalone:*

Group ID = 0, Number of units = 0, Interleave order = 0 [0000 0000 0000 0000] ⇒ unit is neither master nor slave, does not drive the SYNC pin and ignores any clock on SYNC pin.

For synchronization

*Master:*

Group ID = 1, Number of units = 0, Interleave order = 0 [0000 0001 0000 0000] ⇒ unit is master, and sends its internal clock out on the SYNC pin.

*Slave:*

- Group ID = 1, Number of units = 2, Interleave order = 0 [0000 0001 0010 0000] ⇒ the unit operates in−phase to the clock applied on its SYNC (or operates on its own internal clock if no clock on SYNC)
- Group ID = 1, Number of units = 2, Interleave order = 1 [0000 0001 0010 0001] ⇒ the unit operates out−of−phase to the clock applied on its SYNC (or operates on its own internal clock if no clock on SYNC).

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The default is set to standalone.

| PMBUS Data | Mode |
|---|---|
| 16'b0000_0000_0000_0000 | Standalone |
| 16'b0000_0001_0000_0000 | Master Sync |
| 16'b0000_0001_0010_0000 | Sync Slave − In Phase |
| 16'b0000_0001_0010_0001 | Sync Slave − Out of Phase |

### VOUT_OV_FAULT_RESPONSE (41h)

VOUT_OV_FAULT_RESPONSE command Instructs the device on what action to take in response to an output over voltage fault set based on the manufacture specific command PCT_VOUT_LIMIT(C6h), Bits<11:9>.

The device also sets

- Sets the VOUT_OV bit in the STATUS_BYTE
- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT OV Fault bit in the STATUS_VOUT
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with Clear Faults section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to 40(hex) ⇒ latch off behavior The data byte is encoded in the format shown below

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | | 00 | Chip continues operation without interruption |
| | | 01 | Chip continues operation for the delay time specified by bits[2:0]. If the fault condition is still present at the end of the delay time, the chip responds as programmed in the Retry setting (bits[5:3]) |
| | | 10 | Not Supported − The chip shuts down (disables the output) and responds according to the retry setting bits[5:3] |
| | | 11 | Not Supported − The chip's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 5:3 | Retry Setting (Latchoff or Hiccup) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001−110 | Not Supported |
| | | 111 | The chip attempts to restart continuously without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), VIN/VCC is removed or another fault condition causes the unit to shut−down. Hiccup time is 1 s |
| 2:0 | Delay Time | XXX | X00− 6.25 μs<br>X01 − 7.5 μs<br>X10 − 8.75 μs<br>X11 − 10 μs |

For 0 V warning the FETs are turned off immediately. An option is provided to turn off the high side FET and turn on the low side FET. MFR_MODE _SETTINGS(C8) Bit<2> is used for this purpose. An attempt to write "Not supported" data given in the table above will flag an invalid data fault.



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### VOUT_UV_WARN_LIMIT (43h)

The VOUT_UV_WARN_LIMIT command specifies the VOUT UV warn limit threshold. The command follows the ULINEAR16 format. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The range, resolution and default value is given in the table below.

| Range | Resolution | Default |
|---|---|---|
| 0.5−5.5 V | 1.9535 mV | 0.2 V (0067 (hex)) |

When VOUT crosses the VOUT UV threshold the STATUS _VOUT(7A) Bit#6 is flagged.

### VOUT_UV_FAULT_RESPONSE (45h)

VOUT_UV_FAULT_RESPONSE command Instructs the device on what action to take in response to an output under voltage fault set based on the manufacture specific command PCT_VOUT_LIMIT(C6h) Bits<5:3>.

The device also

- Sets the VOUT bit in the STATUS_WORD
- Sets the VOUT UV Fault bit in the STATUS_VOUT
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with Clear Faults section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to 40(hex) ⇒ latch off behavior The data byte is encoded in the format shown below

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | | 00 | Chip continues operation without interruption |
| | | 01 | Chip continues operation for the delay time specified by bits[2:0]. If the fault condition is still present at the end of the delay time, the chip responds as programmed in the Retry setting (bits[5:3]) |
| | | 10 | Not Supported – The chip shuts down (disables the output) and responds according to the retry setting bits[5:3] |
| | | 11 | Not Supported – The chip's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. |
| 5:3 | Retry Setting (Latchoff or Hiccup) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001−110 | Not Supported |
| | | 111 | The chip attempts to restart continuously without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), VIN/VCC is removed or another fault condition causes the unit to shutdown. Hiccup time is 1 s |
| 2:0 | Delay Time | XXX | X00 – 6.25 μs<br>X01 – 7.5 μs<br>X10 – 8.75 μs<br>X11 – 10 μs |

An attempt to write "Not supported" data given in the table above will flag an invalid data fault.

### IOUT_OC_FAULT_LIMIT (46h)

This command sets the value of the peak output current in amperes for the high side FET and causes an over current peak detection fault. The IOUT_OC_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits un−signed exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 2−62A | 2 | 54 A (081B(hex)) |



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The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 1 is written, an invalid data fault is flagged. All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault.

| PMBUS Data(hex) | OC Peak Fault Limit(A) |
|---|---|
| 0801 | 2 |
| 0802 | 4 |
| 0803 | 6 |
| 0804 | 8 |
| 0805 | 10 |
| 0806 | 12 |
| 0807 | 14 |
| 0808 | 16 |
| 0809 | 18 |
| 080A | 20 |
| 080B | 22 |
| 080C | 24 |
| 080D | 26 |
| 080E | 28 |
| 080F | 30 |
| 0810 | 32 |
| 0811 | 34 |
| 0812 | 36 |
| 0813 | 38 |
| 0814 | 40 |
| 0815 | 42 |
| 0816 | 44 |
| 0817 | 46 |
| 0818 | 48 |
| 0819 | 50 |
| 081A | 52 |
| 081B | 54 |
| 081C | 56 |
| 081D | 58 |
| 081E | 60 |
| 081F | 62 |


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### IOUT_OC_FAULT_RESPONSE (47h)

This command instructs the device on what action to take in response to an output over current peak fault The device also

- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT bit in the STATUS_BYTE
- Sets the OCP Peak Fault Bit #7 in the STATUS_IOUT
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with "Clear Faults" section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to 80(hex) ⇒ latch off behavior.

The data byte is encoded in the format shown below.

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | | 00 | Chip continues operation without interruption while maintaining the output current at the values set by IOUT_OC_FAULT_LIMIT without regard to the output voltage |
| | | 01 | Chip continues operating indefinitely except if VOUT_UV is detected |
| | | 10 | The chip continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage. For the delay time set by bits[2:0]. If the chip is still operating in current limiting at the end of the delay time , the chip responds as programmed by the Retry Setting in bits[5:3] |
| | | 11 | The chip shuts down and responds as programmed by the Retry setting in bits[5:3] |
| 5:3 | Retry Setting (Latchoff or Hiccup) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001−110 | Not Supported |
| | | 111 | The chip attempts to restart continuously without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), VIN/VCC is removed or another fault condition causes the unit to shutdown. Hiccup time is 1 s |
| 2:0 | Delay Time | XXX | 000 – 160−320 μs<br>001 – 320−480 μs<br>010 – 640−800 μs<br>011 – 1.28−1.44 ms<br>100 – 2.56−2.72 ms<br>101 – 5.12−5.28 ms<br>110 – 9.6−9.76 ms<br>111 – 10.08−10.24 ms |

NOTE: An attempt to write "Not supported" data given in the table above will flag an invalid data fault.

### IOUT_OC_WARN_LIMIT (4Ah)

This command sets the value of the output current in amperes that causes a over current detection warn flag.

The IOUT_OC_WARN_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits signed exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 1−64 A | 62.5 mA | 32 A (E200(hex)) |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

Few examples are given in the Table below. The exponent is read only and if an exponent other than −4(11100b) is written, an invalid data fault is flagged. There is no range check on this command.

| Examples | |
|---|---|
| IOUT OC WARN Limit | PMBUS Data |
| 10 A | E0A0(hex) |
| 15 A | E0F0(hex) |
| 20 A | E140(hex) |
| 25 A | E190(hex) |
| 30 A | E1E0(hex) |
| 35 A | E230(hex) |



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### IOUT_UC_FAULT_LIMIT (4Bh)

This command sets the value of the output negative current limit in amperes that causes a under current detection fault flag. The IOUT_UC_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits un−signed exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 10−24 A | 2 A | 14A(000Ehex) |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault.

| IOUT UC FAULT Limit | PMBUS Data |
|---|---|
| 10 A | 000A(hex) |
| 12 A | 000C(hex) |
| 14 A | 000E(hex) |
| 16 A | 0010(hex) |
| 18 A | 0012(hex) |
| 20 A | 0014(hex) |
| 22 A | 0016(hex) |
| 24 A | 0018(hex) |

When this fault happens the device sets

- Sets the None of the above bit in the STATUS_BYTE
- Sets the IOUT bit in the STATUS_WORD
- Sets the IOUT UC Fault bit in the STATUS_IOUT
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with Clear Faults section and not when the fault condition is removed.

### OT_FAULT_LIMIT (4Fh)

This command sets the temperature in degrees Celsius at which chip should indicate an over temperature fault. The OT_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 80−160°C | 1°C | 140°C |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. The mantissa range is 80°C to 160°C. Any mantissa outside this range will assert invalid data fault. Also if the OT fault limit is set lower or equal to OT warn limit then an invalid data fault is flagged. Few examples are given in the Table below.

| OT Fault Limit | PMBUS Data |
|---|---|
| 80°C | 0050(hex) |
| 90°C | 005A(hex) |
| 100°C | 0064(hex) |
| 105°C | 0069(hex) |
| 120°C | 0078(hex) |
| 160°C | 00A0(hex) |


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### OT_FAULT_RESPONSE (50h)

OT_FAULT_RESPONSE command Instructs the device on what action to take in response to an over temperature fault set by OT_FAULT_LIMIT command. The device also:

- Sets the Temp bit in the STATUS_BYTE
- Sets the Over Temp Fault bit in the STATUS_TEMP
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with Clear Faults section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to C0(hex) ⇒ recovery The data byte is encoded in the format shown below

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | Ignore/latchoff or recovery | 00 | Chip continues operation without interruption |
| | | 01 | Not Supported – Chip continues operation for the delay time specified by bits[2:0]. If the fault condition is still present at the end of the delay time, the chip responds as programmed in the Retry setting (bits[5:3]) |
| | | 10 | The chip shuts down (disables the output) and responds according to the retry setting bits[5:3] |
| | | 11 | The chip's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists |
| 5:3 | Retry Setting (Latchoff ) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001–110 | Not Supported |
| | | 111 | Not Supported The chip attempts to restart continuously without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), VIN/VCC is removed or another fault condition causes the unit to shut–down. Hiccup time is 1 s |
| 2:0 | Delay Time | XXX | Not Supported |

An attempt to write "Not supported" data given in the table above will flag an invalid data fault.

### OT_WARN_LIMIT (51h)

This command sets the temperature in degrees Celsius at which chip should indicate an over temperature warn flag.

The OT_WARN_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 70–150°C | 1°C | 115°C |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. The mantissa range is 70°C to 150°C. Any mantissa outside this range will assert invalid data fault. Also if the OT warn limit is set higher or equal to OT fault limit then an invalid data fault is flagged. Few examples are given in the Table below.

| OT Warn Limit | PMBUS Data |
|---|---|
| 80°C | 0050(hex) |
| 90°C | 005A(hex) |
| 100°C | 0064(hex) |
| 105°C | 0069(hex) |
| 120°C | 0078(hex) |
| 160VC | 00A0(hex) |

When over temperature warn flag is asserted, the device:

- Sets the Temp bit in the STATUS_BYTE
- Sets the Over Temp Warn bit in the STATUS_TEMP

The warn bit once set is cleared only in accordance with Clear Faults section and not when the warn condition is removed.



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### VIN_OV_FAULT_LIMIT (55h)

This command sets the value of the input voltage $V_{IN}$ in volts that causes an input over voltage fault.

The VIN_OV_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 18–24 V | 2 V | 20 V |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 1(00001b) is written, an invalid data fault is flagged. All the options supported are given in the Table below. Any data other than the data given in the table below will flag an invalid data fault.

| $V_{IN}$ Fault Limit | PMBUS Data |
|---|---|
| 18 V | 0809(hex) |
| 20 V | 080A(hex) |
| 22 V | 080B(hex) |
| 24 V | 080C(hex) |

### VIN_OV_FAULT_RESPONSE (56h)

VOUT_OV_FAULT_RESPONSE command Instructs the device on what action to take in response to an input over voltage fault set based on the VIN_OV_FAULT_LIMIT(55h) . The device also sets

- Sets the None of the above bit in the STATUS_BYTE
- Sets the VIN OVP bit in the STATUS_WORD
- Sets the VIN OV Fault bit in the STATUS_INPUT
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with Clear Faults section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to C0(hex) ⇒ Recovery behavior The data byte is encoded in the format shown below.

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | | 00 | Chip continues operation without interruption |
| | | 01 | Chip continues operation for the delay time specified by bits[2:0].<br>If the fault condition is still present at the end of the delay time, the chip responds as programmed in the Retry setting (bits[5:3]) |
| | | 10 | Not Supported – The chip shuts down (disables the output) and responds according to the retry setting bits[5:3] |
| | | 11 | The chip's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. |
| 5:3 | Retry Setting (Latchoff or Hiccup) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001–110 | Not Supported |
| | | 111 | Not Supported |
| 2:0 | Delay Time | XXX | X00 – 6.25 μs<br>X01 – 7.5 μs<br>X10 – 8.75 μs<br>X11 – 10 μs |

For 0 V warning the FETs are turned off immediately. An option is provided to turn off the high side FET and turn on the low side FET. MFR_MODE _SETTINGS(C8) Bit<2> is used for this purpose. An attempt to write "Not supported" data given in the table will flag an invalid data fault.



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### TON_DELAY (60h)

This command sets the time, in milliseconds, from when a start condition is received (as programmed by the ON_OFF_CONFIG command) until the output voltage starts to rise. The TON_DELAY command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 1−10 ms | 1 ms | 1 ms |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. Any mantissa Bit<10:4> if not 00(hex) will assert invalid data fault. Few examples are given in the Table below.

| TON Delay | PMBUS Data |
|---|---|
| 1 ms | 0001(hex) |
| 2 ms | 0002(hex) |
| 3 ms | 0003(hex) |
| 5 ms | 0005(hex) |
| 9 ms | 0009(hex) |
| 10 ms | 000A(hex) |

### TON_RISE (61h)

This command sets the time, in milliseconds, from when the output starts to rise until the voltage has entered the regulation band. The TON_RISE command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 1−20 ms | 1 ms | 5 ms |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. Any mantissa Bit<10:5> if not 00(hex) will assert invalid data fault. 0ms setting will also set an invalid data fault. Few examples are given in the Table below.

| TON Rise | PMBUS Data |
|---|---|
| 1 ms | 0001(hex) |
| 2 ms | 0002(hex) |
| 3 ms | 0003(hex) |
| 5 ms | 0005(hex) |
| 9 ms | 0009(hex) |
| 10 ms | 000A(hex) |

### TON_MAX_FAULT_LIMIT (62h)

This command sets an upper limit, in milliseconds, on how long the unit can attempt to power up the output without reaching the output under voltage fault limit. The TON_MAX_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 0−50 ms | 2 ms | 12 ms |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 1(00001b) is written, an invalid data fault is flagged. Any mantissa Bit<10:5> if not 00(hex) will assert invalid data fault. 0ms setting will also set an invalid data fault. Few examples are given in the Table below.

| TON Max Fault Limit | PMBUS Data |
|---|---|
| 2 ms | 0801(hex) |
| 4 ms | 0802(hex) |
| 10 ms | 0805(hex) |
| 20 ms | 080A(hex) |
| 30 ms | 080F(hex) |
| 40 ms | 0814(hex) |

### TON_MAX_FAULT_RESPONSE (63h)

TON_MAX_FAULT_RESPONSE command Instructs the device on what action to take in response to an Ton−max fault set by TON_MAX_FAULT_LIMIT command; The device also:

- Sets the VOUT bit in the STATUS_BYTE
- Sets the TON MAX fault bit in the STATUS_VOUT
- Notifies the host by asserting the ALERTB



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The fault bit once set is cleared only in accordance with Clear Faults section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to 80(hex) ⇒ Latchoff The data byte is encoded in the format shown below

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | Ignore/latchoff or recovery | 00 | Chip continues operation without interruption |
| | | 01 | Not Supported – Chip continues operation for the delay time specified by bits[2:0]. If the fault condition is still present at the end of the delay time, the chip responds as programmed in the Retry setting (bits[5:3]) |
| | | 10 | The chip shuts down (disables the output) and responds according to the retry setting bits[5:3] |
| | | 11 | Not Supported –The chip's output is disabled while the fault is present. Operation resumes and the output is enabled when the fault condition no longer exists. |
| 5:3 | Retry Setting (Latchoff ) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001–110 | Not Supported |
| | | 111 | The chip attempts to restart continuously without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), VIN/VCC is removed or another fault condition causes the unit to shutdown. Hiccup time is 1 s |
| 2:0 | Delay Time | XXX | Not Supported |

NOTE: An attempt to write "Not supported" data given in the table above will flag an invalid data fault.

### TOFF_DELAY (64h)

This command sets the time, in milliseconds, from when a stop condition is received (as programmed by the ON_OFF_CONFIG command) until the unit stops transferring energy to the output. The TOFF_DELAY command has two data bytes encoded in LINEAR11 format (5bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 0–10 ms | 1 ms | 0 ms |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. Any mantissa Bit<10:4> if not 00(hex) will assert invalid data fault. Few examples are given in the Table below.

| TOFF Delay | PMBUS Data |
|---|---|
| 1 ms | 0001(hex) |
| 2 ms | 0002(hex) |
| 3 ms | 0003(hex) |
| 5 ms | 0005(hex) |
| 9 ms | 0009(hex) |
| 10 ms | 000A(hex) |

### TOFF_FALL (65h)

This command sets the time, in milliseconds, from the end of the turn–off delay time until the voltage is commanded to zero. The TOFF_FALL command has two data bytes encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 1–20 ms | 1 ms | 5 ms |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The exponent is read only and if an exponent other than 0(00000b) is written, an invalid data fault is flagged. Any mantissa Bit<10:5> if not 00(hex) will assert invalid data fault. 0ms setting will also set an invalid data fault. Few examples are given in the Table below.

| TOFF Fall | PMBUS Data |
|---|---|
| 1 ms | 0001(hex) |
| 2 ms | 0002(hex) |
| 3 ms | 0003(hex) |
| 5 ms | 0005(hex) |
| 9 ms | 0009(hex) |
| 10 ms | 000A(hex) |


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### STATUS_BYTE (78h)

This command returns one byte of information with the summary of the critical faults. The below table shows all the bits.

| Bit | Function | Support |
|---|---|---|
| 7 | Busy – nonvolatile memory is being accessed either for read or write operation | Yes |
| 6 | OFF | Yes |
| 5 | VOUT_OVP Fault | Yes |
| 4 | IOUT_OC(Peak Fault) | Yes |
| 3 | VIN_UV | No |
| 2 | Temperature Fault or Warn | Yes |
| 1 | CML(PEC Failed, Invalid data or Invalid command) | Yes |
| 0 | None of the above (vin_ovp, vin_off, ocp average fault, hsd_ilim2, lsd_ilim, pgood_fault, vout_uvlo_fault, vout_ uvwarn, ocp_warn, ocp_peak & uvlo fault, over temp umbrella, sw_fault, boot_uvlo, all STATUS_MFR faults | Yes |

### STATUS_WORD (79h)

This command returns two bytes of information with the summary of the critical faults. The lower byte of STATUS_WORD is the same register as STATUS_BYTE command. The below table shows all the bits in the upper byte.

| Upper Byte Bit # | Function | Supporting |
|---|---|---|
| 7 | VOUT(all STATUS_VOUT) | Yes |
| 6 | IOUT/POUT(Peak OCP Fault or Average OCP Fault or Warn or Neg ILIM Fault) | Yes |
| 5 | INPUT(VIN OVP Fault & VIN_OFF Fault) | Yes |
| 4 | MFR(all STATUS_MFR) | Yes |
| 3 | POWERGOOD# | Yes |
| 2 | FANS | No |
| 1 | Other | No |
| 0 | Unknown | No |

If output voltage is valid then POWERGOOD# bit is cleared. If output voltage is not present POWERGOOD# is set.

### STATUS_VOUT (7Ah)

This command returns one byte of information with the summary of the $V_{OUT}$ faults. The below table shows all the bits. The table also shows SMBALERT_MASK command support.

| Status VOUT Reporting | Support | Support Alert Mask |
|---|---|---|
| Bit<7> output over voltage fault | Yes | Yes |
| Bit<6> output over voltage warning | Yes | No |
| Bit<5> output under voltage warning | Yes | No |
| Bit<4> output under voltage fault | Yes | Yes |
| Bit<3>output max or min warning | No | No |
| Bit<2> ton max fault | Yes | Yes |
| Bit<1> ton max warning | No | No |
| Bit<0> output voltage tracking error | No | No |



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### STATUS_IOUT (7Bh)

This command returns one byte of information with the summary of the $I_{OUT}$ faults. The below table shows all the bits. The table also shows SMBALERT_MASK command support.

| Status IOUT Reporting | Support | Support Alert Mask |
|---|---|---|
| Bit<7> output over current peak fault | Yes | Yes |
| Bit<6> output over current and low voltage fault | Yes | Yes |
| Bit<5> output over current average warning | Yes | No |
| Bit<4> output under current fault | Yes | Yes |
| Bit<3> current share fault | No | No |
| Bit<2> in power limiting mode | No | No |
| Bit<1> output overpower fault | No | No |
| Bit<0> output overpower warning | No | No |

### STATUS_INPUT (7Ch)

This command returns one byte of information with the summary of the VIN faults. The below table shows all the bits. The table also shows SMBALERT_MASK command support.

| Status INPUT Reporting | Support | Support Alert Mask |
|---|---|---|
| Bit<7> input over voltage fault | Yes | Yes |
| Bit<6> input over voltage warning | No | No |
| Bit<5> input under voltage warning | No | No |
| Bit<4> input under voltage fault | No | No |
| Bit<3> unit off for insufficient input voltage | Yes | Yes |
| Bit<2> input over current fault | No | No |
| Bit<1> input over current warning | No | No |
| Bit<0> input overpower warning | No | No |

### STATUS_TEMPERATURE (7Dh)

This command returns one byte of information with the summary of the temperature faults. The below table shows all the bits. The table also shows SMBALERT_MASK command support.

| Status Temperature Reporting | Support | Support Alert Mask |
|---|---|---|
| Bit<7> over temperature fault | Yes | Yes |
| Bit<6> over temperature warning | Yes | No |
| Bit<5> under temperature warning, reports 0 | No | No |
| Bit<4> under temperature fault | No | No |
| Bit<3> Reserved, reports 0 | No | No |
| Bit<2> Reserved, reports 0 | No | No |
| Bit<1> Reserved, reports 0 | No | No |
| Bit<0> Reserved, reports 0 | No | No |



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### STATUS_CML(7Eh)

This command returns one byte of information with the summary of the below faults. The table also shows SMBALERT_MASK command support.

| Status CML Reporting | Support | Support Alert Mask |
|---|---|---|
| Bit<7> command not supported | Yes | Yes |
| Bit<6> invalid data | Yes | Yes |
| Bit<5> PEC fault | Yes | Yes |
| Bit<4> OTP fault – Not supported, reports 0 | No | No |
| Bit<3:2> Reserved, reports 0 | No | No |
| Bit<1> other communication fault, reports 0 | No | No |
| Bit<0>other memory or logic fault, reports 0 | No | No |

### STATUS_MFR_SPECIFIC (80h)

This command returns one byte of information with the summary of the below faults. The table also shows SMBALERT_MASK command support.

| Status MFR Reporting | Support | Support Alert Mask |
|---|---|---|
| Bit<7> ocp average fault flag | Yes | Yes |
| Bit<6> hsd_ilim2 | Yes | Yes |
| Bit<5>sw_fault | Yes | Yes |
| Bit<4>boot_uvlo | Yes | Yes |
| Bit<3> over temp analog | Yes | Yes |
| Bit<2> Lg Pin Fault | Yes | Yes |
| Bit<1> MTP Programming Fault | Yes | Yes |
| Bit<0> Not used, reports 0 | No | No |

### READ_VIN (88h)

The READ_VIN command returns the input voltage in Volts. The two data bytes are encoded in LINEAR11 format (5 bits signed exponent and 11 bits mantissa). Exponent is FIXED −5 (11011b) indicating a LSB of 31.25 mV.

The range and resolution are shown in the below table.

| Range | Resolution |
|---|---|
| 0–25 V | 31.25 mV |

Few examples are given in the Table below.

| Read VIN | PMBUS Data |
|---|---|
| 6 V | D8C0(hex) |
| 10 V | D940(hex) |
| 12 V | D980(hex) |
| 18 V | DA40(hex) |

### READ_IIN (89h)

The READ_IIN command returns the input current in Amps. The two data bytes are encoded in LINEAR11 format (5 bits signed exponent and 11 bits mantissa). Exponent is FIXED −4 (11100b) indicating a LSB of 62.5 mA. The range and resolution are shown in the below table. READ_IIN acknowledges only if the device is regulating.

| Range | Resolution |
|---|---|
| 0–64 A | 62.5 mA |

Few examples are given in the Table below.

| Read IIN(Amps) | PMBUS Data |
|---|---|
| 6 | E060(hex) |
| 10 | E0A0(hex) |
| 12 | E0C0(hex) |
| 18 | E120(hex) |



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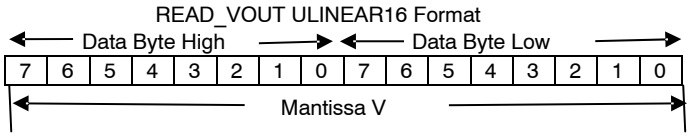
**READ_VOUT(8Bh)**

The READ_VOUT command returns the actual, measured (not commanded) output voltage in the same format as set by the VOUT_MODE command. The two data bytes are encoded in LINEAR16 format as shown in below.




The exponent is defined by VOUT_MODE command. Exponent is FIXED −9 (10111b) indicating a LSB of 1.953 mV.

The range and resolution are shown in the below table. READ_VOUT will only acknowledge if the device is regulating.

| Range | Resolution |
|---|---|
| 0.5 V–5.5 V | 1.953 mV (set by VOUT_MODE command) |

Few examples are given in the Table below.

| Read VOUT(V) | PMBUS Data |
|---|---|
| 0.8 V | 019A(hex) |
| 1.0 V | 0200(hex) |
| 1.5 V | 0300(hex) |
| 2.0 V | 0400(hex) |
| 3.3 V | 069A(hex) |
| 5.0 V | 0A00(hex) |
| 5.5 V | 0B00(hex) |

**READ_IOUT(8Ch)**

The READ_IOUT command returns the measured output current in Amps. The two data bytes are encoded in LINEAR11 format (5 bits signed exponent and 11 bits mantissa). Exponent is FIXED −4 (11100b) indicating a LSB of 62.5 mA. The range and resolution are shown in the below table. “READ_IOUT” will not acknowledge if the device is not regulating.

| Range | Resolution |
|---|---|
| 0–64 A | 62.5 mA |

Few examples are given in the Table below.

| Read IOUT(Amps) | PMBUS Data |
|---|---|
| 6 | E060(hex) |
| 10 | E0A0(hex) |
| 12 | E0C0(hex) |
| 18 | E120(hex) |

**READ_TEMPERATURE(8Dh)**

The READ_TEMPERATURE command returns the measured temperature in degree Celsius. The two data bytes are encoded in LINEAR11 format (5 bits unsigned exponent and 11 bits signed mantissa). Exponent is FIXED 0 (00000b) indicating a LSB of 1°C.The range and resolution are shown in the below table.

| Range | Resolution |
|---|---|
| −40 to 175°C | 1°C |

Few examples are given in the Table below.

| Read Temp (°C) | PMBUS Data |
|---|---|
| 25 | 0019(hex) |
| 50 | 0032(hex) |
| 100 | 0064(hex) |
| −20 | 07EC(hex) |

**READ_FREQ(95h)**

The READ_ FREQ command returns the switching frequency in KHz. The two data bytes are encoded in LINEAR11 format (5bits unsigned exponent and 11 bits unsigned mantissa). Exponent is FIXED 0 (00000b) indicating a LSB of 1KHz. The range and resolution are shown in the below table. READ_FREQ will only acknowledge if the device is regulating.

| Range | Resolution |
|---|---|
| 100 Khz – 2.5 MHz | 1 KHz |

Few examples are given in the Table below.

| Read Freq (KHz) | PMBUS Data |
|---|---|
| 200 | 00C8(hex) |
| 400 | 0190(hex) |
| 600 | 0258(hex) |
| 800 | 0320(hex) |



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**PMBUS_REVISION(98h)**

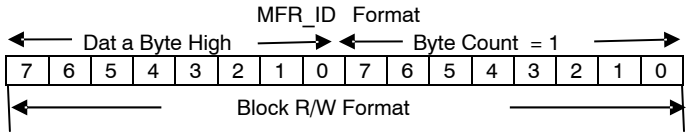
PMBUS_REVISION command stores or reads the revision of the PMBUS to which the device is compliant. This command is read only and has one data byte. Bits [7:4] indicate the revision of PMBUS specification Part I to which the device is compliant. Bits [3:0] indicate the revision of PMBUS specification Part II to which the device is compliant. The permissible values are shown below.

| Bits [7:4] | Part I Revision | Bits[3:0] | Part II Revision |
|---|---|---|---|
| 0000b | 1.0 | 0000b | 1.0 |
| 0001b | 1.1 | 0001b | 1.1 |
| 0010b | 1.2 | 0010b | 1.2 |
| 0011b | 1.3 | 0011b | 1.3 |

FAN2510xx supports Revsion1.3 and therefore reads back 33(hex) for PMBUS_REVISION command.

**MFR_ID(99h)**

MFR_ID command is used to either set or read the manufacture's ID (name, abbreviation or symbol that identifies the unit's manufacturer). This command is read/write accessible and has two data bytes as shown below.




The Block R/W format needs to be used to access this register for read and write operations. The lower byte represents the number of bytes and this is fixed to 1(00000001b). The higher byte is used to represent the MFR_ID.

The higher byte contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

**MFR_MODEL (9Ah)**

MFR_MODEL command is used to either set or read the manufacture's model number. This command is read/ write accessible and has two data bytes. The Block R/W format needs to be used to access this register for read and write operations. The lower byte represents the number of bytes and this is fixed to 1(00000001b). The higher byte is used to represent the MFR_MODEL.

The higher byte contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

**MFR_REVISION (9Bh)**

MFR_REVISION command is used to either set or read the manufacture's revision number. This command is read/write accessible and has two data bytes. The Block R/W format needs to be used to access this register for read and write operations. The lower byte represents the number of bytes and this is fixed to 1(00000001b). The higher byte is used to represent the MFR_REVISION.

The higher byte contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

**MFR_SERIAL (9Eh)**

MFR_SERIAL command is used to either set or read the manufacture's serial number of the device. This command is read/write accessible and has two data bytes. The Block R/W format needs to be used to access this register for read and write operations. The lower byte represents the number of bytes and this is fixed to 1(00000001b). The higher byte is used to represent the MFR_SERIAL. The higher byte contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.



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### MFR_VOUT_MIN (A4h)

MFR_VOUT_MIN command is used to retrieve the minimum rated value, in Volts, to which the output voltage may be set for the device. This command is read accessible and has two data bytes in UNLINEAR16 format. The exponent is defined by VOUT_MODE command. Exponent is FIXED −9 (10111b) indicating a LSB of 1.953 mV. The read back of this register is set to 0100(hex) to represent 0.5 V.

### MFR_VOUT_MAX (A5h)

MFR_VOUT_MIN command is used to retrieve the maximum rated value, in Volts, to which the output voltage may be set for the device. This command is read accessible and has two data bytes in UNLINEAR16 format The exponent is defined by VOUT_MODE command. Exponent is FIXED −9 (10111b) indicating a LSB of 1.953 mV. The read back of this register is set to 0B01(hex) to represent 5.5 V.

### IC_DEVICE_ID (ADh)

IC_DEVICE_ID command is used to read the type or part number of the IC embedded within a PMBUS that is used for the PMBUS interface. This command is read accessible and has two data bytes. The Block Read format needs to be used to access this register for read operation. The lower byte represents the number of bytes and this is fixed to 1(00000001b). The higher byte is used to represent the IC_DEVICE_ID.

### IC_DEVICE_REV (AEh)

IC_DEVICE_REV command is used to read the revision of the IC whose type or part number is read with the IC_DEVICE_ID command. This command is read accessible and has two data bytes. The Block Read format needs to be used to access this register for read operation. The lower byte represents the number of bytes and this is fixed to 1(00000001b). The higher byte is used to represent the IC_DEVICE_REV.

### IOUT_AVG_FAULT_RESPONSE (C4h)

This manufacture specific command instructs the device on what action to take in response to an output over current average fault. The device also:

- Sets the IOUT bit in the STATUS_WORD
- Sets the None of the above bit in the STATUS_BYTE
- Sets the OCP Average Fault Bit #7 in the STATUS_MFR_SPECIFIC
- Notifies the host by asserting the ALERTB

The fault bit once set is cleared only in accordance with “ClearFaults” section and not when the fault condition is removed. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The default of this register is set to 80(hex) ⇒ latch off behavior The data byte is encoded in the format shown below

| Bits | Description | Value | Meaning |
|---|---|---|---|
| 7:6 | | 00 | Chip continues operation without interruption while maintaining the output current at the values set by IOUT_OC_FAULT_LIMIT without regard to the output voltage |
| | | 01 | Chip continues operating indefinitely except if VOUT_UV is detected |
| | | 10 | The chip continues to operate, maintaining the output current at the value set by IOUT_OC_FAULT_LIMIT without regard to the output voltage. For the delay time set by bits[2:0]. If the chip is still operating in current limiting at the end of the delay time , the chip responds as programmed by the Retry Setting in bits[5:3] |
| | | 11 | The chip shuts down and responds as programmed by the Retry setting in bits[5:3] |
| 5:3 | Retry Setting(Latchoff or Hiccup) | 000 | A zero value for the retry setting means that the chip does not attempt to restart. The output remains disabled until the faulty is cleared |
| | | 001−110 | Not Supported |
| | | 111 | The chip attempts to restart continuously without limitation, until it is commanded OFF (by the ENABLE pin or OPERATION command or both), VIN/VCC is removed or another fault condition causes the unit to shutdown. Hiccup time is 1 second |
| 2:0 | Delay Time | XXX | 000 – 160−320 μs<br>001 – 320−480 μs<br>010 – 640−800 μs<br>011 – 1.28−1.44 ms<br>100 – 2.56−2.72 ms<br>101 – 5.12−5.28 ms<br>110 – 9.6−9.76 ms<br>111 – 10.08−10.24 ms |

NOTE: An attempt to write “Not supported” data given in the table above will flag an invalid data fault.



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### IOUT_AVG_FAULT_LIMIT (C5h)

This manufacturer specific command sets the value of the output current in amperes that causes an average over current detection fault flag. The IOUT_AVG_FAULT_LIMIT command has two data bytes encoded in LINEAR11 format (5 bits signed exponent and 11 bits mantissa). The range, resolution and default are shown in the below table.

| Range | Resolution | Default |
|---|---|---|
| 1−64 A | 62.5 mA | 45 A(E2D0(hex)) |

The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. Few examples are given in the Table below. The exponent is read only and if an exponent other than −4(11100b) is written, an invalid data fault is flagged. The 0A setting is not allowed and there is no maximum value range check on this command.

| Examples | |
|---|---|
| **IOUT_AVG_FAULT Limit** | **PMBUS Data** |
| 10 A | E0A0(hex) |
| 15 A | E0F0(hex) |
| 20 A | E140(hex) |
| 30 A | E1E0(hex) |
| 40 A | E280(hex) |
| 45 A | E2D0(hex) |

### PCT_VOUT_LIMIT (C6h)

This manufacturer specific command sets the value of the output voltage in terms of %, the level that causes an output under voltage, over voltage 1, over voltage 2 fault.

The PCT_VOUT_LIMIT command has two data bytes encoded in LINEAR16 format. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The below table shows all the options allowed

| Bit<11:9> | OVP2 Thresh(Fault) | Bit<8:6> | OVP1 Thresh (Warn) | Bit<5:3> | UVLO Thresh |
|---|---|---|---|---|---|
| 000 | 110% | 000 | N/A | 000 | 55% |
| 001 | 112% | 001 | N/A | 001 | 60% |
| 010 | 114% | 010 | 106% | 010 | 65% |
| 011 | 116% | 011 | 108% | 011 | 70% |
| 100 | 118% | 100 | 110% | 100 | 75% |
| 101 | 120% | 101 | 112% | 101 | 80% |
| 110 | 122% | 110 | 114% | 110 | 85% |
| 111 | 124% | 111 | 116% | 111 | 90% |

Default is set to OVP Warn: 108%, OVPFault−116%, UVLO Fault−75% (Default = 06E0(hex)).

OVP Warn threshold needs to be less than OVP Fault threshold. UVLO Fault threshold needs to be less than OVP Fault and Warn threshold.



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### PCT_PGOOD_LIMIT (C7h)

This manufacture specific command sets the value of the good on and off levels in %. The PCT_PGOOD_LIMIT command has one byte. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The below table shows all the options allowed

| Bit<5:3> | PGOOD ON | Bit<2:0> | PGOOD OFF |
|---|---|---|---|
| 000 | 84% | 000 | 82% |
| 001 | 86% | 001 | 84% |
| 010 | 88% | 010 | 86% |
| 011 | 90% | 011 | 88% |
| 100 | 92% | 100 | 90% |
| 101 | 94% | 101 | 92% |
| 110 | 96% | 110 | 94% |
| 111 | 98% | 111 | 96% |

The default PGOOD ON level is set to 90% and default PGOOD OFF level is set to 84% (19(hex)). If PGOOD_ON level is set to a value which is less than PGOOD_OFF level an invalid data fault is flagged.

### MFR_MODE_SETTINGS (C8h)

This manufacture specific command sets

- CCM behavior,
- Enable/Disable VSET pin,
- Turn on/off LS FET at OV_WARN and
- Gain calibration for input current reporting (READ_IIN)

This is a one byte command. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command. The below table shows all the options allowed

| Bit # | Function | Default |
|---|---|---|
| 0 | “1” Disable Select VSET pin | Select VSET(0) |
| 1 | | CCM(0) |
| 2 | “1” Enable LS on for OVP1 | LS off (0) |
| 3 | Unused | 0 |
| 4 | Input IMON<3:0> | 1010 |
| 5 | | |
| 6 | | |
| 7 | | |

VSET pin resistor (with up to 1% tolerance) is used to set the initial Vout setting of the device. The table shows the mapping from various resistors to the selected Vout and gain setting. A MFR_MODE_SETTINGS bit<0> is used to select this initial $V_{SET}$ value or not.

| $V_{SET}$ Resistor Value (kΩ) | $V_{OUT}$ Preset Value (V) | Gain |
|---|---|---|
| Short | 0.6 | 1 |
| 0.845 | 0.6 | 1 |
| 1.3 | 0.9 | 1 |
| 1.78 | 0.95 | 1 |
| 2.32 | 1 | 1 |
| 2.87 | 1.05 | 1 |
| 3.48 | 1.2 | 1 |
| 4.12 | 1.25 | 1 |
| 4.75 | 1.5 | 1 |
| 5.49 | 1.8 | 1 |
| 6.19 | 2.1 | 0.5 |
| 6.98 | 2.5 | 0.5 |
| 7.87 | 3.3 | 0.5 |
| 8.87 | 5 | 0.25 |
| 10 & greater value | 0.8 | 1 |



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### MFR_PMBUS_BASE (C9h)

This manufacture specific command sets part of the base part of the PMBUS address. ADDR pin resistor (with up to 1% tolerance) is used to set the PMBUS address of the device.

This is a one byte command. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

The table shows the mapping from ADDR pin resistors to the selected PMBUS address. The base part of the address comes from the MFR_PMBUS_BASE command. Base address is added to the offset from the below table to generate the 7 bit PMBUS address used for all the PMBUS communication.

To change the base address, use the current base address (factory default is 7'10h) to write the new/desired address to this register. All subsequent data transactions use the revised base address.

When an ARA command is received by the FAN2510XY, it responds by sending its slave address. This functionality is supported only when the base address is 7'40h or greater. The FAN2510XY should not be used with a base address less than 40h in systems employing ARA functionality, as it will result in an incorrect device response to the system.

| ADDR Resistor Value (kΩ) | Offset Address (h) | PMBUS Address (h) |
|---|---|---|
| 0 (short) | – | 0F |
| 0.845 | 00 | Base+00 |
| 1.3 | 01 | Base+01 |
| 1.78 | 02 | Base+02 |
| 2.32 | 03 | Base+03 |
| 2.87 | 04 | Base+04 |
| 3.48 | 05 | Base+05 |
| 4.12 | 06 | Base+06 |
| 4.75 | 07 | Base+07 |
| 5.49 | 08 | Base+08 |
| 6.19 | 09 | Base+09 |
| 6.98 | 0A | Base+0A |
| 7.87 | 0B | Base+0B |
| 8.87 | 0C | Base+0C |
| 10 | 0D | Base+0D |
| ≥12.4 | – | 0F |

### MFR_ID2 (CAh)

This manufacture specific command provides an option for customers who need 16 bits of manufacture's ID (name, abbreviation or symbol that identifies the unit's manufacturer). This is a two byte command accessible for read and write. The contents of this register can be stored to nonvolatile memory using the STORE_USER_ALL command.

### PMBUS Device Fault Management Clearing Warning or Fault Bits

All of the warning or fault bits (except PGOOD fault) set in the status registers remain set , even if the fault or warning condition is removed or corrected until one of the following occur:

- Bit is individually cleared
- Device receives a CLEAR_FAULTS command
- The output is commanded through the ENABLE pin, the OPERATION command, or the combined action of ENABLE pin and OPERATION command to turn OFF and then turn back on, or
- Bias power is removed from the PMBUS device. This means that VDD or VIN supply collapses below the level

The two exceptions to the above rule that status bits remain set are the OFF and POWERGOOD# bits. These bits always reflect the current state of the device and the POWER_GOOD signal.

### Clearing Individual Bits

Any or all the bits in any status register except STATUS_BYTE and STATUS_WORD can be directly cleared by issuing the status command with one data byte written. The data byte is a binary value. A 1 in any bit position indicates that bit is to be cleared, if set, and unchanged if not set. Examples of data bytes:

- 00010000b indicates that bit[4] is to be cleared and all other bits are to be unchanged,
- 01100010b indicates that bits[6],[5] and [11] are to be cleared and all other bits are to be unchanged
- 11111111b, or FFh, indicates all bits are to be cleared

### Clearing Bits in the STATUS_BYTE and STATUS_WORD

Most bits in the STATUS_BYTE and STATUS_WORD are cleared by clearing the bit or all of the bits that cause the bit in STATUS_BYTE or STATUS_WORD to be set. In general, STATUS_BYTE and STATUS_WORD are the logical OR of the bits in a lower level status register. Figure 10 shows this concept.


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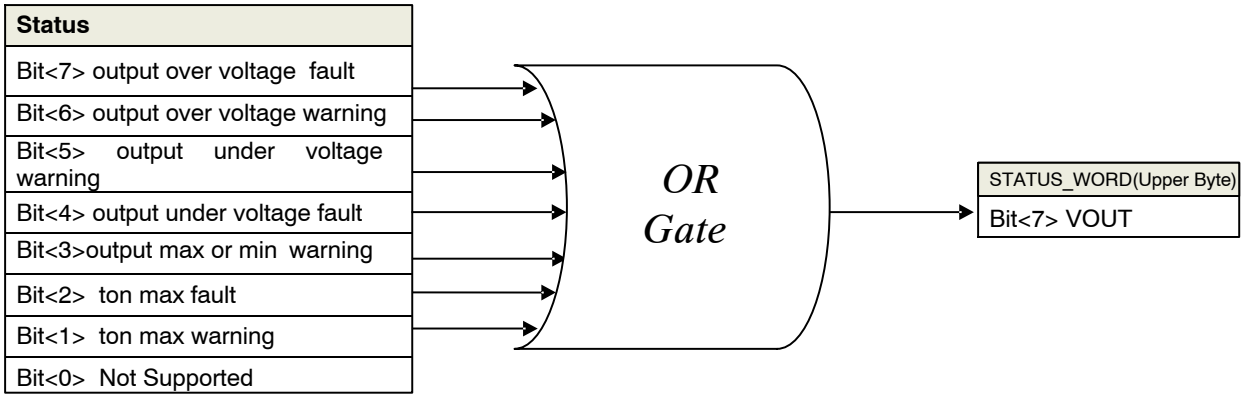


**Figure 13. Conceptual View of Creating Bits in STATUS_BYTE and STATUS_WORD**

For example, if the VOUT_OV_FAULT bit is STATUS_VOUT register is set, then the VOUT bit in the STATUS_WORD is also set. When the VOUT_OCV_FAULT bit in the STATUS_VOUT register is cleared, the VOUT bit in the STATUS_WORD will be cleared at the same time provided no other bits in the STATUS_VOUT are set.

OFF and POWERGOOD# bits cannot be cleared as they always reflect the current state of the device.

### Immediate Reassertion after Clearing if Condition is still present

If the warning or fault condition is present when the bit is cleared, the bit is immediately set again. The ALERTB# will also be asserted again immediately after the status bit is cleared. The SMBALERT_MASK command can be used to prevent this behavior.

### Conceptual View of How Status Bits and ALERTB# Work

When some warning or fault event is detected a latch is set. The output of this latch becomes the status bit in one of the lower level status register (such as STATUS_VOUT). The latch output may also be used, either by itself or OR'ed with other status bits, to create the corresponding bit in STATUS_BYTE or STATUS_WORD and to affect SMBALERT#.

The output of the latch passes through a gate controlled by the corresponding SMBALERT_MASK bit. If this bit is set, the output of the latch is blocked from driving the SMBALERT# circuit. If the SMBALERT_MASK bit is cleared, the latch output is allowed to pass and drive the SMBALERT# circuit. Figure 14 below gives a conceptual illustration of how the SMBALERT# signal is generated.

When the SMBALERT# circuit detects the rising edge of the latch output it asserts the SMBALERT# signal output goes low).

The SMBALERT# signal remains asserted until is cleared. It is cleared when the device successfully transmits its address in response to receiving the Alert Response Address. It is also cleared by a CLEAR_FAULTS command. The latch can also be cleared by writing a 1 to corresponding bit in the status register.

Conceptually the bit clearing commands act as pulses, driving the reset pin on the latch only momentarily. This means that if the vent is ongoing (the event detector is still active) the output latch will immediately set again. As described above, this will cause the SMBALERT# to reassert if it had been previously cleared (and the SMBALERT_MASK bit is not set). This also means that host won't be able to see the status bit get cleared.



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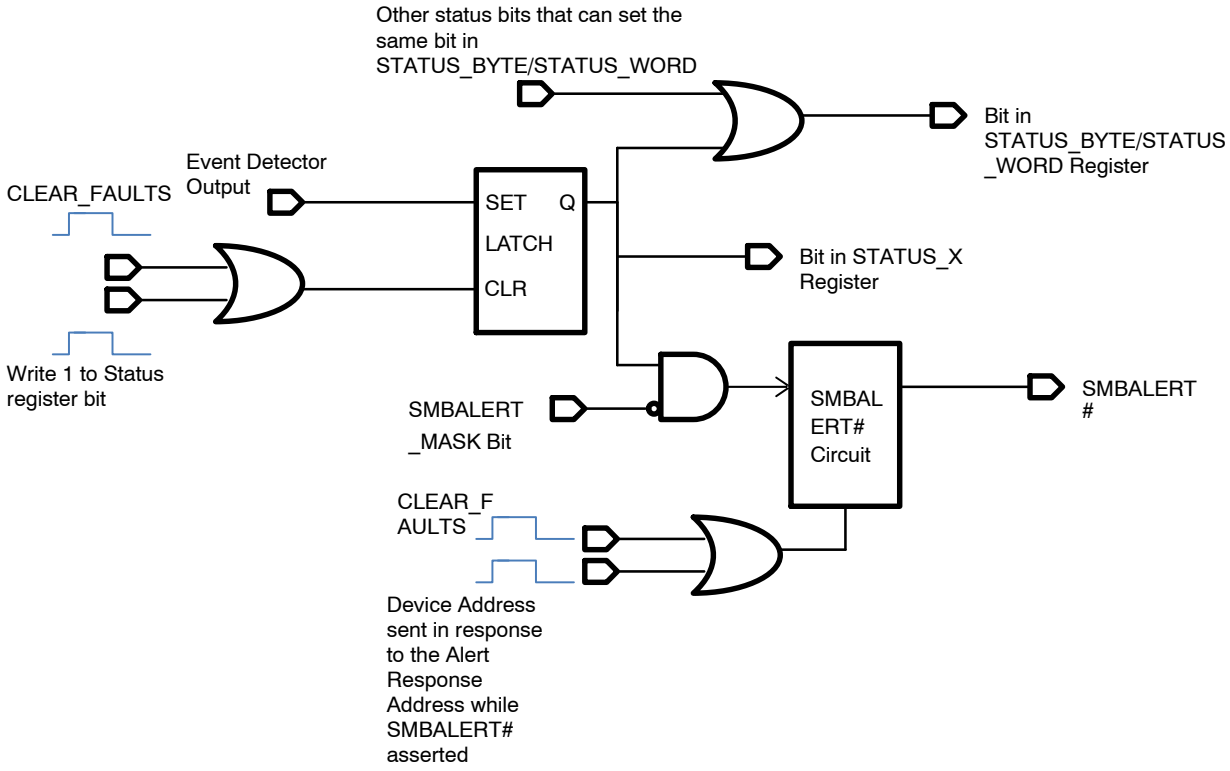


**Figure 14. Conceptual Schematic of Status Bits and SMBALERT#**

### PCB Layout Guideline

All high−current nodes, such as PVIN, SW, VOUT, and PGND, should have the shortest and widest copper possible to reduce parasitic inductance and resistance. This helps reduces switching noise and PCB temperature rise, improving system performance.

Place ceramic input bypass capacitors ($C_{IN}$) next to the IC's PVIN and PGND pins. Route directly to the IC on top layer using the widest and shortest possible traces to reduce series parasitics. Series L increases peak switching voltage levels and may result in the necessity of adding a RC snubber, which typically impacts efficiency. Input bulk capacitors can be placed farther away from the IC.

The SW, PH, and BOOT pins contain high voltage discontinuous switching signals with sharp edges. Care should be taken to avoid capacitive coupling to noise sensitive signals (FB, COMP, VSEN±, VDIFF). Avoid routing sensitive signals next to, or over/under on adjacent layers without GND shields, to the discontinuous switching signals.

Place de−coupling capacitors for PVCC and VCC adjacent to their respective IC pins and connect with widest possible trace on the top layer. The other side of the bypass caps may be connected with vias to the system GND plane, and PGND.

It is recommended to create a location for a series boot resistor ($R_{BOOT}$), in series with $C_{BOOT}$, between the BOOT and PH pins. A low value (<5Ω) $R_{BOOT}$ can be useful in limiting peak SW voltages to safe levels, particularly when elevated PVIN levels are used. $R_{BOOT}$ slows the rising SW edge and may be a useful RC snubber substitute, although either can have a negative impact on efficiency. Use the widest and most direct trace possible to reduce series parasitics. Avoid adding stray, or parasitic, capacitance from BOOT−GND.

The PVIN and PGND pins handle large, high frequency currents. The use of thermal ties on PVIN and PGND connections is not recommended, as this tends to raise parasitic L. Multiple, direct connected vias are recommended, instead.

### ORDERING INFORMATION

| Device | Current | Package | Shipping † |
|---|---|---|---|
| FAN251030MNTXG | 35 A | WQFN34, 5.0 x 7.0 mm (Pb−Free) | 4,000 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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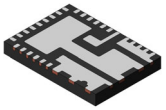
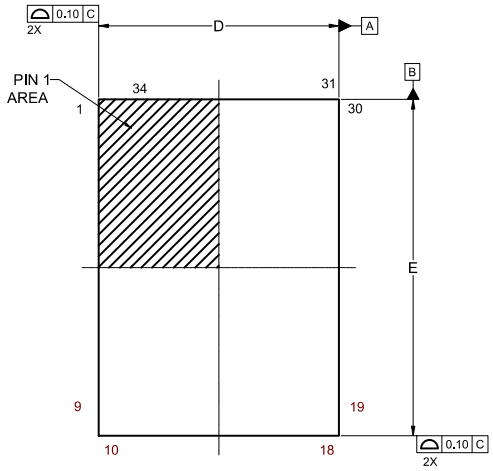
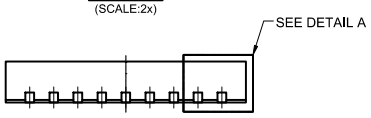


## WQFN−34 5.00x7.00x0.75, 0.50P
CASE 510CL
ISSUE E

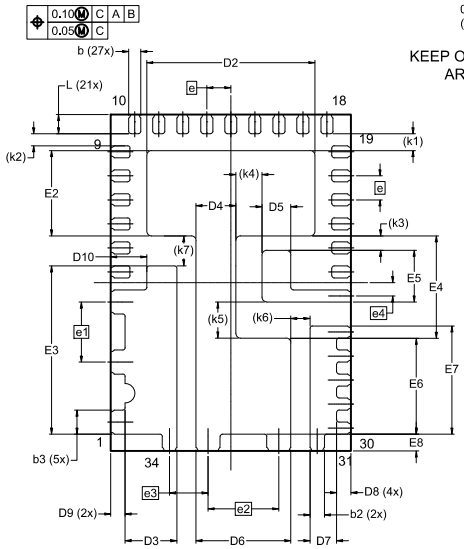
DATE 08 JUN 2026



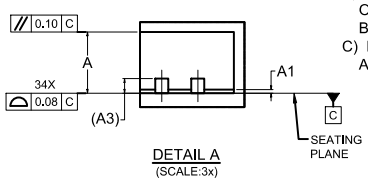

TOP VIEW
(SCALE:2x)



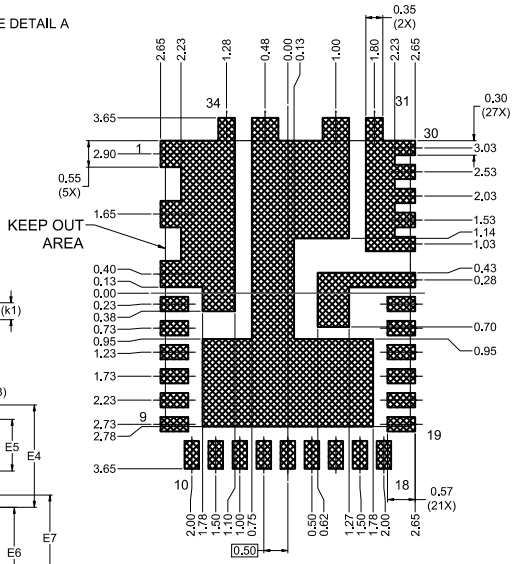

FRONT VIEW
(SCALE:2x)




BOTTOM VIEW
(SCALE:2x)




DETAIL A
(SCALE:3x)



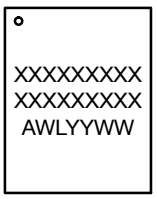

LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES: UNLESS OTHERWISE SPECIFIED
A) ALL DIMENSIONS ARE IN MILLIMETERS.
B) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
C) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2018.

| DIM | MILLIMETERS | | |
|---|---|---|---|
| | MIN. | NOM. | MAX. |
| A | 0.70 | 0.75 | 0.80 |
| A1 | 0.00 | – | 0.50 |
| A3 | | 0.20 REF | |
| b | 0.20 | 0.25 | 0.30 |
| b2 | 0.25 | 0.30 | 0.35 |
| b3 | 0.40 | 0.50 | 0.60 |
| D | 4.90 | 5.00 | 5.10 |
| D2 | 3.40 | 3.50 | 3.60 |
| D3 | 0.98 | 1.08 | 1.18 |
| D4 | 0.73 | 0.83 | 0.93 |
| D5 | 0.50 | 0.60 | 0.70 |
| D6 | 1.87 | 1.97 | 2.07 |
| D7 | 0.45 | 0.55 | 0.65 |
| D8 | 0.20 | 0.30 | 0.40 |
| D9 | 0.20 | 0.30 | 0.40 |
| D10 | 0.65 | 0.75 | 0.85 |
| E | 6.90 | 7.00 | 7.10 |
| E2 | 1.68 | 1.78 | 1.88 |
| E3 | 3.40 | 3.50 | 3.60 |
| E4 | 2.03 | 2.13 | 2.23 |
| E5 | 0.98 | 1.08 | 1.18 |
| E6 | 1.89 | 1.99 | 2.09 |
| E7 | 2.15 | 2.25 | 2.35 |
| E8 | 0.25 | 0.35 | 0.45 |
| e | | 0.50 BSC | |
| e1 | | 1.25 BSC | |
| e2 | | 1.47 BSC | |
| e3 | | 0.80 BSC | |
| e4 | | 0.275BSC | |
| k1 | | 0.35 REF | |
| k2 | | 0.25 REF | |
| k3 | | 0.30 REF | |
| k4 | | 0.54 REF | |
| k5 | | 0.75 REF | |
| k6 | | 0.40 REF | |
| k7 | | 0.63 REF | |
| L | 0.30 | 0.40 | 0.50 |

## GENERIC MARKING DIAGRAM*




XXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

| | | | |
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