





**Block Diagram**

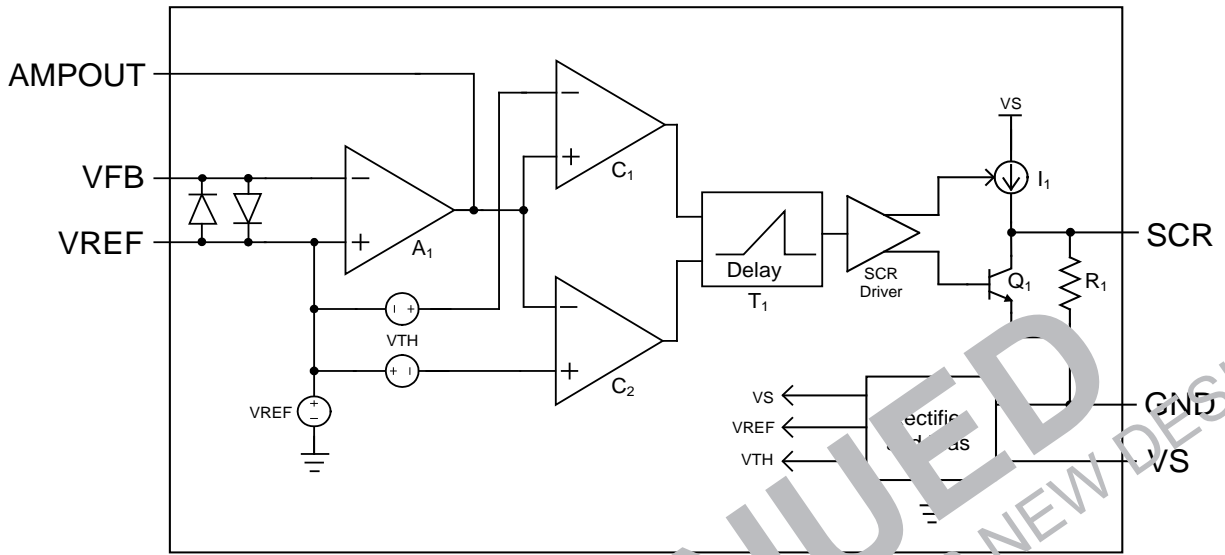


Figure 1. Block Diagram

**Typical Application**

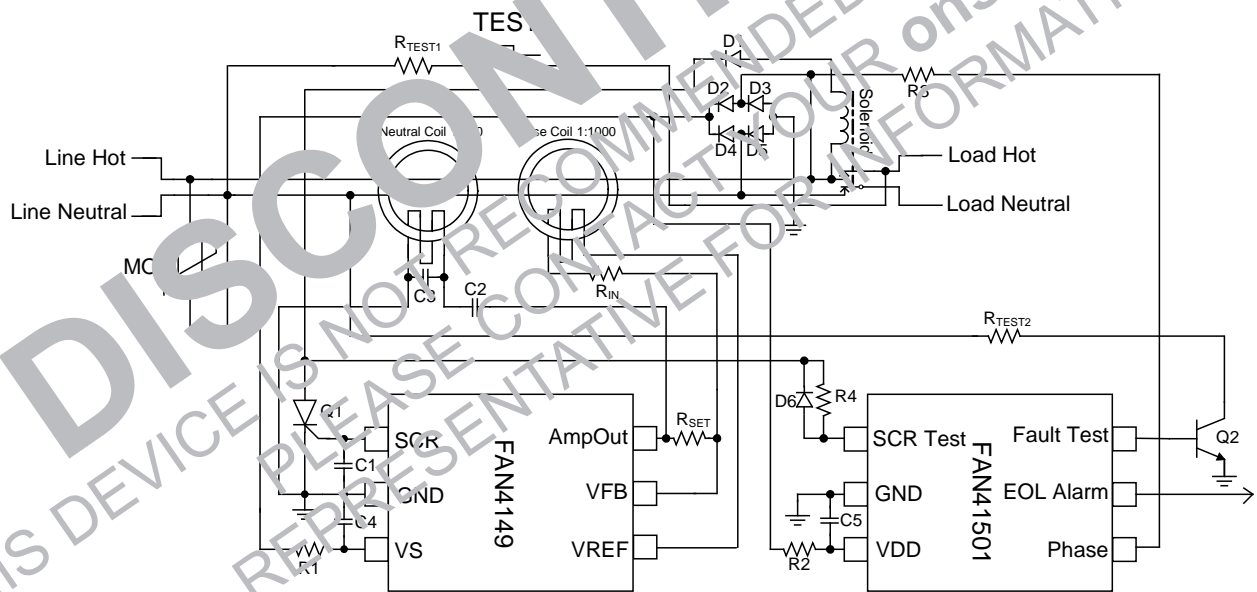


Figure 2. Typical Application<sup>(1,2)</sup>

**Table 1. Typical Values**

R1: 75 kΩ	R <sub>IN</sub> : 470 Ω	R <sub>TEST1</sub> : 15 kΩ	R <sub>TEST2</sub> : 10 kΩ	R <sub>SET</sub> : 750 kΩ <sup>(3)</sup>
R2: 75 kΩ	R3: 1 MΩ	R4: 909 kΩ	C1: 22 nF	C2: 10 nF
C3: 5.6 nF	C4: 220 nF	C5: 1 μF		

XMFR: Magnetic Metals 5029/F3006

**Notes:**

1. Contact Fairchild for self-test requirement details.
2. Portions of this schematic are subject to U.S. patents 8,085,516 and 8,760,824.
3. Value depends on sense-coil characteristics and application.

### Pin Configuration

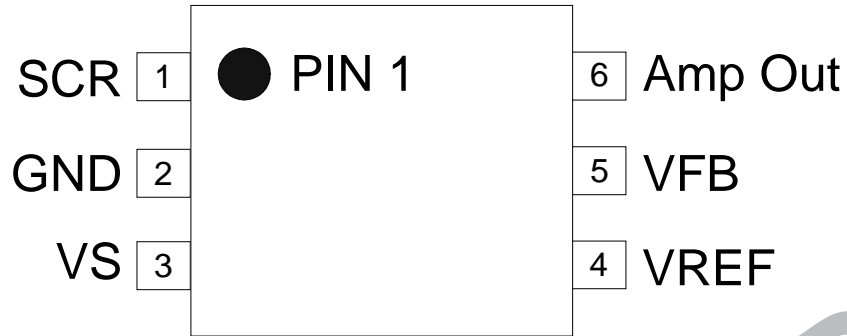


Figure 3. Pin Configuration

### Pin Definitions

Pin #	Name	Description
1	SCR	Gate drive for external SCR
2	GND	Supply input for FAN4149 circuitry
3	VS	Supply input for FAN4149 circuitry
4	VREF	Non-inverting input for current sense amplifier
5	VFB	Inverting input for current sense amplifier
6	Amp Out	An external resistor connected to VFB sets the I <sub>FAULT</sub> sensitivity threshold

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## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Condition	Min.	Max.	Unit
$I_{CC}$	Supply Current	Continuous Current, VS to GND		15	mA
$V_{CC}$	Supply Voltage	Continuous Voltage to GND, All Pins	-0.8	16.0	V
$T_{STG}$	Storage Temperature Range		-65	+150	°C
ESD	Electrostatic Discharge Capability	Human Body Model, ANSI/ESDA/JEDEC JS-001-2012		2.5	kV
		Charged Device Model, JESD22-C101		1.0	

## DC Electrical Characteristics

Unless otherwise specified,  $T_A=25^\circ\text{C}$ ,  $I_{shunt}=1\text{ mA}$ , and referencing Figure 2.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
$V_{REG}$	Power Supply Shunt Regulator Voltage	VS to GND	13.7	14.0	14.3	V
$I_Q$	Quiescent Current	VS to GND=10 V	425	500	575	$\mu\text{A}$
$V_{REF}$	Reference Voltage	$V_{REF}$ to GND	6.85	7.00	7.15	V
$V_{TH}$	Trip Threshold	Amp Out to $V_{REF}$	4.35	4.50	4.65	V
$V_{OS}$	Amplifier Offset	Gain=1000	-175	$\pm 50$	175	$\mu\text{V}$
	Amplifier Offset Drift <sup>(4)</sup>	Gain=1000	-100		100	$\mu\text{V}$
$I_{OS}$	Amplifier Input Offset <sup>(4)</sup>	Design Value	-50	0	50	nA
$G$	Amplifier DC Gain <sup>(4)</sup>	Design Value		100		dB
$GBW$	Amplifier Gain Bandwidth <sup>(5)</sup>	Design Value		3		MHz
$V_{SW+}$	Amplifier Positive Voltage Swing	Amp Out to $V_{REF}$ , $I_{FAULT}=10\ \mu\text{A}$	5.5			V
$V_{SW-}$	Amplifier Negative Voltage Swing	$V_{REF}$ to Amp Out, $I_{FAULT}=-10\ \mu\text{A}$	5.5			V
$I_{SNK}$	Amplifier Current Sink	Amp Out= $V_{REF} + 3\text{ V}$ , $V_{FB}=V_{REF} + 100\text{ mV}$	400			$\mu\text{A}$
$I_{SRL}$	Amplifier Current Source	Amp Out= $V_{REF} - 3\text{ V}$ , $V_{FB}=V_{REF} - 100\text{ mV}$	400			$\mu\text{A}$
$t_d$	Delay Filter	Delay from $C_1$ Trip to SCR L->H	0.65	1.00	1.35	ms
$R_{OUT}$	SCR Output Resistance	SCR to GND=250 mV, Amp Out= $V_{REF}$		0.5	1.0	k $\Omega$
$V_{OUT}$	SCR Output Voltage	SCR to GND, Amp Out= $V_{REF}$		1	10	mV
	SCR Output Voltage	SCR to GND, AMP Out= $V_{REF} + 4\text{ V}$	3.0			V
$I_{OUT}$	SCR Output Current	SCR to GND=1 V Amp Out= $V_{REF} + 4\text{ V}$ , $I_{SHUNT}=2\text{ mA}$	650	725		$\mu\text{A}$

### Notes:

- Maximum  $V_{OS}$  offset temperature cycling drift from initial value (JEDEC JESD22-A104).
- Guaranteed by design, not tested in production.

## Functional Description

Refer to Figure 2.

The FAN4149 is a GFCI controller for AC ground-fault circuit interrupters. The low- $V_{OS}$  offset for the sense amplifier allows for direct DC coupling of the sense coil when the FAN4149 is biased with a full-wave diode bridge. This allows for the FAN4149 to be used with the FAN41501 digital auto-monitoring controller to provide for a low-BOM-cost, complete, GFI solution with self testing for the critical GFCI components.

The internal shunt regulator rectifier circuit is supplied from the full-wave rectifier bridge and 75 k $\Omega$  series resistor. A typical 220 nF  $V_S$  bypass capacitor is used to filter the  $V_{AC}$  ripple voltage. The internal 14 V shunt regulator uses a precision temperature-compensated bandgap reference. The combination of precision reference circuitry and precision sense amplifier provides for an accurate ground-fault tolerance. This allows for selection of external components with wider and lower-cost parameter variations. Due to the low quiescent current, a high-value external series resistor ( $R_1$ ) can be used to reduce the maximum power wattage required for this resistor. The 14 V shunt regulator generates the  $V_{REF}$  reference voltage for the sense amplifier's ( $A_1$ ) non-inverting input (AC ground reference). It also supplies the bias for the delay timer ( $t_1$ ), comparators ( $C_1$  &  $C_2$ ), and the SCR driver.

The secondary winding of the sense transformer is connected to pin 4 ( $V_{REF}$ ) and to a resistor  $R_{IN}$ , which is directly DC connected to the inverting input of the sense amplifier at pin 5 ( $V_{FB}$ ). The feedback resistor ( $R_{SET}$ ) converts the sense transformer's secondary current to a voltage at pin 5 ( $V_{FB}$ ). This voltage is compared to the window comparator ( $C_1$  &  $C_2$ ). When the  $V_{FB}$  voltage exceeds the  $\pm V_{TH}$  threshold voltage, the window comparator triggers the internal delay timer. The output of the window comparator must stay HIGH for the duration of the  $t_1$  timer. If the window comparator's output goes LOW, the internal delay timer starts a reset cycle. If the window comparator's output is still HIGH at the end of the  $t_1$  pulse, the SCR driver enables current source  $I_1$  and disables Q1. Current source  $I_1$  then enables the external SCR, which energizes the solenoid, opens the contact switches to the load, and removes the hazardous ground fault. The window comparator allows for detection of a positive or negative  $I_{FAULT}$  signal, independent from the phase of the line voltage.

### Calculation of $R_{SET}$ Resistor

The Amp Out signal must exceed the window comparator's  $V_{TH}$  threshold voltage for longer than the delay timer and calculated by:

$$V_{TH} = I_{FAULT} \times 1.22 \times R_{SET} \times \text{COS}(2\pi \times (t/2P)) / N \quad (1)$$

$$R_{SET} = (V_{TH} \times N) / (1.22 \times I_{FAULT} \times \text{COS}(\pi \times t/P)) \quad (2)$$

where:

$$V_{TH} = 4.5 \text{ V}$$

$$I_{FAULT} = 5 \text{ mA}_{RMS} \text{ (UL943)}$$

$$T = 1 \text{ ms (timer delay)}$$

$$P = \text{Period of the AC Line (1/60 Hz)}$$

$$P = \text{Period of the AC Line (1/60 Hz)}$$

$$N = \text{Ratio of secondary-to-primary turns (1000:1)}$$

$$R_{SET} = 750 \text{ k}\Omega \text{ (standard 1\% value)}$$

In practice, the transformer is non-ideal, so  $R_{SET}$  may need to be adjusted by up to 30% to obtain the desired  $I_{FAULT}$  trip threshold.

### Calculation of $V_{OS}$ Trip Threshold Error

Since the sense coil is directly connected to the feedback of the sense amplifier, the  $V_{OS}$  offset introduces an  $I_{FAULT}$  threshold error. The error can be calculated as follows:

$$\%Error = 100 \times (V_{OS} \times R_{SET} / (R_{IN} + R_{LDC})) / V_{TH} \quad (3)$$

$$V_{OS} = \pm 175 \mu\text{V (worst case)}$$

$$V_{OS} = \pm 50 \mu\text{V (typical)}$$

$$R_{SET} = 750 \text{ k}\Omega$$

$$R_{IN} = 470 \Omega \text{ (typical value)}$$

$$R_{LDC} = 75 \Omega \text{ (sense coil secondary DC resistance)}$$

$$V_{TH} = 4.5 \text{ V}$$

$$\%Error = \pm 5.4\% \text{ (worst case)}$$

$$\%Error = \pm 1.5\% \text{ (typical)}$$

The  $V_{OS} \pm 100 \mu\text{V}$  maximum drift specification is based on temperature cycling per JEDEC JESD22-A104, Condition B, 850 temperature cycles at  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .

### Grounded Neutral Detection

If the neutral load terminal side is incorrectly connected to the earth ground, the sense coil does not correctly detect the hazardous ground fault current from "load hot" to earth ground due to the partial  $I_{FAULT}$  current flowing from the grounded neutral fault (load neutral) to earth ground.

To detect a grounded neutral fault, a grounded neutral coil is required. When a low resistive path occurs from the line neutral and load neutral terminals, the sense and neutral coils are mutually coupled. The mutual coupling produces a positive feedback path around the sense amplifier, which causes the sense amplifier to oscillate. When the peak oscillation voltage exceeds the SCR trigger threshold, the internal delay timer is enabled. Since the amplifier's output signal is crossing the window comparator's trip threshold typically at 6 kHz, the delay timer alternates between detection of a fault/no-fault. The ratio of the fault/no-fault detection time interval determines if the SCR driver is enabled.

The sensitivity of the grounded neutral detection can be changed by the neutral coil turns and the value of  $C_2$  and  $C_3$ .

### GFCI Self Test Requirement

Starting in June of 2015, UL943 requires all permanently connected GFCI products to perform a self-test function. By adding Fairchild's FAN41501 product to the FAN4149 application (see *Figure 2*), a fully compliant 2015 UL943 self-test function can be achieved with two, small, independent, 6-pin, 1.6 mm-wide devices and a minimum number of external components. The 2015 UL code requires that, at power up, the GFCI self test the critical GFCI components --

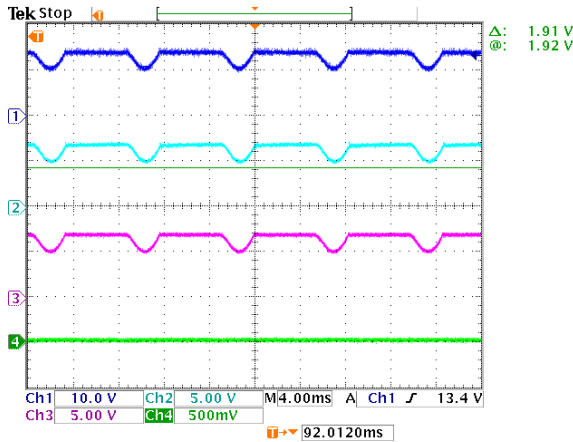
FAN4149, SCR, sense coil, and solenoid -- within five seconds and thereafter within every three hours. The self-test cycle cannot open the load contacts. If a component failure is detected, the load power must be denied. Refer to the [FAN41501](#) datasheet for more details about the UL943 self-test features.

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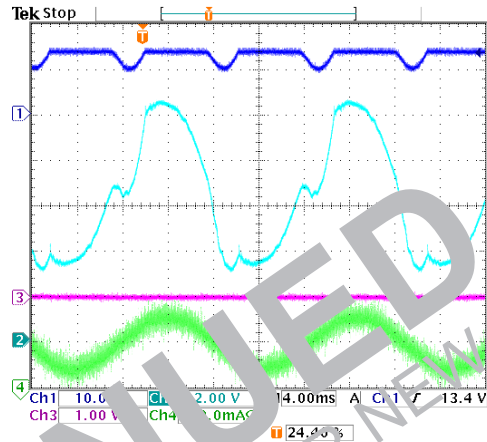
## Typical Performance Characteristics

Unless otherwise specified,  $T_A=25^{\circ}\text{C}$  and according to Figure 2 with SCR disconnected.



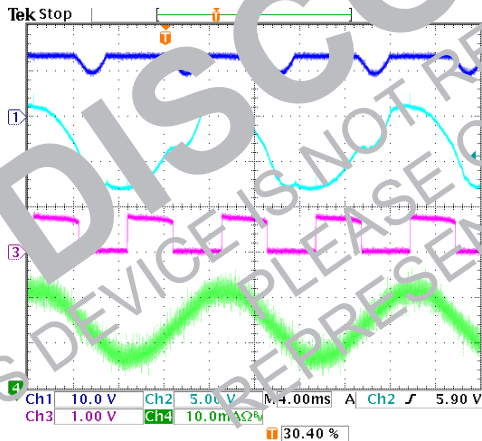
Ch1: VS (Pin 3), 10 V/Div  
 Ch2: AmpOut (Pin 6), 5 V/Div  
 Ch3: VREF (Pin 4), 5 V/Div  
 Ch4: SCR (Pin 1), 500 mV/Div

Figure 4. Typical Waveforms, No Ground Fault



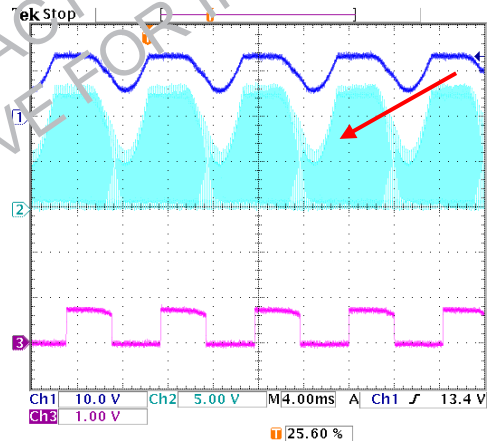
Ch1: VS (Pin 3), 10 V/Div  
 Ch2: AmpOut (Pin 6), 2 V/Div  
 Ch3: SCR (Pin 1), 1 V/Div  
 Ch4: I\_FAULT (Pin 1), 10 mA/Div

Figure 5. Typical Waveforms, 4 mA Ground Fault



Ch1: VS (Pin 3), 10 V/Div  
 Ch2: AmpOut (Pin 6), 5 V/Div  
 Ch3: SCR (Pin 1), 1 V/Div  
 Ch4: I\_FAULT (Pin 1), 10 mA/Div

Figure 6. Typical Waveforms, 5 mA Ground Fault



Ch1: VS (Pin 3), 10 V/Div  
 Ch2: AmpOut (Pin 6), 5 V/Div  
 Ch3: SCR (Pin 1), 1 V/Div

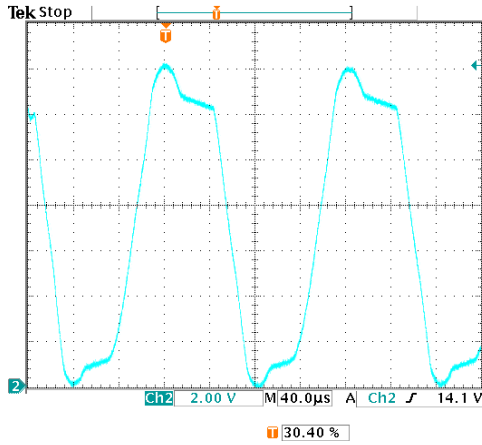
Figure 7. Typical Waveforms for Grounded Neutral Detection

Continued on the following page...



**Typical Performance Characteristics** (Continued)

Unless otherwise specified,  $T_A=25^{\circ}\text{C}$  and according to Figure 1 with SCR disconnected.



Ch2: AmpOut (Pin 6), 2 V/Div

**Figure 8. Typical Waveform for Grounded Neutral Detection**

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## Typical Temperature Characteristics

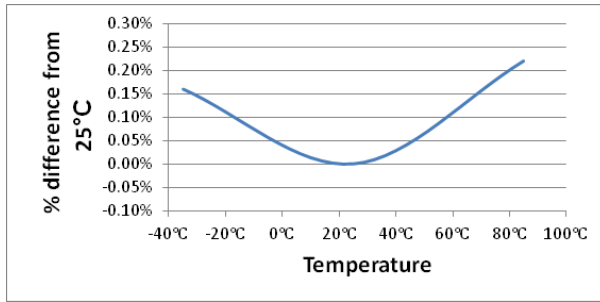


Figure 9. Shunt Regulator Voltage vs. Temperature

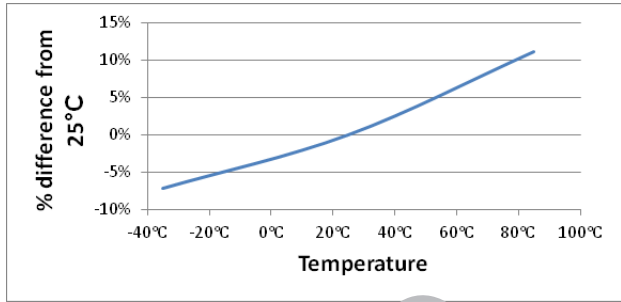


Figure 10. Quiescent Current vs. Temperature

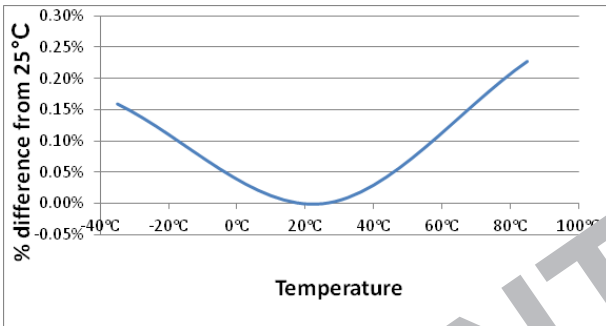


Figure 11. Reference Voltage vs. Temperature

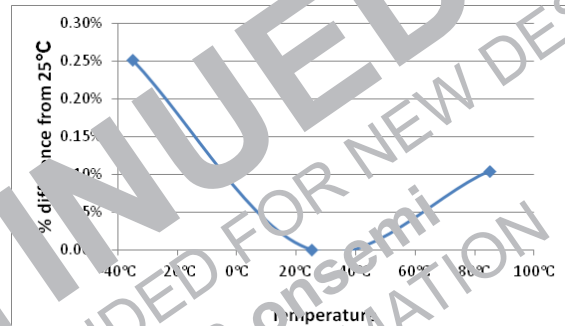


Figure 12. VH Threshold Voltage vs. Temperature

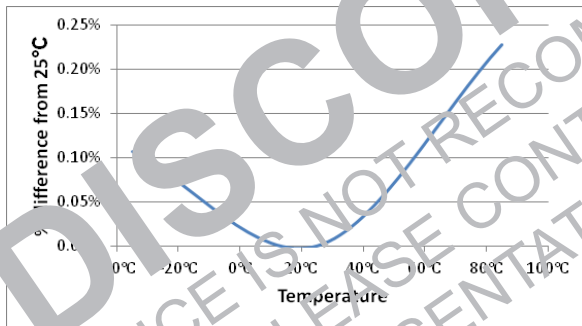


Figure 13. VL Threshold Voltage vs. Temperature

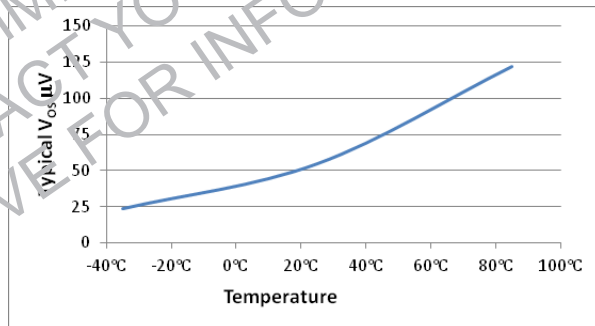


Figure 14. Typical VOS vs. Temperature

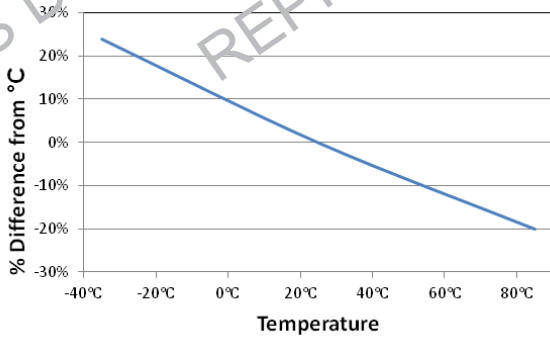
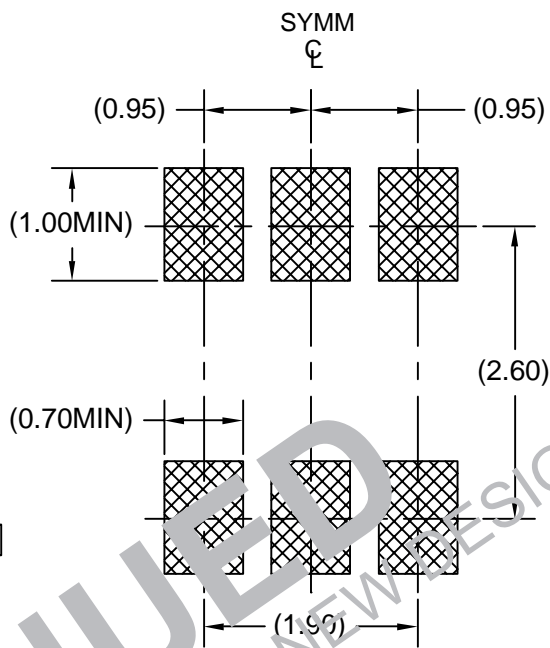
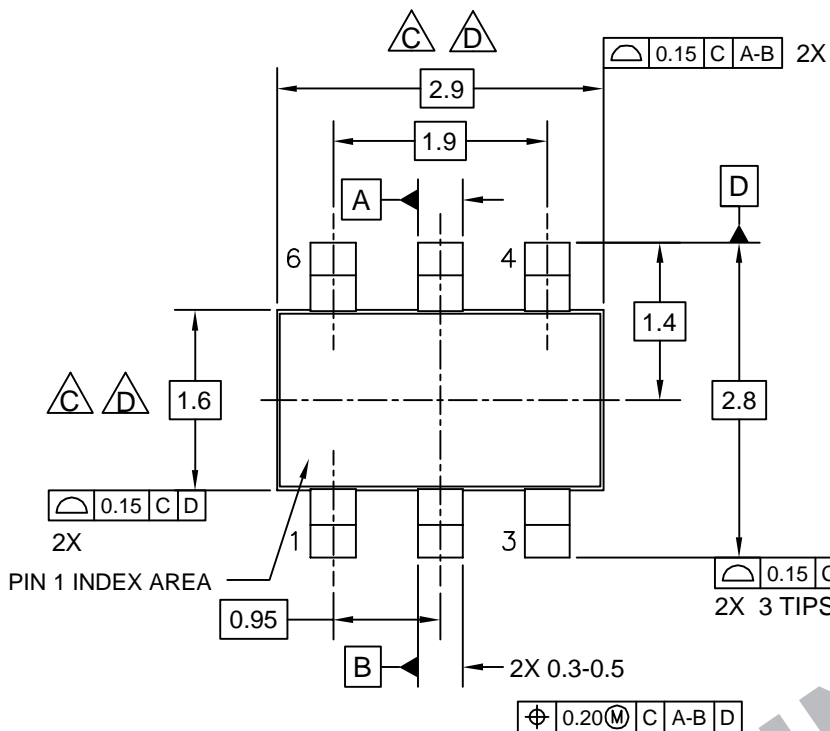
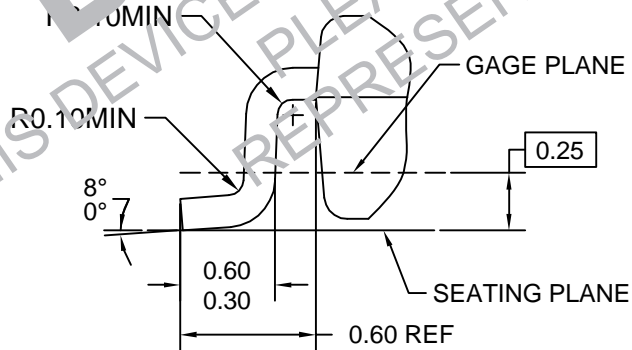
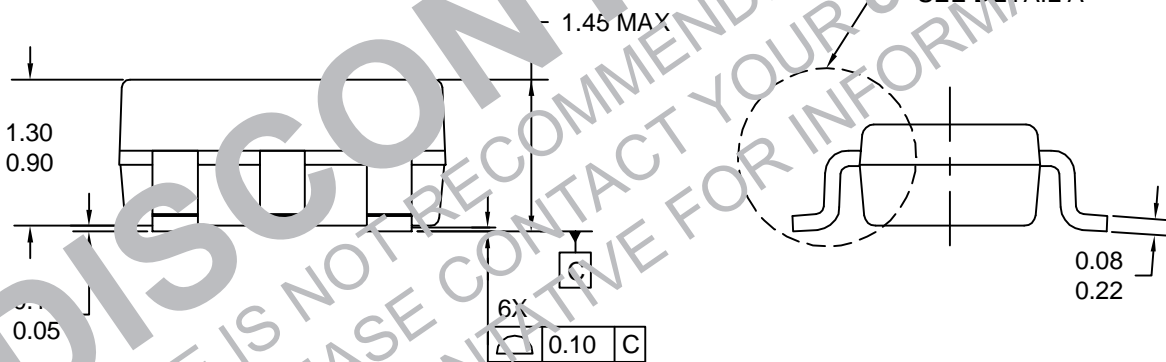


Figure 15. IOUT SCR Out vs. Temperature

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LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
A	RELEASE TO DOCUMENT CONTROL	ECN-MKT-MA06E	11/4/2006	H.ALLEN
2	DWG UPDATED TO CONFORM TO MO178		5 JULY 07	L.HUEBENER



LAND PATTERN RECOMMENDATION



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- F. DRAWING FILE NAME: MA06EREV2

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CHECKED: H.ALLEN		17 JULY 07			
APPROVED:					
6LD,SOT23,JEDEC MO-178 VARIATION AB, 1.6MM WIDE					
		SCALE 1:1	SIZE NA	DRAWING NUMBER MKT-MA06E	REV 2
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