# Synchronous Regulator with Bypass Mode, TINYBOOST®, 2.5 MHz, 1500 mA

# FAN48630J

**ON Semiconductor®**

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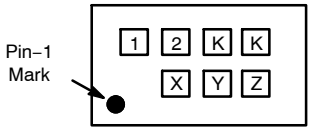
**WLCSP16 1.78x1.78x0.586**
**CASE 567SY**

**MARKING DIAGRAM**




12 = Alphanumeric Device Marking
KK = Lot Rune Code
X = Alphabetical Year Code
Y = 2−weeks Date Code
Z = Assembly Plant Code

**ORDERING INFORMATION**

See detailed ordering and shipping information on page 2 of this data sheet.

### Description

The FAN48630J allows systems to take advantage of new battery chemistries that can supply significant energy when the battery voltage is lower than the required voltage for system power ICs. By combining built−in power transistors, synchronous rectification, and low supply current; this IC provides a compact solution for systems using advanced Li−Ion battery chemistries.

The FAN48630J is a boost regulator designed to provide a minimum output voltage ($V_{OUT(MIN)}$) from a single−cell Li−Ion battery, even when the battery voltage is below system minimum. Output voltage regulation is guaranteed to a maximum load current of 1500 mA. Quiescent current in Shutdown Mode is less than 3 μA, which maximizes battery life. The regulator transitions smoothly between Bypass and normal Boost Mode. The device can be forced into Bypass Mode to reduce quiescent current.

The FAN48630J is available in a 16−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

### Features

- 3 External Components: 0.47 μH Inductor and 0603 Case Size Input and Output Capacitors
- Input Voltage Range: 2.35 V to 5.5 V
- Fixed Output Voltage Option: 3.15 V/3.6 V
- Up to 96% Efficient
- True Bypass Operation when $V_{IN}$ > Target $V_{OUT}$
- Internal Synchronous Rectifier
- Soft−Start with True Load Disconnect
- Forced Bypass Mode
- $V_{SEL}$ Control to Optimize Target $V_{OUT}$
- Short−Circuit Protection
- Low Operating Quiescent Current
- 16−Bump, 0.4 mm Pitch WLCSP

### Applications

- Boost for Low−Voltage Li−ion Batteries, Brownout Prevention, Boosted Audio, USB OTG, and LTE / 3G RF Power
- Cell Phones, Smart Phones, Portable Instruments

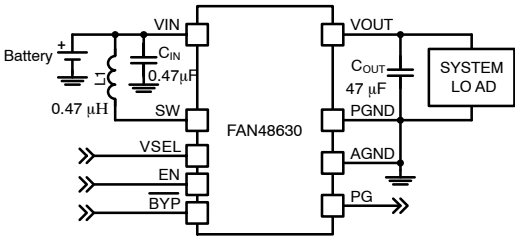



**Figure 1. Typical Application**

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**Table 1. ORDERING INFORMATION**

| Part Number | Output Voltage $V_{SELO}/V_{SEL1}$ | Operating Temperature | Package | Shipping† | Device Marking |
|---|---|---|---|---|---|
| FAN48630BUC31JX | 3.15 V/3.60 V | −40 to 85°C | WLCSP | Tape & Reel | JH |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

## TYPICAL APPLICATION

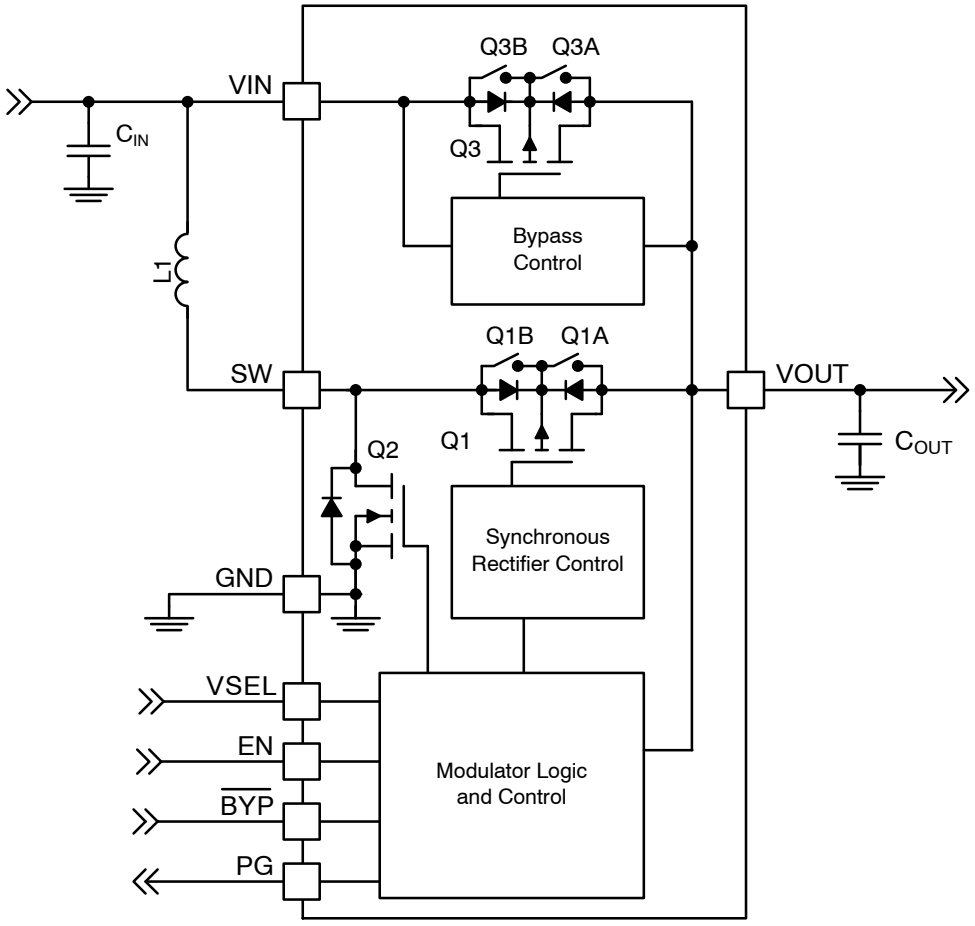


**Figure 2. Typical Application Block Diagram**

**Table 2. RECOMMENDED COMPONENTS**

| Component | Description | Vendor | Parameter | Typ. | Unit |
|---|---|---|---|---|---|
| L1 | 0.47 μH, 30% | Toko: DFE201612C<br>DFR201612C<br>Cyntec: PIFE20161B | L | 0.47 | μH |
| $C_{IN}$ | 4.7 μF, 10%, 6.3 V, X5R, 0603 (1608) | Murata: GRM188R60J475K<br>TDK: C1608X5R0J475K | C | 4.7 | μF |
| $C_{OUT}$ | 47 μF, 20%, 6.3 V, X5R, 0603 (1608) | Samsung: CL10A476MQ8CZNE | C | 47 | |

## PIN CONFIGURATION

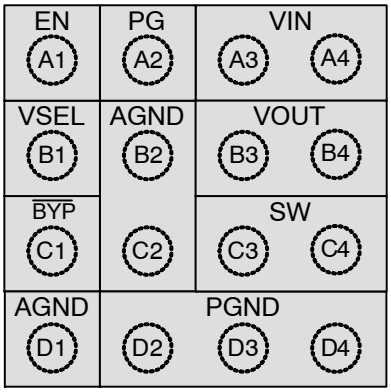


**Figure 3. Top Through View (Bumps Down)**

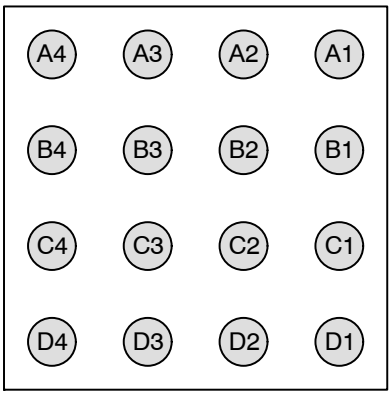


**Figure 4. Bottom View**

**Table 3. PIN DEFINITIONS**

| Pin # | Name | Description |
|---|---|---|
| A1 | EN | Enable. When this pin is HIGH, the circuit is enabled (Note 1). |
| A2 | PG | Power Good. This is an open−drain output. PG is actively pulled LOW if output falls out of regulation due to overload or if thermal protection threshold is exceeded. |
| A3–A4 | VIN | Input Voltage. Connect to Li−Ion battery input power source. |
| B1 | VSEL | Output Voltage Select. When boost is running, this pin can be used to select output voltage. |
| B2, C2, D1 | AGND | Analog Ground. This is the signal ground reference for the IC. All voltage levels are measured with respect to this pin. |
| B3–B4 | VOUT | Output Voltage. Place $C_{OUT}$ as close as possible to the device. |
| C1 | $\overline{BYP}$ | Bypass. This pin can be used to activate Forced Bypass Mode. When this pin is LOW, the bypass switches (Q3 and Q1) are turned on and the IC is otherwise inactive. |
| C3–C4 | SW | Switching Node. Connect to inductor. |
| D2–D4 | PGND | Power Ground. This is the power return for the IC. The $C_{OUT}$ bypass capacitor should be returned with the shortest path possible to these pins. |

1. Do not connect the EN pin to VIN. A logic voltage of 1.8 V should control the EN pin and enable/disable the device.

**Table 4. ABSOLUTE MAXIMUM RATINGS**

| Symbol | Parameter | | Min. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | $V_{IN}$ Input Voltage | | −0.3 | 6.5 | V |
| $V_{OUT}$ | $V_{OUT}$ Output Voltage | | | 6.0 | V |
| | SW Node | DC | −0.3 | 8.0 | V |
| | | Transient: 10 ns, 3 MHz | −1.0 | 8.0 | V |
| | Other Pins | | −0.3 | 6.5 (Note 2) | V |
| ESD | Electrostatic Discharge Protection Level | Human Body Model per JESD22−A114 | 2.0 | | kV |
| | | Charged Device Model per JESD22−C101 | 1.5 | | kV |
| $T_J$ | Junction Temperature | | −40 | +150 | °C |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
2. Lesser of 6.5 V or $V_{IN}$ + 0.3 V.

**Table 5. RECOMMENDED OPERATING CONDITIONS**

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage | 2.35 | 5.5 | V |
| $I_{OUT}$ | Output Current | 0 | 1500 | mA |
| $T_A$ | Ambient Temperature | −40 | +85 | °C |
| $T_J$ | Junction Temperature | −40 | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

**Table 6. THERMAL PROPERTIES**

| Symbol | Parameter | Typ. | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction−to−Ambient Thermal Resistance | 80 | °C/W |
| $\theta_{JB}$ | Junction−to−Board Thermal Resistance | 42 | |

Junction−to−ambient thermal resistance is a function of application and board layout. This data is measured with four−layer Fairchild evaluation boards (1 oz copper on all layers). Special attention must be paid not to exceed junction temperature $T_{J(max)}$ at a given ambient temperate $T_A$.

**Table 7. ELECTRICAL CHARACTERISTICS** Recommended operating conditions, unless otherwise noted, circuit per Figure 1, $V_{IN}$ = 2.35 V to 5.5 V, $T_A$ = −40°C to 85°C. Typical values are given at $V_{IN}$ = 3.0 V and $T_A$ = 25°C.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $I_Q$ | $V_{IN}$ Quiescent Current | Bypass Mode $V_{OUT}$ = 3.15 V, $V_{IN}$ = 4.2 V | | 140 | 190 | μA |
| | | Boost Mode $V_{OUT}$ = 3.15 V, $V_{IN}$ = 2.5 V | | 150 | 250 | μA |
| | | Shutdown: EN = 0, $V_{IN}$ = 3.0 V | | 1.5 | 5.0 | μA |
| | | Forced Bypass Mode, $V_{IN}$ = 3.5 V | | 4 | 10 | μA |
| $I_{LK}$ | VOUT to VIN Reverse Leakage | $V_{OUT}$ = 3.6 V, EN = 0 | | 0.2 | 1.0 | μA |
| $I_{LK_OUT}$ | $V_{OUT}$ Leakage Current | $V_{OUT}$ = 0, EN = 0, $V_{IN}$ = 4.2 V | | 0.1 | 1.0 | μA |
| $V_{UVLO}$ | Under−Voltage Lockout | $V_{IN}$ Rising | | 2.20 | 2.35 | V |
| $V_{UVLO_HYS}$ | Under−Voltage Lockout Hysteresis | | | 200 | | mV |
| $V_{PG(OL)}$ | PG Low | $I_{PG}$ = 5 mA | | | 0.4 | V |
| $I_{PG_LK}$ | PG Leakage Current | | | | 1 | μA |
| $V_{IH}$ | Logic Level High EN, VSEL, $\overline{BYP}$ | | 1.2 | | | V |
| $V_{IL}$ | Logic Level Low EN, VSEL, $\overline{BYP}$ | | | | 0.4 | V |
| $R_{LOW}$ | Logic Control Pin Pull Downs (LOW Active) | $\overline{BYP}$, VSEL, EN | | 300 | | kΩ |
| $I_{PD}$ | Weak Current Source Pull−Down | $\overline{BYP}$, VSEL, EN | | 100 | | nA |
| $V_{REG}$ | Output Voltage Accuracy | 2.35 V ≤ $V_{IN}$ ≤ $V_{OUT_TARGET}$ −100 mV, DC, 0 to 1500 mA | −2 | | 4 | % |
| $f_{SW}$ | Switching Frequency | $V_{IN}$ = 2.7 V, $V_{OUT}$ = 3.15 V, Load = 1000 mA | 2.0 | 2.5 | 3.0 | MHz |
| $I_{V_LIM}$ | Boost Valley Current Limit | $V_{IN}$ = 2.6 V | 2.6 | 2.9 | 3.1 | A |
| $V_{OVP}$ | Output Over−Voltage Protection Threshold | | | 6.0 | 6.3 | V |
| $V_{OVP_HYS}$ | Output Over−Voltage Protection Hysteresis | | | 300 | | mV |
| $R_{DS(ON)N}$ | N−Channel Boost Switch $R_{DS(ON)}$ | $V_{IN}$ = 3.5 V, $V_{OUT}$ = 3.5 V | | 85 | 120 | mΩ |
| $R_{DS(ON)P}$ | P−Channel Sync Rectifier $R_{DS(ON)}$ | $V_{IN}$ = 3.5 V, $V_{OUT}$ = 3.5 V | | 65 | 85 | mΩ |
| $R_{DS(ON)P_BYP}$ | P−Channel Bypass Switch $R_{DS(ON)}$ | $V_{IN}$ = 3.5 V, $V_{OUT}$ = 3.5 V | | 65 | 85 | mΩ |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

**Table 8. SYSTEM CHARACTERISTICS**

The following table is verified by design and verified while using the following external components: L = 0.47 μH, DFE201612C−R47M (Toko), $C_{IN}$ = 4.7 μF, 0603 (1608 metric), C1608X5R0J475K (TDK), $C_{OUT}$ = 47 μF, 0603 (1608 metric), CL10A476MQ8CZNE (Samsung). These parameters are not verified in production. Minimum and maximum values are at $V_{IN}$ = 2.5 V to 5.5 V, $T_A$ = −40°C to +85°C; circuit per Figure 1, unless otherwise noted. Typical values are at $T_A$ = 25°C, $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.6 V, $V_{EN}$ = 1.8 V.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $\Delta V_{OUT_LOAD}$ | Load Regulation | $I_{OUT}$ = 0 A to 1 A, $V_{IN}$ = 3.0 V | | 80 | | mV/A |
| $\Delta V_{OUT_LINE}$ | Line Regulation | 2.7 V ≤ $V_{IN}$ ≤ 3.0 V, $I_{OUT}$ = 1 A | | 7 | | mV/V |
| $V_{OUT_RIPPLE}$ | Ripple Voltage | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.6 V, $I_{OUT}$ = 800 mA, PWM Mode | | 10 | | mV |
| | | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.6 V, $I_{OUT}$ = 50 mA, PFM Mode | | 11 | | |
| η | Efficiency | $V_{IN}$ = 2.5 V, $V_{OUT}$ = 3.15 V, $I_{OUT}$ = 20 mA, PFM | | 90 | | % |
| | | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.15 V, $I_{OUT}$ = 500 mA, PWM | | 96 | | |
| | | $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.6 V, $I_{OUT}$ = 600 mA, PWM | | 93 | | |
| $T_{SS}$ | Soft−Start | EN High to 95% of Target_ $V_{OUT}$. $R_L$ = 50 Ω | | 550 | | μs |
| $\Delta V_{OUT_LOAD_TRX}$ | Load Transient | $V_{IN}$ = 3.0 V, $I_{OUT}$ = 0.5 A ⇔1 A, $T_R$ = $T_F$ = 1 μs | | ±95 | | mV |
| $\Delta V_{OUT_LINE_TRX}$ | Line Transient | $V_{IN}$ = 2.5 V ⇔ 3.0 V, $T_R$ = $T_F$ = 10 μs, $I_{OUT}$ = 300 mA | | ±15 | | mV |

## TYPICAL CHARACTERISTICS

Unless otherwise specified; $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.6 V, and $T_A$ = 25°C; circuit and components according to Figure 1.

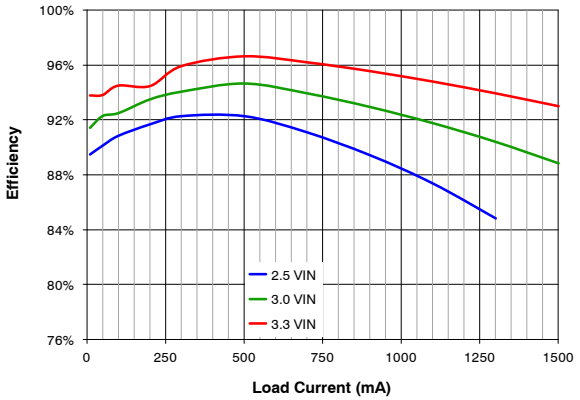


**Figure 5. Efficiency vs. Load Current and Input Voltage**

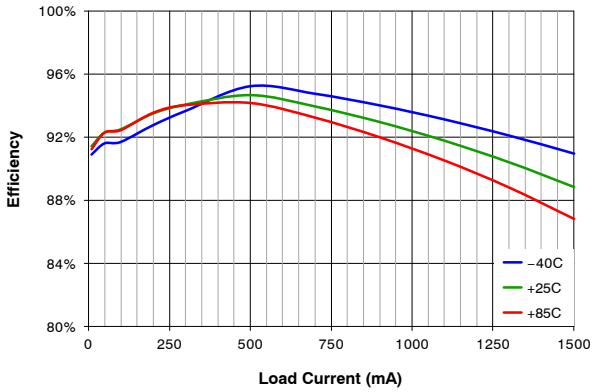


**Figure 6. Efficiency vs. Load Current and Temperature**

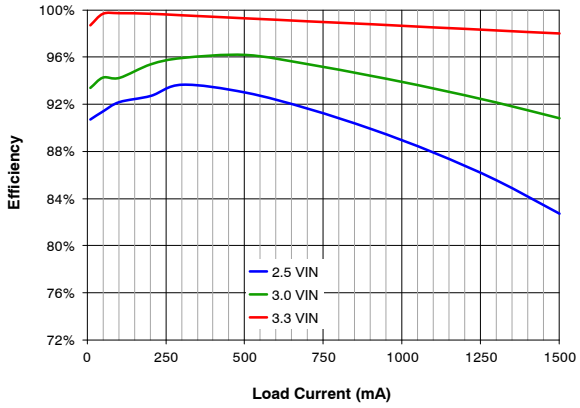


**Figure 7. Efficiency vs. Load Current and Input Voltage, $V_{OUT}$ = 3.15 V**

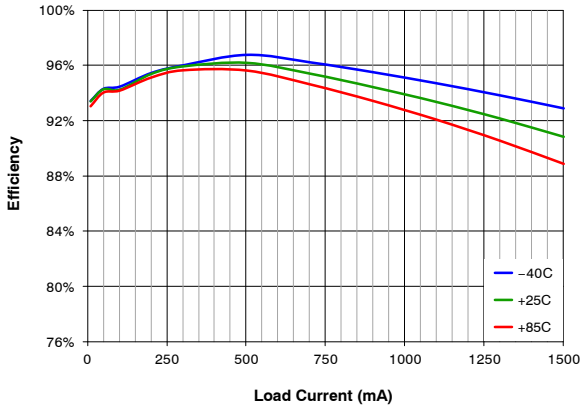


**Figure 8. Efficiency vs. Load Current and Temperature, $V_{OUT}$ = 3.15 V**

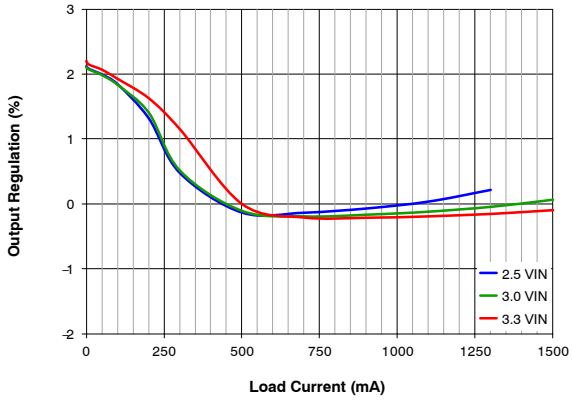


**Figure 9. Output Regulation vs. Load Current and Input Voltage**

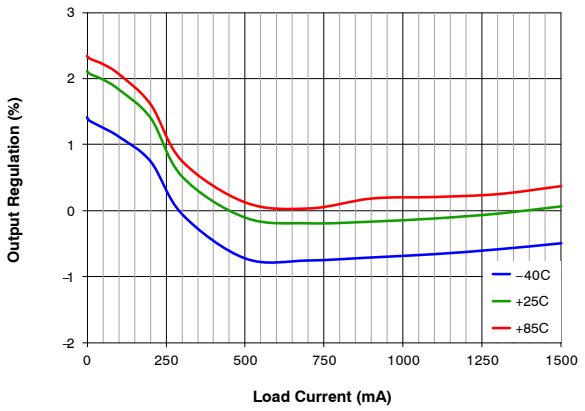


**Figure 10. Output Regulation vs. Load Current and Temperature**

## TYPICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified; $V_{IN}$ = 3.0 V, $V_{OUT}$ = 3.6 V, and $T_A$ = 25°C; circuit and components according to Figure 1.

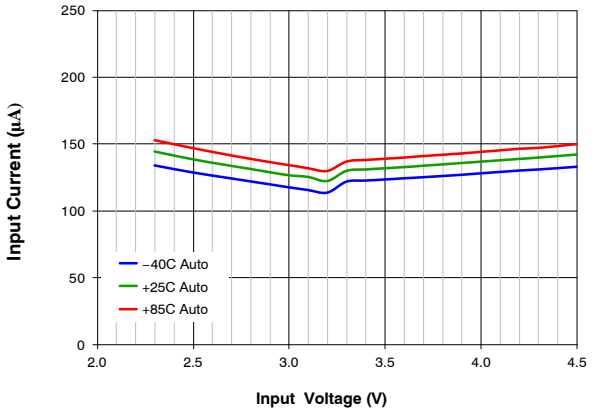


**Figure 11. Quiescent Current vs. Input Voltage and Temperature, $V_{OUT}$ = 3.15 V, Auto Mode**

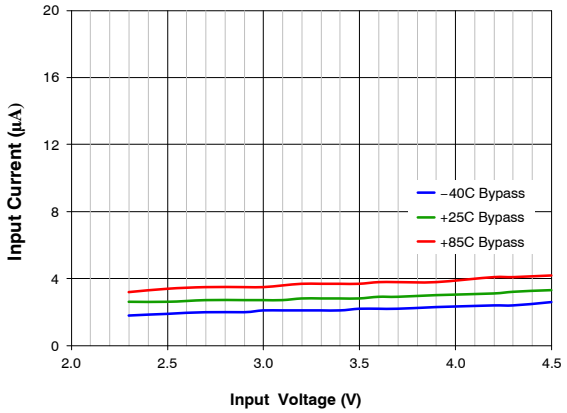


**Figure 12. Quiescent Current vs. Input Voltage and Temperature, $V_{OUT}$ = 3.15 V, Forced Bypass Mode**

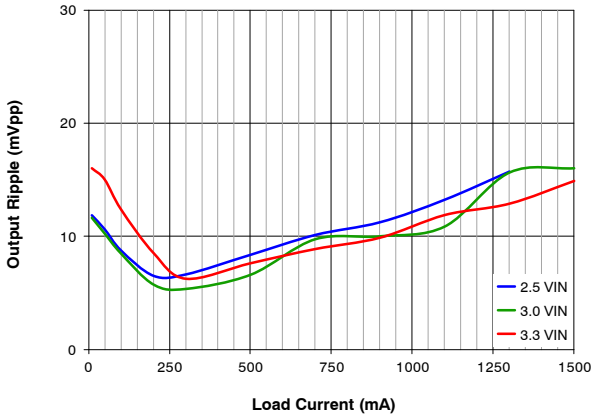


**Figure 13. Output Ripple vs. Load Current and Input Voltage**

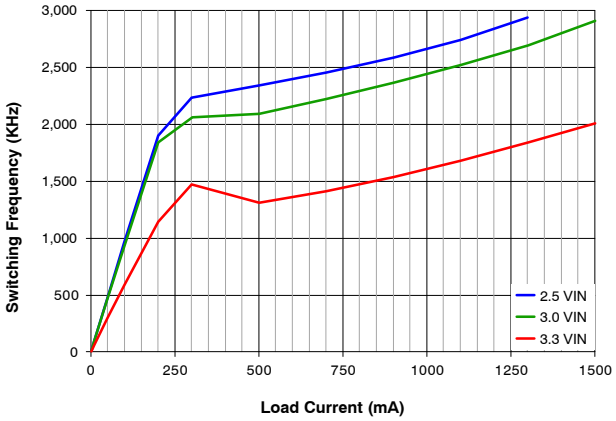


**Figure 14. Frequency vs. Load Current and Input Voltage**

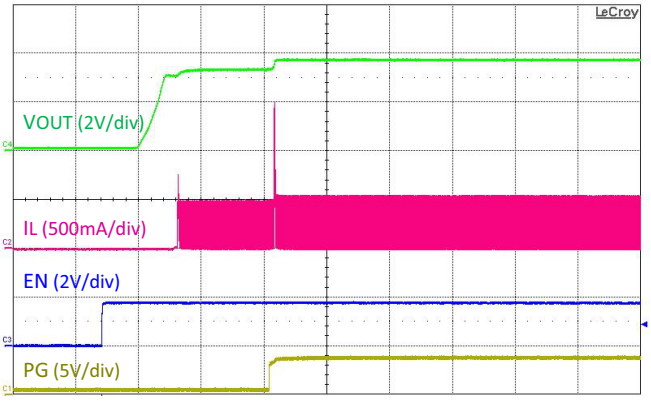


**Figure 15. Startup, 50 Ω Load**

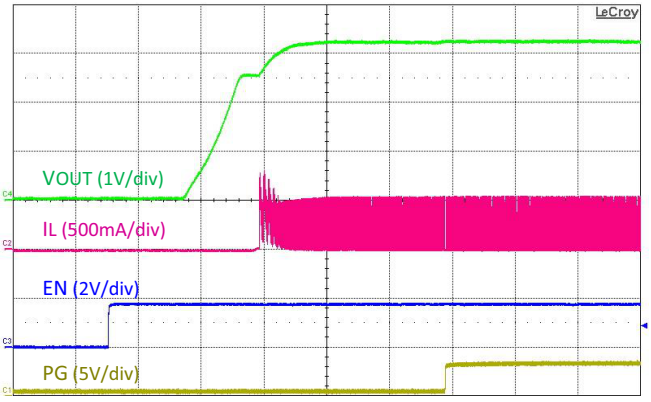


**Figure 16. Startup, 50 Ω Load, $V_{IN}$ = 2.5 V, $V_{OUT}$ = 3.15 V**

## TYPICAL CHARACTERISTICS (CONTINUED)

Unless otherwise specified, $V_{IN}$ = 3.0 V; $V_{OUT}$ = 3.6 V, and $T_A$ = 25°C; circuit and components according to Figure 1.

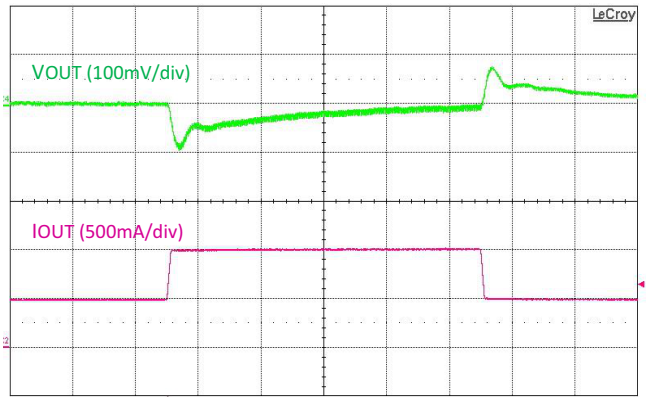


**Figure 17. Load Transient, $I_{OUT}$ = 500 ↔ 1000 mA, 1 μs Edge**

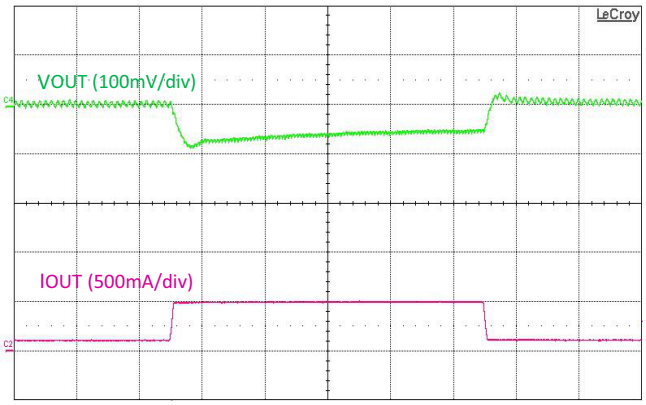


**Figure 18. Load Transient, $I_{OUT}$ = 100 ↔ 500 mA, 1 μs Edge, $V_{OUT}$ = 3.15 V**

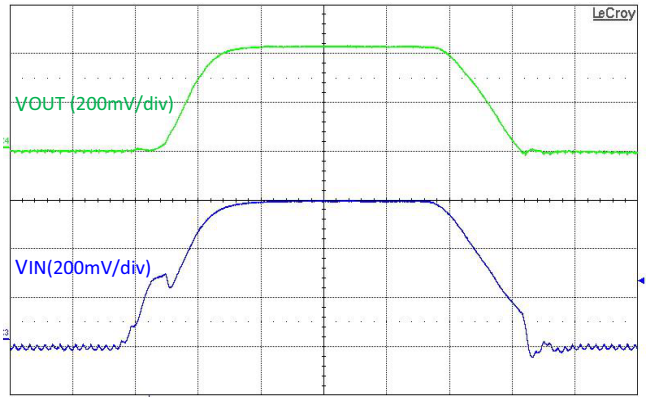


**Figure 19. Line Transient, $V_{IN}$ = 3.0 V ↔ 3.6 V, 10 μs Edge, $I_{OUT}$ = 500 mA, $V_{OUT}$ = 3.15 V**

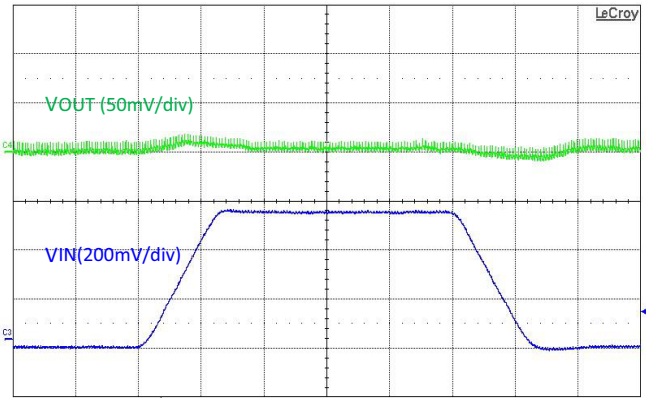


**Figure 20. Line Transient, $V_{IN}$ = 2.5 V ↔ 3.0 V, 10 μs Edge, $I_{OUT}$ = 300 mA**

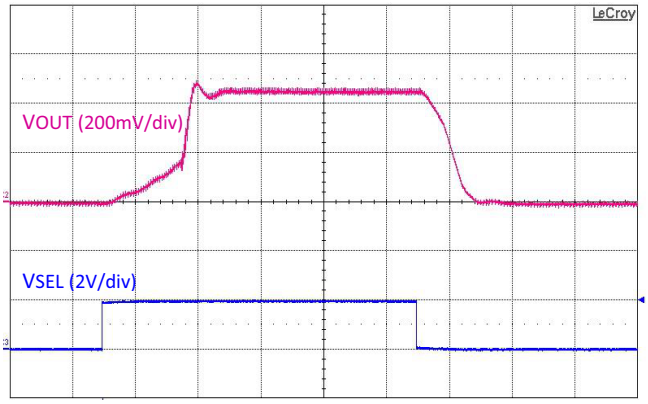


**Figure 21. $V_{SEL}$ Step, $V_{IN}$ = 3 V, $V_{OUT}$ = 3.15 ↔ V3.6 V, $I_{OUT}$ = 500 mA**

## CIRCUIT DESCRIPTION

FAN48630J is a synchronous boost regulator, typically operating at 2.5 MHz in Continuous Conduction Mode (CCM), which occurs at moderate to heavy load current and low $V_{IN}$ voltages. The regulator includes a Bypass Mode that activates when $V_{IN}$ is above the boost regulator's setpoint.

In anticipation of a heavy load transition, the setpoint can be adjusted upward by fixed amounts with the VSEL pin to reduce the required system headroom during lighter−load operation to save power.

**Table 9. Operating States**

| Mode | Description | Invoked When |
|---|---|---|
| LIN | Linear Startup | $V_{IN} > V_{OUT}$ |
| SS | Boost Soft−Start | $V_{OUT} < V_{OUT(MIN)}$ |
| BST | Boost Operating Mode | $V_{OUT} = V_{OUT(MIN)}$ |
| BPS | True Bypass Mode | $V_{IN} > V_{OUT(MIN)}$ |

### Boost Mode

The FAN48630J uses a current−mode modulator to achieve excellent transient response and smooth transitions between CCM and Discontinuous Conduction Mode (DCM) operation. During CCM operation, the device maintains a switching frequency of about 2.5 MHz. In light−load operation (DCM), frequency is reduced to maintain high efficiency.

**Table 10. Boost Startup Sequence**

| Start State | Entry | Exit | End State | Timeout (μs) |
|---|---|---|---|---|
| LIN1 | $V_{IN}$ > UVLO, EN = 1 | $V_{OUT} > V_{IN}$−300 mV | SS | |
| | | | LIN2 | 512 |
| LIN2 | LIN1 Exit | $V_{OUT} > V_{IN}$−300 mV | SS | |
| | | TIMEOUT | FAULT | 1024 |
| SS | LIN1 or LIN2 Exit | $V_{OUT} = V_{OUT(MIN)}$ | BST | |
| | | OVERLOAD TIMEOUT | FAULT | 64 |

#### Shutdown and Startup

If EN is LOW, all bias circuits are off and the regulator is in Shutdown Mode. During shutdown, current flow is prevented from $V_{IN}$ to $V_{OUT}$, as well as reverse flow from $V_{OUT}$ to $V_{IN}$. During startup, it is recommended to keep DC current draw below 500 mA.

*LIN State*

When EN is HIGH and $V_{IN}$ > UVLO, the regulator attempts to bring $V_{OUT}$ within 300 mV of $V_{IN}$ using the internal fixed current source from $V_{IN}$ (Q3). The current is limited to LIN1 set point.

If $V_{OUT}$ reaches $V_{IN}$−300 mV during LIN1 Mode, the SS state is initiated. Otherwise, LIN1 times out after 512 μs and LIN2 Mode is entered.

In LIN2 Mode, the current source is incremented to 2 A. If $V_{OUT}$ fails to reach $V_{IN}$−300 mV after 1024 μs, a fault condition is declared.

*SS State*

Upon the successful completion of the LIN state ($V_{OUT} \geq V_{IN}$−300 mV), the regulator begins switching with boost pulses current limited to 50% of nominal level.

During SS state, $V_{OUT}$ is ramped up by stepping the internal reference. If $V_{OUT}$ fails to reach regulation during the SS ramp sequence for more than 64 μs, a fault condition is declared. If large $C_{OUT}$ is used, the reference is automatically stepped slower to avoid excessive input current draw.

*BST State*

This is a normal operating state of the regulator.

*BPS State*

If $V_{IN}$ is above $V_{REG}$ when the SS Mode successfully completes, the device transitions directly to BPS Mode.

#### FAULT State

The regulator enters the FAULT state under any of the following conditions:

- $V_{OUT}$ fails to achieve the voltage required to advance from LIN state to SS state.
- $V_{OUT}$ fails to achieve the voltage required to advance from SS state to BST state.
- Boost current limit triggers for 2 ms during the BST state.
- $V_{DS}$ protection threshold is exceeded during BPS state.
- $V_{IN}$ drops below UVLO threshold.

Once a FAULT is triggered, the regulator stops switching and presents a high−impedance path between VIN to VOUT. After waiting 20 ms, a restart is attempted.

#### Power Good

Power good is 0 FAULT, 1 POWER GOOD, open−drain output.

The Power good pin is provided for signaling the system when the regulator has successfully completed soft−start and no faults have occurred. Power good also functions as an early warning flag for high die temperature and overload conditions.

- PG is released HIGH when the soft−start sequence is successfully completed.
- PG is pulled LOW when PMOS current limit has triggered for 64 μs OR the die the temperature exceeds

120CC. PG is re−asserted when the device cools below to 100CC.

- Any FAULT condition causes PG to be de−asserted.

### Over−Temperature

The regulator shuts down when the die temperature exceeds 150°C. Restart occurs when the IC has cooled by approximately 20°C.

### Bypass Operation

In normal operation, the device automatically transitions from Boost Mode to Bypass Mode, if $V_{IN}$ goes above target $V_{OUT}$. In Bypass Mode, the device fully enhances both Q1 and Q3 to provide a very low impedance path from VIN to VOUT. Entry to the Bypass Mode is triggered by condition where $V_{IN} > V_{OUT}$ and no switching has occurred during past 5 μs. To soften the entry to Bypass Mode, Q3 is driven as a linear current source for the first 5 μs. Bypass Mode exit is triggered when $V_{OUT}$ reaches the target $V_{OUT}$ voltage. During Automatic Bypass Mode, the device is short−circuit protected by voltage comparator tracking the voltage drop from $V_{IN}$ to $V_{OUT}$; if the drop exceeds 200 mV, FAULT is declared.

With sufficient load to enforce CCM operation, the Bypass Mode to Boost Mode transition occurs at the target $V_{OUT}$. The corresponding input voltage at the transition point is:

$$V_{IN} \le V_{OUT} + I_{LOAD} * (DCR_L + R_{DS(ON)P}) \| R_{DS(ON)BYP} \quad \text{(eq. 1)}$$

The Bypass Mode entry threshold has 25 mV hysteresis imposed at VOUT to prevent cycling between modes. The transition from Boost Mode to Bypass Mode occurs at the target $V_{OUT}$+25 mV. The corresponding input voltage is:

$$V_{IN} \ge V_{OUT} + 25mV + I_{LOAD} * (DCR_L + R_{DS(ON)P}) \quad \text{(eq. 2)}$$

### Forced Bypass

Entry to Forced Bypass Mode initiates with a current limit on Q3 and then proceeds to a true bypass state. To prevent reverse current to the battery, the device waits until output discharges below $V_{IN}$ before entering Forced Bypass Mode.

After the transition is complete, most of the internal circuitry is disabled to minimize quiescent current draw. Short−circuit, UVLO, output OVP and over−temperature protections are inactive in Forced Bypass Mode.

In Forced Bypass Mode, $V_{OUT}$ can follow $V_{IN}$ below $V_{OUT(MIN)}$.

### VSEL

$V_{SEL}$ can be asserted in anticipation of a positive load transient. Raising $V_{SEL}$ increases $V_{OUT(MIN)}$ by a fixed amount and $V_{OUT}$ is stepped to the corresponding target output voltage in 20 μs. The functionality can also be utilized to mitigate undershoot during severe line transients, while minimizing $V_{OUT}$ during more benign operating conditions to save power.

### EN

Setting the EN pin voltage below 0.4 V disables the part. Placing the voltage above 1.2 V enables the part. Do not connect the EN pin to VIN. A logic voltage of 1.8 V should control the EN pin and enable / disable the device. The EN pin should be pulled HIGH after the $V_{IN}$ voltage has reached a minimum voltage of 2.3 V.

## APPLICATION INFORMATION

### Output Capacitance ($C_{OUT}$)

*Stability*

The effective capacitance ($C_{EFF}$) of small, high−value, ceramic capacitors decreases as bias voltage increases. FAN48630J is guaranteed for stable operation with the minimum value of $C_{EFF}$ ($C_{EFF(MIN)}$) outlined in Table 11.

**Table 11. Minimum $C_{EFF}$ Required for Stability**

| Operating Conditions | | |
|---|---|---|
| $V_{OUT}$ (V) | $I_{LOAD}$ (mA) | $C_{EFF(MIN)}$ (µF) |
| 3.15 | 0 to 1500 | 15 |

$C_{EFF}$ varies with manufacturer, material, and case size.

*Inductor Selection*

Recommended nominal inductance value is 0.47 µH.

FAN48630J employs valley−current limiting; peak inductor current can reach 3.8 A for a short duration during overload conditions. Saturation effects cause the inductor current ripple to become higher under high loading as only valley of the inductor current ripple is controlled.

A 0.33 µH inductor can be used for improved transient performance.

*Startup*

Input current limiting is in effect during soft−start, which limits the current available to charge $C_{OUT}$ and any additional capacitance on the $V_{OUT}$ line. If the output fails to achieve regulation within the limits described in the Startup section, a FAULT occurs, causing the circuit to shut down then restart after 20 ms. If the total combined output capacitance is very high, the circuit may not start on the first attempt, but eventually achieves regulation if no load is present. If a high−current load and high capacitance are both present during soft−start, the circuit may fail to achieve regulation and continually attempts soft−start, only to have the output capacitance discharged by the load when in a FAULT state.

*Output Voltage Ripple*

Output voltage ripple is inversely proportional to $C_{OUT}$. During $t_{ON}$, when the boost switch is on, all load current is supplied by $C_{OUT}$. Output ripple is calculated as:

$$V_{RIPPLE(P-P)} = t_{ON} * \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 3)}$$

and

$$t_{ON} = t_{SW} * D = t_{SW} * \left(1 - \frac{V_{IN}}{V_{OUT}}\right) \quad \text{(eq. 4)}$$

therefore:

$$V_{RIPPLE(P-P)} = t_{SW} * \left(1 - \frac{V_{IN}}{V_{OUT}}\right) * \frac{I_{LOAD}}{C_{OUT}} \quad \text{(eq. 5)}$$

and

$$t_{SW} = \frac{1}{f_{SW}} \quad \text{(eq. 6)}$$

### Layout Recommendations

The layout recommendations below highlight various top−copper pours using different colors.

To minimize spikes at $V_{OUT}$, $C_{OUT}$ must be placed as close as possible to PGND and VOUT, as shown in Figure 22.

For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal vias.

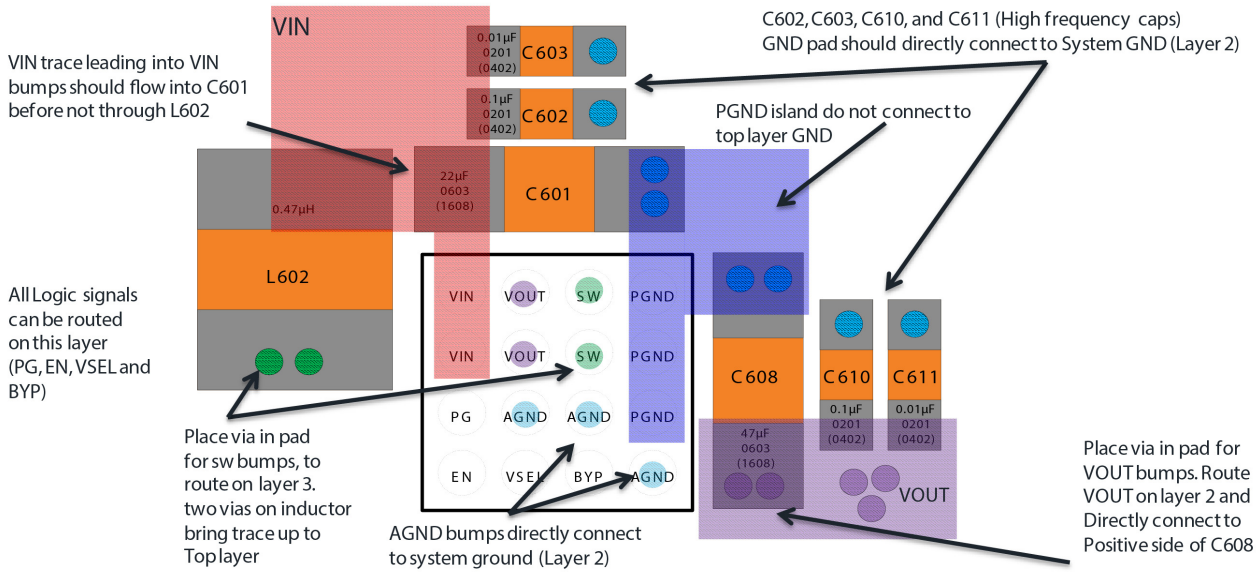


**Figure 22. Top Layer**

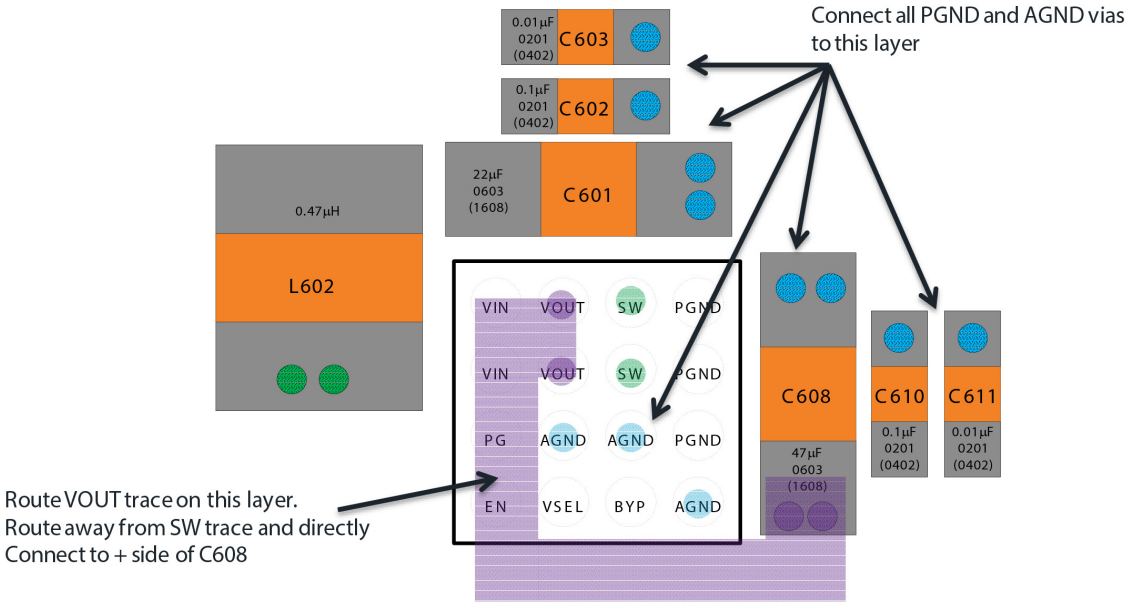


**Figure 23. Layer 2**

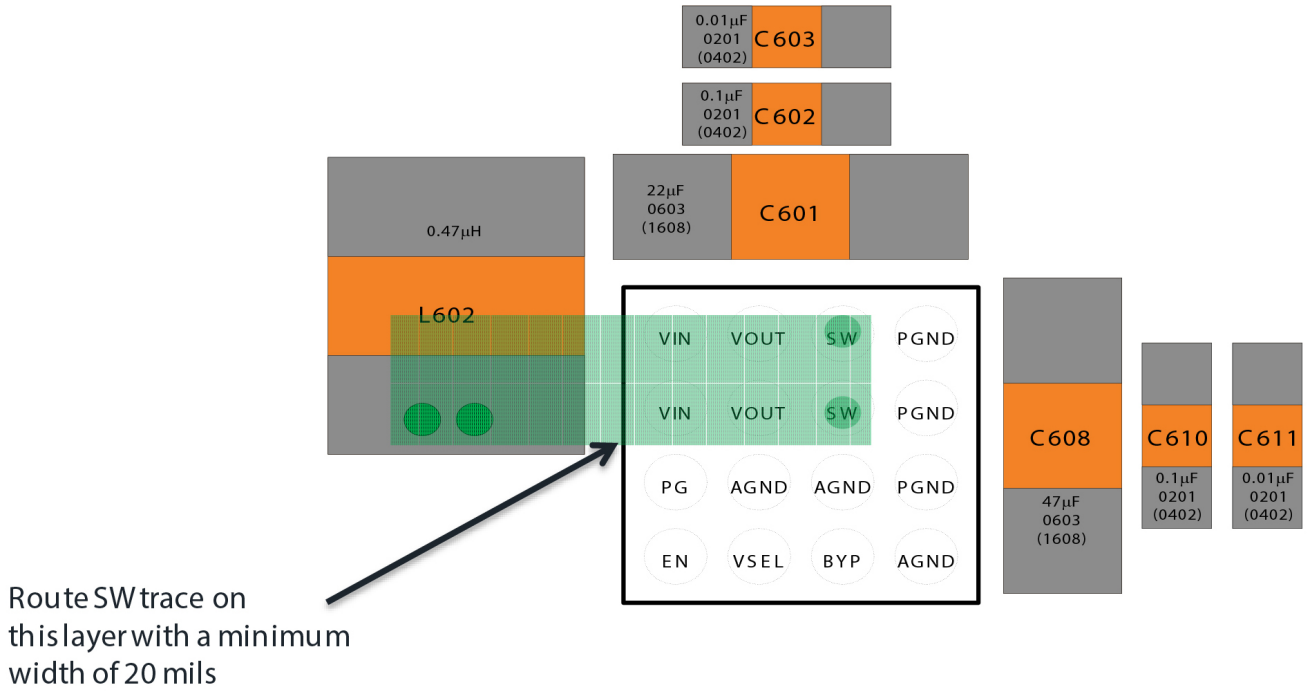


**Figure 24. Layer 3**

**Table 12. PRODUCT−SPECIFIC DIMENSIONS**

| Product | D | E | X | Y |
|---|---|---|---|---|
| FAN48630BUC31JX | 1.780 ± 0.030 | 1.780 ± 0.030 | 0.290 | 0.290 |

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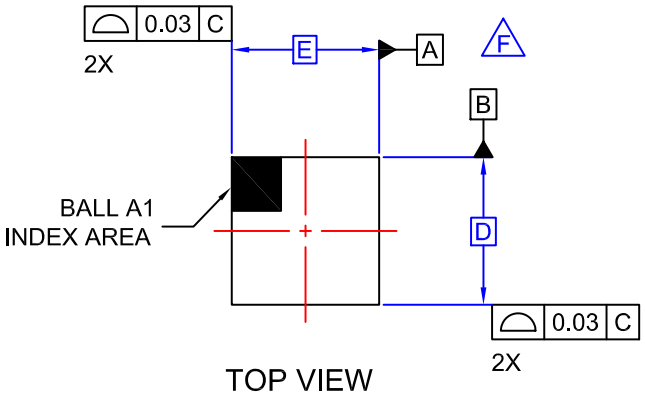
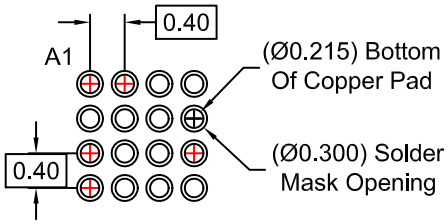
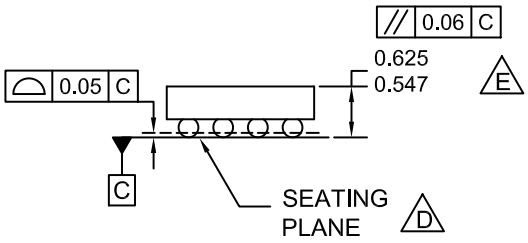
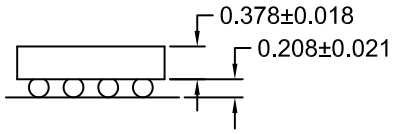



TOP VIEW

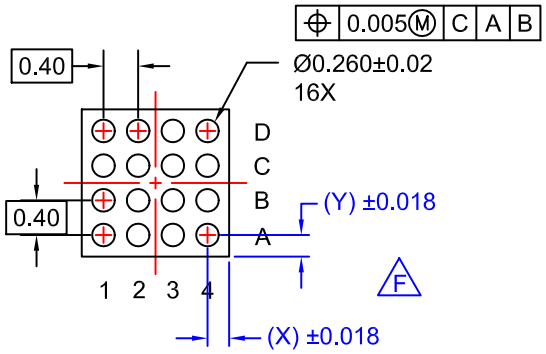



RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)




SIDE VIEWS




BOTTOM VIEW

NOTES
A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 1994.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

| | | |
|---|---|---|
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