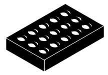
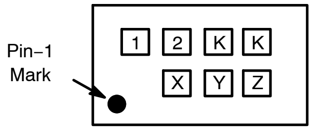
# 3.0 A, 2.4 MHz, Digitally Programmable Buck Regulator

# FAN53528



WLCSP−15
CASE 567QS

## MARKING DIAGRAM



1, 2 = Two Alphanumeric Characters for Device Mark
KK = Two Alphanumeric Characters for Lot Rune Code Mark
. = Pin 1 Indicator
X = Alphabetical Year Code
Y = 2−weeks Date Code
Z = Assembly Plant Code

## ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

### Descriptions

The FAN53528 is a step−down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5 V to 5.5 V. The output voltage is programmed through an $I^2C$ interface capable of operating up to 3.4 MHz.

Using a proprietary architecture with synchronous rectification, the FAN53528 is capable of delivering 3.0 A continuous at over 80% efficiency, maintaining that efficiency at load currents as low as 10 mA. The regulator operates at a nominal fixed frequency of 2.4 MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light−loads, Pulse Frequency Modulation (PFM) is used to operate in Power−Save Mode with a typical quiescent current of 50 mA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed−frequency control, operating at 2.4 MHz. In Shutdown Mode, the supply current drops below 1 mA, reducing power consumption. PFM Mode can be disabled if fixed frequency is desired. The FAN53528 is available in a 15−bump, 1.310 mm × 2.015 mm, 0.4 mm ball pitch WLCSP.

### Features

- Fixed−Frequency Operation: 2.4 MHz
- Best−in−Class Load Transient
- Continuous Output Current Capability: 3.0 A
- 2.5 V to 5.5 V Input Voltage Range
- Digitally Programmable Output Voltage:
    - 0.35 V to 1.14375 V in 6.25 mV Steps
- Programmable Slew Rate for Voltage Transitions
- $I^2C$−Compatible Interface Up to 3.4 Mbps
- PFM Mode for High Efficiency in Light-Load
- Quiescent Current in PFM Mode: 50 µA (Typical)
- Input Under−Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- 15−Bump Wafer−Level Chip Scale Package (WLCSP)

### Applications

- Application, Graphic, and DSP Processors
    - ARM™, Tegra™, OMAP™, NovaThor™, ARMADA™, Krait™, etc.
- Hard Disk Drives, LPDDR3, LPDDR4
- Tablets, Netbooks, Ultra−Mobile PCs
- Smart Phones

- Gaming Devices

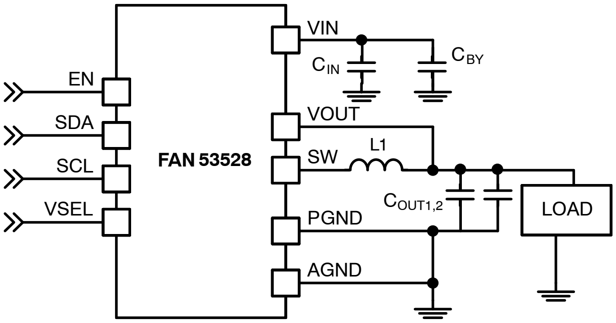


**Figure 1. Typical Application**

## PACKAGE MARKING AND ORDERING INFORMATION

| Part Number | Power−Up Defaults |  | EN Delay | Temperature Range | Package | Packing Method | Device Marking |
|---|---|---|---|---|---|---|---|
|  | VSEL0 | VSEL1 |  |  |  |  |  |
| FAN53528BUC08X | 0.4 | 0.6 | No | −40 to 85°C | WLCSP | Tape & Reel | FX |
| FAN53528DUC40X | 0.6 | 0.9 | No |  |  |  | FY |
| FAN53528GUC48X | 0.65 | 0.7 | No |  |  |  | FZ |
| FAN53528EUC48X | 0.65 | 0.7 | 5 ms |  |  |  | FW |
| *FAN53528DUC1204X | 1.1 | 0.9 | [illegible] |  |  |  | TBD |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*This device is not released yet.

## RECOMMENDED EXTERNAL COMPONENTS

### Table 1. RECOMMENDED EXTERNAL COMPONENTS FOR 3.0 A MAXIMUM LOAD CURRENT

| Component | Description | Vendor | Parameter | Typ. | Unit |
|---|---|---|---|---|---|
| L1 | 330 nH, 2016 Case Size | See Table 2 |  |  |  |
| L1 Alternative (Note 1) | 470 nH 2016 Case Size |  |  |  |  |
| $C_{OUT1}$, $C_{OUT2}$ | 22 μF, 6.3 V, X5R, 0603 | C1608X5R0J226M080AC (TDK) | C | 22 | μF |
| $C_{IN}$ | 1 Piece; 4.7 μF, 10 V, X5R, 0603 | C1608X5R1A475K (TDK) | C | 4.7 |  |
| $C_{BY}$ (Note 1) | 1 Piece; 100 nF, 6.3V, X5R, 0201 | GRM033R60J104KE19D (Murata) | C | 100 | nF |

1. L1 Alternative can be used if not following reference design. $C_{BY}$ is recommended to reduce any high frequency component on VIN bus. $C_{BY}$ is optional and used to filter any high frequency component on VIN bus.

### Table 2. RECOMMENDED INDUCTORS

| Manufacturer | Part # | L (nH) | DCR (mΩ Typ.) | $I_{SAT}$ (Note 2) | Component Dimensions |  |  |
|---|---|---|---|---|---|---|---|
|  |  |  |  |  | L | W | H |
| Toko | DFE201610E−R33N | 330 | 21 | 6.1 | 2.0 | 1.6 | 1.0 |
| Toko | DFE201610E−R47N | 470 | 26 | 5.3 | 2.0 | 1.6 | 1.0 |

2. $I_{SAT}$ where the dc current drops the inductance by 30%.

## PIN CONFIGURATION

Top View Bottom View

**Figure 2. Pin Configuration**

**Table 3. PIN DEFINITIONS**

| Pin # | Name | Description |
|---|---|---|
| D1 | VSEL | **Voltage Select.** When this pin is LOW, $V_{OUT}$ is set by the VSEL0 register. When this pin is HIGH, $V_{OUT}$ is set by the VSEL1 register. The polarity of pin in conjunction with the MODE bits in the Control register 02h, will select Forced PWM or Auto PFM/PWM mode of operation. VSEL0 = Auto PFM, and VSEL1 = FPWM. The VSEL pin has an internal pull−down resistor (250 kW), which is only activated with a logic low. |
| D2 | EN | **Enable.** The device is in Shutdown Mode when this pin is LOW. Device keeps register content when EN pin is LOW. The EN Pin has an internal pull−down resistor (250 kW), which is only activated with a logic low. |
| E2 | SCL | **$I^2C$ Serial Clock** |
| D3 | SDA | **$I^2C$ Serial Data** |
| E3 | VOUT | **VOUT.** Sense pin for $V_{OUT}$. Connect to $C_{OUT}$. |
| A3, B3, C2 | PGND | **Power Ground.** The low−side MOSFET is referenced to this pin. $C_{IN}$ and $C_{OUT}$ should be returned with a minimal path to these pins. |
| C3, E1 | AGND | **Analog Ground.** All signals are referenced to this pin. Avoid routing high di/dt AC currents through this pin. |
| A1, B1, C1 | VIN | **Power Input Voltage.** Connect to the input power source. Connect to $C_{IN}$ with minimal path. |
| A2, B2 | SW | **Switching Node.** Connect to the inductor. |

### Table 4. ABSOLUTE MAXIMUM RATINGS

| Symbol | Parameter | Parameter | Min | Max | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Voltage on SW, VIN Pins | IC Not Switching | −0.3 | 7.0 | V |
| | | IC Switching | −0.3 | 6.5 | |
| | Voltage on EN Pin | | −0.3 | VIN<br>(Note 3) | |
| | Voltage on All Other Pins | IC Not Switching | −0.3 | VIN<br>(Note 3) | |
| $V_{OUT}$ | Voltage on VOUT Pin | | −0.3 | 6.5 | V |
| $V_{INOV\_SLEW}$ | Maximum Slew Rate of $V_{IN}$ > 6.5V, PWM Switching | | | 100 | V/ms |
| ESD | Human Body Model, ANSI/ESDA/JEDEC JS−001−2012 | | 2000 | | V |
| | Charged Device Model per JESD22−C101 | | 1000 | | |
| $T_J$ | Junction Temperature | | −40 | +150 | °C |
| $T_{STG}$ | Storage Temperature | | −65 | +150 | °C |
| $T_L$ | Lead Soldering Temperature, 10 Seconds | | | +260 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. Lesser of 7V or $V_{IN}$ + 0.3 V.

### Table 5. RECOMMENDED OPERATING CONDITIONS

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $V_{IN}$ | Supply Voltage Range | 2.5 | | 5.5 | V |
| $I_{OUT}$ | Output Current | 0 | | 3.0 | A |
| $T_A$ | Operating Ambient Temperature | −40 | | +85 | °C |
| $T_J$ | Operating Junction Temperature | −40 | | +125 | °C |

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

### Table 6. THERMAL PROPERTIES

| Symbol | Parameter | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|
| $\theta_{JA}$ | Junction−to−Ambient Thermal Resistance (Note 4) | | 42 | | °C/W |

4. Junction−to−ambient thermal resistance is a function of application and board layout. This data is simulated with four−layer 2s2p boards with vias in accordance to JESD51− JEDEC standard. Special attention must be paid not to exceed the junction temperature

**Table 7. ELECTRICAL CHARACTERISTICS**

Minimum and maximum values are at $V_{IN}$ = 3.6 V, $T_A$ = −40°C to +85°C, unless otherwise noted.
Typical values are at $T_A$ = 25°C, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.4 V and EN = 1.8 V.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| **POWER SUPPLIES** | | | | | | |
| $I_Q$ | Quiescent Current | $I_{LOAD}$ = 0 | | 50 | | μA |
| $I_{SD}$ | H/W Shutdown Supply Current | EN = GND | | 0.1 | 3.0 | μA |
| | S/W Shutdown Supply Current | EN = 1.8 V, BUCK_ENx = 0,<br>2.5 V ≤ $V_{IN}$ ≤ 5.5 V | | 2 | 12 | μA |
| $V_{UVLO}$ | Under−Voltage Lockout Threshold | $V_{IN}$ Rising | | 2.32 | 2.45 | V |
| $V_{UVHYST}$ | Under−Voltage Lockout Hysteresis | | | 350 | | mV |
| **EN, VSEL, SDA, SCL** | | | | | | |
| $V_{IH}$ | HIGH−Level Input Voltage | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | 1.1 | | | V |
| $V_{IL}$ | LOW−Level Input Voltage | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V | | | 0.4 | V |
| $I_{IN}$ | Input Bias Current | Input Tied to GND or VIN | | 0.01 | 1.00 | μA |
| **$V_{OUT}$ REGULATION** | | | | | | |
| $V_{REG}$ | $V_{OUT}$ DC Accuracy | 2.8 V ≤ $V_{IN}$ ≤ 4.8 V, $V_{OUT}$ = 0.4 V<br>$I_{OUT(DC)}$ = 0 A, Auto Mode | −3 | | +5 | % |
| | | 2.8 V ≤ $V_{IN}$ ≤ 4.8 V, $V_{OUT}$ = 0.4 V,<br>$I_{OUT(DC)}$ = 0 A, Forced PWM Mode | −1.5 | | +1.5 | |
| | | 2.8 V ≤ $V_{IN}$ ≤ 4.8 V, $V_{OUT}$ from Minimum to Maximum,<br>$I_{OUT(DC)}$ = 0 to 3.0 A, Auto Mode | −4 | | +6 | |
| **POWER SWITCH/PROTECTION** | | | | | | |
| $I_{LIMPK}$ | P−MOS Peak Current Limit | | 4.00 | 4.75 | 5.50 | A |
| $T_{LIMIT}$ | Thermal Shutdown | | | 150 | | °C |
| $T_{HYST}$ | Thermal Shutdown Hysteresis | | | 17 | | °C |
| $V_{SDWN}$ | Input OVP Shutdown | Rising Threshold | | 6.15 | | V |
| | | Falling Threshold | 5.50 | 5.73 | | |
| **FREQUENCY CONTROL** | | | | | | |
| $f_{SW}$ | Oscillator Frequency | | 2.05 | 2.40 | 2.75 | MHz |
| **DAC** | | | | | | |
| | Resolution | | | 7 | | Bits |
| | Differential Nonlinearity (Note 5) | | | | 0.5 | LSB |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

5. Monotonicity assured by design.

### Table 8. SYSTEM CHARACTERISTICS

The following system characteristics are guaranteed by design and are not performed in production testing. Recommended operating conditions, unless otherwise noted, $V_{IN}$ =2.5 V to 5.5 V, $T_A$ = −40°C to +85°C, $V_{OUT}$ =0.4 V.
Typical values are given at $T_A$ = 25°C, $V_{IN}$ =3.6 V. System characteristics are based on circuit per Figure 1.
L = 0.33 mH, DFE201610E−R33M (TOKO), $C_{IN}$ = 1 × 4.7 μF, 10 V, 0603 (1608 metric), C1608X5R1A475K (TDK) and $C_{OUT}$ = 2 × 22 μF (6.3 V, 0603, TDK C1608X5R0J226M080AC) + 4 × 100 μF (6.3 V, 0201, Murata GRM033R60J104KE19D) + 1 × 4.7 μF (6.3 V, 0402, TDK C1005X5R0J475M050BC).

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $LOAD_{REG}$ | Load Regulation | $I_{OUT}$ = 0 A to 3 A, Forced PWM Mode | | 0.05 | | %/A |
| $LINE_{REG}$ | Line Regulation | 2.5 V ≤ $V_{IN}$ ≤ 5.5 V, $I_{OUT}$ =1.5 A | | 0.09 | | %/V |
| $V_{OUT\_RIPPLE}$ | Ripple Voltage | $I_{OUT}$ = 20 mA, PFM Mode | | 16 | | mV |
| | | $I_{OUT}$ = 700 mA, PFM Mode | | 5 | | |
| $\Delta V_{OUT\_LOAD}$ | Load Transient | $I_{OUT}$ = 10 mA ⇔ 700 mA,<br>$t_R = t_F$ = 200 ns, $V_{OUT}$ = 0.4 V, Auto Mode | | ±20 | | mV |
| | | $I_{OUT}$ = 0 mA ⇔ 800 mA,<br>$t_R = t_F$ = 0.9 μs, $V_{IN}$ = 3.2 V, $V_{OUT}$ = 1.125 V,<br>Auto Mode | | ±13 | | |
| | | $I_{OUT}$ = 0 mA ⇔ 800 mA,<br>$t_R = t_F$ = 0.9 μs, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 1.125 V,<br>Auto Mode | | ±15 | | |
| $\Delta V_{OUT\_LINE}$ | Line Transient | $V_{IN}$ = 3.0 V ⇔ 3.6 V,<br>$t_R = t_F$ = 10 μs, $I_{OUT}$ = 100 mA, Forced PWM Mode | | ±11 | | mV |
| $t_{ss}$ | Soft−Start | EN High to 95% of Target_$V_{OUT}$ (0.4 V),<br>$I_{OUT}$ = 200 mA; FAN53528BUC08X | | 85 | | μs |
| $t_{delay}$ | EN Delay | EN High to $V_{OUT}$ Start−to−Rise,<br>$V_{OUT}$ = 0.6 V, $I_{OUT}$ = 0 A; FAN53528EUC48X | | 5 | | ms |

### Table 9. I$^2$C TIMING SPECIFICATIONS

Guaranteed by design.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $f_{SCL}$ | SCL Clock Frequency | Standard Mode | | | 100 | kHz |
| | | Fast Mode | | | 400 | kHz |
| | | Fast Mode Plus | | | 1000 | |
| | | High−Speed Mode, $C_B$ ≤ 100 pF | | | 3400 | |
| | | High−Speed Mode, $C_B$ ≤ 400 pF | | | 1700 | |
| $t_{BUF}$ | Bus−Free Time between STOP and START Conditions | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| | | Fast Mode Plus | | 0.5 | | |
| $t_{HD;STA}$ | START or REPEATED START Hold Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 260 | | |
| | | High−Speed Mode | | 160 | | |
| $t_{LOW}$ | SCL LOW Period | Standard Mode | | 4.7 | | μs |
| | | Fast Mode | | 1.3 | | |
| | | Fast Mode Plus | | 0.5 | | |
| | | High−Speed Mode, $C_B$ ≤ 100 pF | | 160 | | ns |
| | | High−Speed Mode, $C_B$ ≤ 400 pF | | 320 | | |

**Table 9. I$^2$C TIMING SPECIFICATIONS** (continued)
Guaranteed by design.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{HIGH}$ | SCL HIGH Period | Standard Mode | | 4 | | µs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 260 | | |
| | | High−Speed Mode, $C_B \le 100$ pF | | 60 | | |
| | | High−Speed Mode, $C_B \le 400$ pF | | 120 | | |
| $t_{SU;STA}$ | Repeated START Setup Time | Standard Mode | | 4.7 | | µs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 260 | | |
| | | High−Speed Mode | | 160 | | |
| $t_{SU;DAT}$ | Data Setup Time | Standard Mode | | 250 | | ns |
| | | Fast Mode | | 100 | | |
| | | Fast Mode Plus | | 50 | | |
| | | High−Speed Mode | | 10 | | |
| $t_{HD;DAT}$ | Data Hold Time | Standard Mode | 0 | | 3.45 | µs |
| | | Fast Mode | 0 | | 900 | ns |
| | | Fast Mode Plus | 0 | | 450 | |
| | | High−Speed Mode, $C_B \le 100$ pF | 0 | | 70 | |
| | | High−Speed Mode, $C_B \le 400$ pF | 0 | | 150 | |
| $t_{RCL}$ | SCL Rise Time | Standard Mode | $20+0.1C_B$ | | 1000 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High−Speed Mode, $C_B \le 100$ pF | | 10 | 80 | |
| | | High−Speed Mode, $C_B \le 400$ pF | | 20 | 160 | |
| $t_{FCL}$ | SCL Fall Time | Standard Mode | $20+0.1C_B$ | | 300 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High−Speed Mode, $C_B \le 100$ pF | | 10 | 40 | |
| | | High−Speed Mode, $C_B \le 400$ pF | | 20 | 80 | |
| $t_{RCL1}$ | Rise Time of SCL After a REPEATED START Condition and After ACK Bit | High−Speed Mode, $C_B \le 100$ pF | | 10 | 80 | ns |
| | | High−Speed Mode, $C_B \le 400$ pF | | 20 | 160 | |
| $t_{RDA}$ | SDA Rise Time | Standard Mode | $20+0.1C_B$ | | 1000 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High−Speed Mode, $C_B \le 100$ pF | | 10 | 80 | |
| | | High−Speed Mode, $C_B \le 400$ pF | | 20 | 160 | |

**Table 9. I²C TIMING SPECIFICATIONS** (continued)
Guaranteed by design.

| Symbol | Parameter | Condition | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_{FDA}$ | SDA Fall Time | Standard Mode | $20+0.1C_B$ | | 300 | ns |
| | | Fast Mode | $20+0.1C_B$ | | 300 | |
| | | Fast Mode Plus | $20+0.1C_B$ | | 120 | |
| | | High−Speed Mode, $C_B \le 100$ pF | | 10 | 80 | |
| | | High−Speed Mode, $C_B \le 400$ pF | | 20 | 160 | |
| $t_{SU;STO}$ | Stop Condition Setup Time | Standard Mode | | 4 | | μs |
| | | Fast Mode | | 600 | | ns |
| | | Fast Mode Plus | | 120 | | |
| | | High−Speed Mode | | 160 | | |
| $C_B$ | Capacitive Load for SDA and SCL | | | | 400 | pF |

## TIMING DIAGRAMS

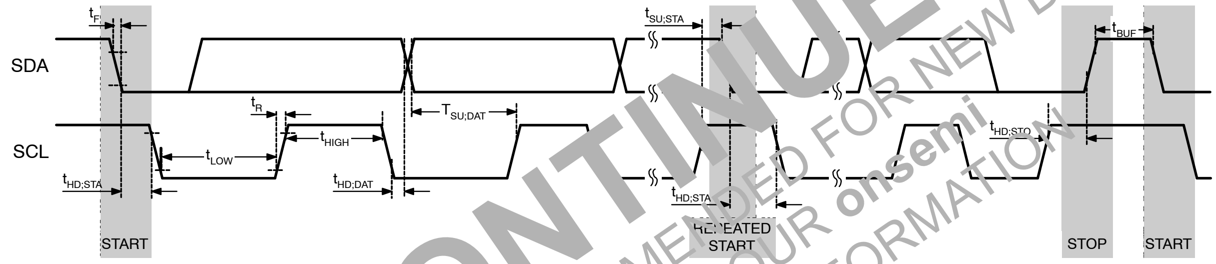
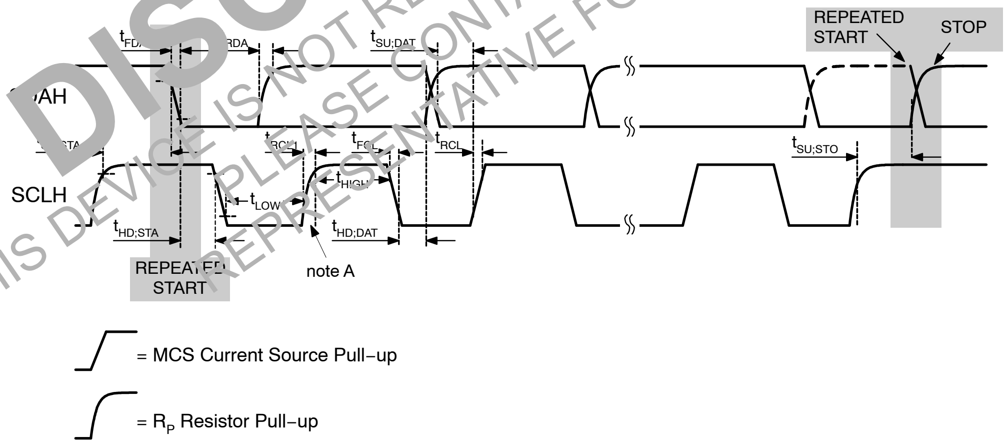


**Figure 3. I²C Interface Timing for Fast Plus, Fast, and Slow Modes**



Note A: First rising edge of SCLH after Repeated Start and after each ACK bit.

**Figure 4. I²C Interface Timing for High−Speed Mode**

## TYPICAL CHARACTERISTICS

UNLESS OTHERWISE SPECIFIED, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.4 V, AUTO MODE, $T_A$ = 25°C; CIRCUIT AND COMPONENTS ACCORDING TO FIGURE 1 AND TABLE 1.

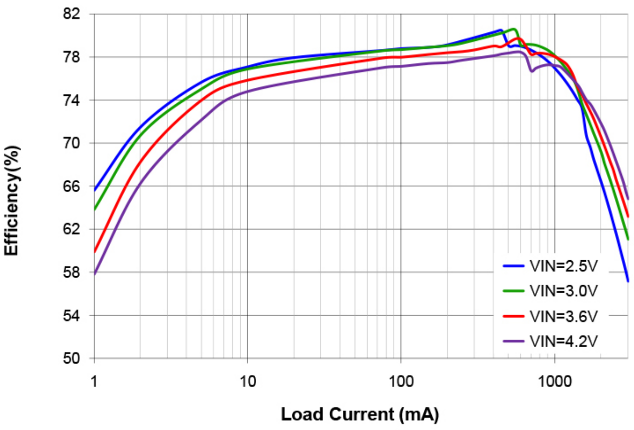


Figure 5. Efficiency vs. Load Current and Input Voltage, $V_{OUT}$ = 0,4 V, Auto Mode

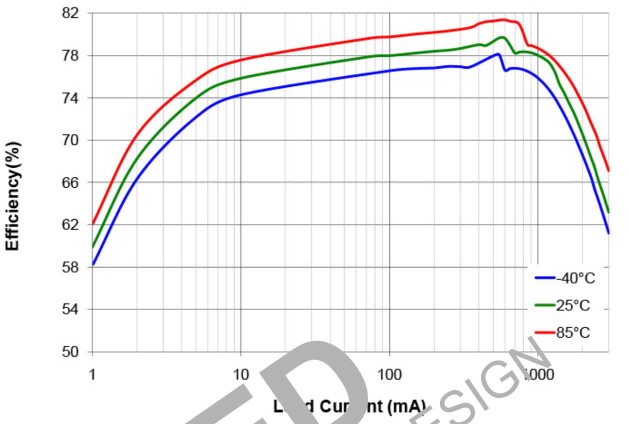


Figure 6. Efficiency vs. Load Current and Temperature, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.4 V, Auto Mode

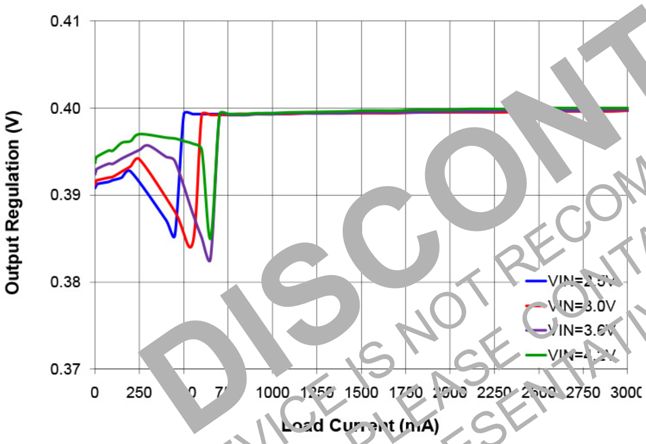


Figure 7. Output Regulation vs. Load Current and Input Voltage, $V_{OUT}$ = 0.4 V, Auto Mode

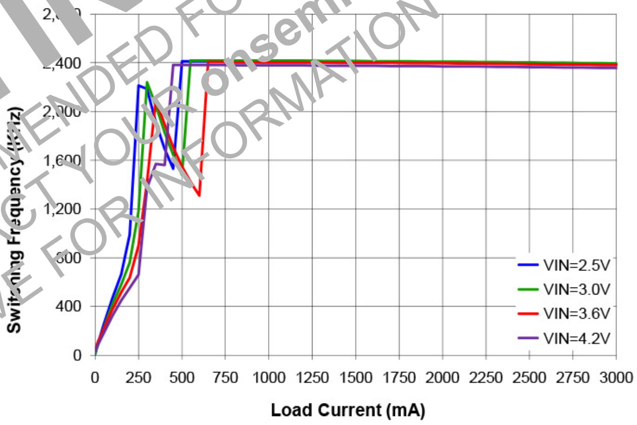


Figure 8. Frequency vs. Load Current and Input Voltage, $V_{OUT}$ = 0.65 V, Auto Mode

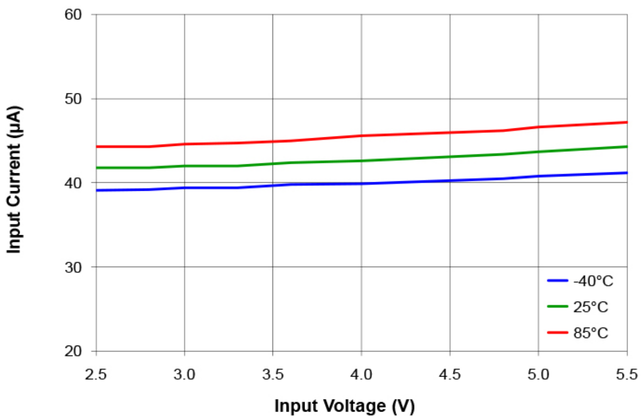


Figure 9. Quiescent Current vs. Input Voltage and Temperature $V_{OUT}$ = 0.4 V, Auto Mode

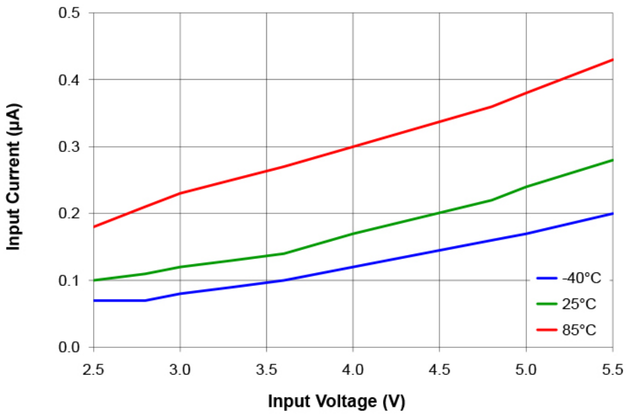


Figure 10. Shutdown Current vs. Input Voltage and Temperature

## TYPICAL CHARACTERISTICS (continued)

UNLESS OTHERWISE SPECIFIED, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.4 V, AUTO MODE, $T_A$ = 25°C; CIRCUIT AND COMPONENTS ACCORDING TO FIGURE 1 AND TABLE 1.

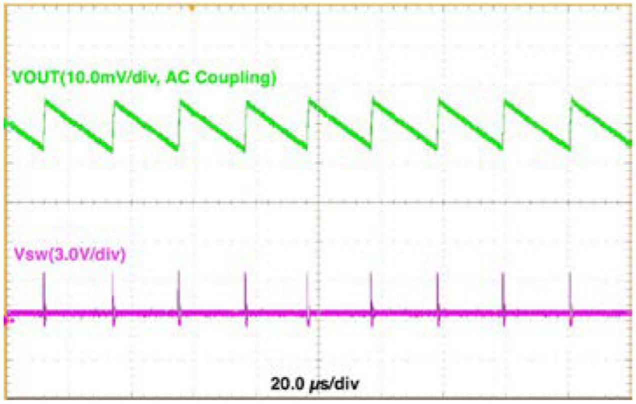


Figure 11. Output Ripple, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.65 V, 20 mA Load

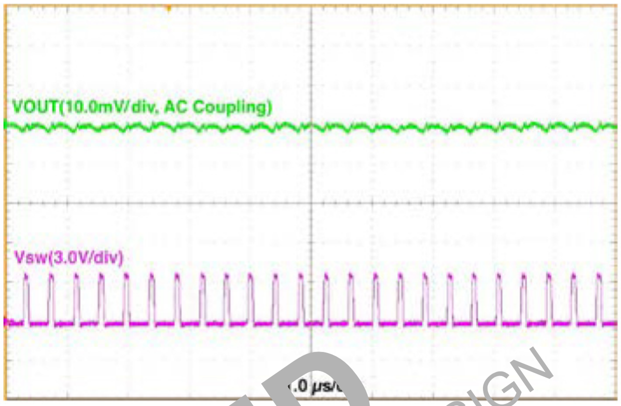


Figure 12. Output Ripple, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.65 V, 770 mA Load

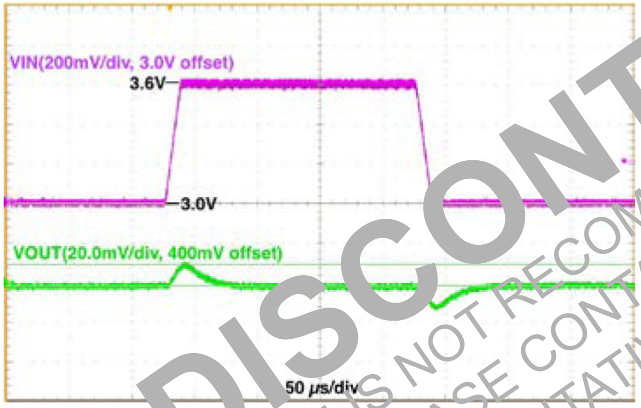


Figure 13. Line Transient, $V_{IN}$ = 3.0 V ⇔ 3.6 V, $V_{OUT}$ = 0.4 V, 10 µs Edge, 100 mA Load, Forced PWM Mode

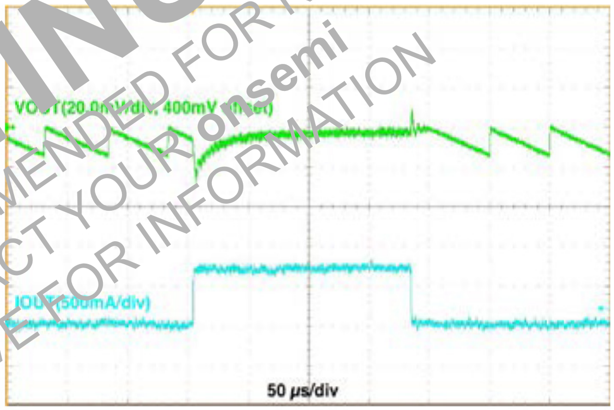


Figure 14. Load Transient, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.4 V, 10 mA ⇔ 700 mA, 200 ns Edge, Auto Mode

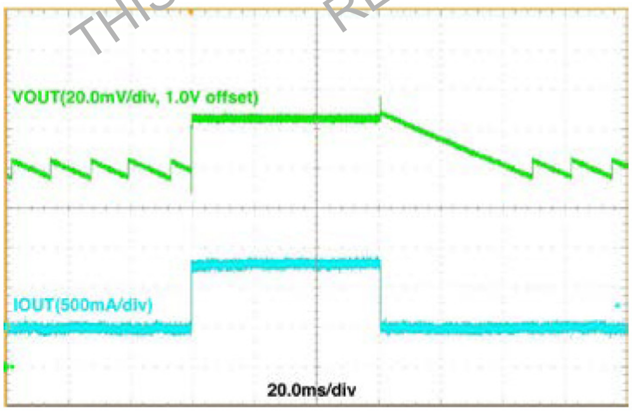


Figure 15. Load Transient, $V_{IN}$ = 3.2 V, $V_{OUT}$ = 1.125 V, 0 mA ⇔ 800 mA, 900 ns Edge, Auto Mode

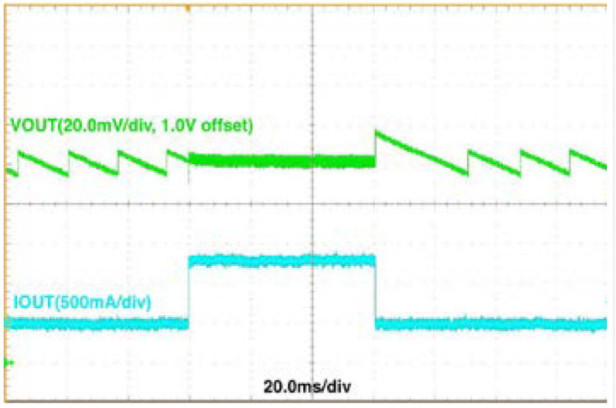


Figure 16. Load Transient, $V_{IN}$ = 3.8 V, $V_{OUT}$ = 1.125 V, 0 mA ⇔ 800 mA, 900 ns Edge, Auto Mode

## TYPICAL CHARACTERISTICS (continued)

UNLESS OTHERWISE SPECIFIED, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.4 V, AUTO MODE, $T_A$ = 25°C; CIRCUIT AND COMPONENTS ACCORDING TO FIGURE 1 AND TABLE 1.

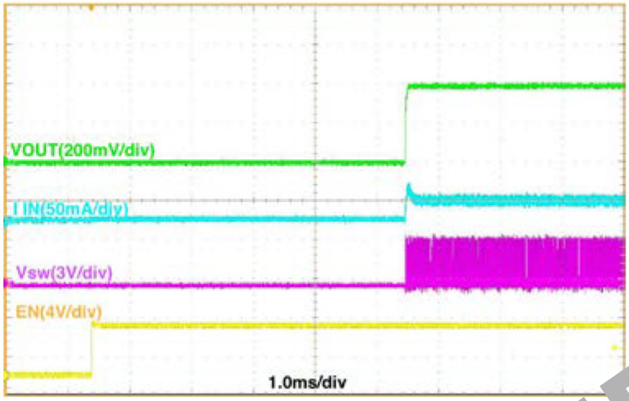


**Figure 17. Startup, $V_{IN}$ = 3.6 V, $V_{OUT}$ = 0.65 V, 200 mA Load, with 5 ms EN Delay, Auto Mode**

## OPERATING DESCRIPTION

The FAN53528 is a step−down switching voltage regulator that delivers a programmable output voltage from an input voltage supply of 2.5 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53528 is capable of delivering 3.0 A at over 80% efficiency. The regulator operates at a nominal frequency of 2.4 MHz at full load, which reduces the value of the external components to 330 nH or 470 nH for the output inductor and 44 μF for the output capacitor. High efficiency is maintained at light load with single−pulse PFM.

An $I^2C$−compatible interface allows transfers up to 3.4 Mbps. This communication interface can be used to:

- Dynamically reprogram the output voltage in 6.25 mV increments;
- Reprogram the mode to enable or disable PFM;
- Control voltage transition slew rate; or
- Enable/disable the regulator.

### Control Scheme

The FAN53528 uses a proprietary non−linear, fixed−frequency PWM modulator to deliver a fast load transient response, while maintaining a constant switching frequency over a wide range of operating conditions. The regulator performance is independent of the output capacitor ESR, allowing for the use of ceramic output capacitors. Although this type of operation normally results in a switching frequency that varies with input voltage and load current, an internal frequency loop holds the switching frequency constant over a large range of input voltages and load currents.

For very light loads, the FAN53528 operates in Discontinuous Current Mode (DCM) single−pulse PFM, which produces low output ripple compared with other PFM architectures. Transition between PWM and PFM is relatively seamless, providing a smooth transition between DCM and CCM Modes.

PFM can be disabled by programming the MODE bits in the CONTROL register in combination with the state of the VSEL pin. See table in the Control Register 02h.

### Enable and Soft−Start

When the EN pin is LOW; the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, $I^2C$ can be written to or read from as long as input voltage is above the UVLO. The registers keep the content when the EN pin is LOW. The registers are reset to default values during a Power On Reset (POR). When the OUTPUT_DISCHARGE bit in the Control register is enabled (logic HIGH) and the EN pin is LOW or the BUCK_ENx bit is LOW, an 11 Ω load is connected from VOUT to GND to discharge the output capacitors.

Raising EN while the BUCK_ENx bit is HIGH activates the part and begins the soft−start cycle. For option EUC48X, there is 5 ms delay time from EN HIGH to $V_{OUT}$ start soft−start. And for options FAN53528BUC08X, FAN53528GUC48X and FAN53528DUC40X, there is no EN Delay. During soft−start, the modulator's internal reference is ramped slowly to minimize surge currents on the input and prevent overshoot of the output voltage. Synchronous rectification is inhibited, allowing the IC to start into a pre−charged capacitive load.

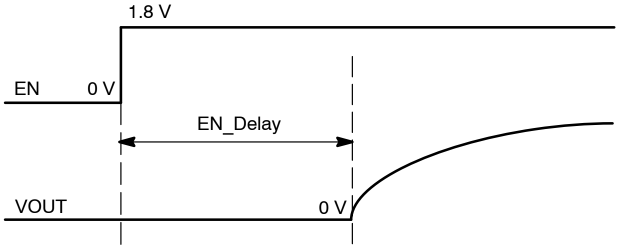


Figure 18. EN Delay

If large values of output capacitance are used, the regulator may fail to start. The maximum $C_{OUT}$ capacitance for starting with a heavy constant−current load is approximately:

$$C_{OUTMAX} \approx (I_{LMPK} - I_{LOAD}) \times \frac{320\mu}{V_{OUT}} \qquad \text{(eq. 1)}$$

where $C_{OUTMAX}$ is expressed in μF and $I_{LOAD}$ is the load current during soft−start, expressed in A.

If the regulator is at its current limit for 16 consecutive current limit cycles, the regulator shuts down and enters tri−state before reattempting soft−start 1700 μs later. This limits the duty cycle of full output current during soft−start to prevent excessive heating.

The IC allows for software enable of the regulator, when EN is HIGH, through the BUCK_EN bits. BUCK_EN0 and BUCK_EN1 are both initialized HIGH. These options reset after a POR, regardless of the state of the VSEL pin.

Table 10. HARDWARE AND SOFTWARE ENABLE

| Pins | | BITS | | | |
|---|---|---|---|---|---|
| EN | VSEL | BUCK_EN0 | BUCK_EN1 | Output | Mode |
| 0 | X | X | X | OFF | Shutdown |
| 1 | 0 | 0 | X | OFF | Shutdown |
| 1 | 0 | 1 | X | ON | Auto |
| 1 | 1 | X | 0 | OFF | Shutdown |
| 1 | 1 | X | 1 | ON | FPWM |

### VSEL Pin and I²C Programming Output Voltage

The output voltage is set by the NSELx control bits in VSEL0 and VSEL1 registers. The output is given as:

$$V_{OUT} = 0.35\ \text{V} + \text{NSELx} \times 6.25\ \text{mV} \qquad \text{(eq. 2)}$$

For example, if NSEL =1010000 (80 decimal), then $V_{OUT}$ = 0.35 + 0.5 = 0.85 V.

Output voltage can also be controlled by toggling the VSEL pin LOW or HIGH. VSEL LOW corresponds to VSEL0 and VSEL HIGH corresponds to VSEL1. Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

### Transition Slew Rate Limiting

When transitioning from a low to high voltage, the IC can be programmed for one of eight possible slew rates using the SLEW bits in the Control register, as shown in Table 11.

Table 11. TRANSITION SLEW RATE

| Decimal | Bin | Slew Rate | |
|---|---|---|---|
| 0 | 000 | 64.00 | mV/μs |
| 1 | 001 | 32.00 | mV/μs |
| 2 | 010 | 16.00 | mV/μs |
| 3 | 011 | 8.00 | mV/μs |
| 4 | 100 | 4.00 | mV/μs |
| 5 | 101 | 2.00 | mV/μs |
| 6 | 110 | 1.00 | mV/μs |
| 7 | 111 | 0.50 | mV/μs |

Transitions from high to low voltage rely on the output load to discharge $V_{OUT}$ to the new set point. Once the high−to−low transition begins, the IC stops switching until $V_{OUT}$ has reached the new set point.

### Under−Voltage Lockout (UVLO)

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage rises HIGH enough to properly operate. This ensures proper operation of the regulator during startup or shutdown.

### Input Over−Voltage Protection (OVP)

When $V_{IN}$ exceeds $V_{SDWN}$ (~ 6.2 V), the IC stops switching to protect the circuitry from internal spikes above 6.5 V. An internal filter prevents the circuit from shutting down due to noise spikes.

### Current Limiting

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. 16 consecutive current limit cycles in current limit, cause the regulator to shut down and stay off for about 1700 μs before attempting a restart.

### Thermal Shutdown

When the die temperature increases, due to a high load condition and/or high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 17°C hysteresis.

### Monitor Register (Reg05)

The Monitor register indicates of the regulation state of the IC. If the IC is enabled and is regulating, its value is (1000 0001).

### I²C Interface

The serial interface is compatible with Standard, Fast, Fast Plus, and HS Mode I²C Bus® specifications. The SCL line is an input and its SDA line is a bi−directional open−drain output; it can only pull down the bus when active. The SDA line only pulls LOW during data reads and when signaling ACK. All data is shifted in MSB (bit 7) first.

### I²C Slave Address

In hex notation, the slave address assumes a 0 LS Bit. The hex slave address is A0 for FAN53528BUCxxX and A4 for FAN53528DUCxxX, FAN53528EUCxxX, and FAN53528GUCxxX.

**Table 12. I²C SLAVE ADDRESS**

| Option | Hex | Bits | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|
| | | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| BUCxx | A0 | 1 | 0 | 1 | 0 | 0 | 0 | 0 | R/$\overline{W}$ |
| DUCxx,<br>EUCxx,<br>GUCxx | A4 | 1 | 0 | 1 | 0 | 0 | 1 | 0 | R/$\overline{W}$ |

Other slave addresses can be assigned. Contact an **onsemi** representative.

### Bus Timing

As shown in Figure 19 data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow sufficient time for the data to set up before the next SCL rising edge.

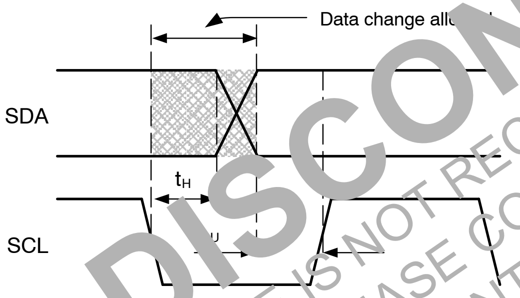


Figure 19. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 20.

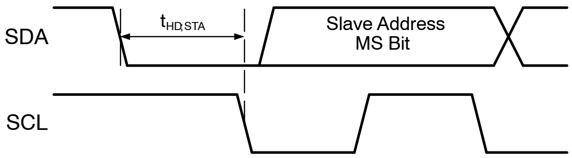


Figure 20. START Bit

A transaction ends with a STOP condition, defined as SDA transitioning from 0 to 1 with SCL high, as shown in Figure 21.

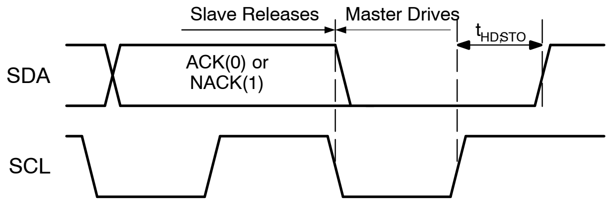


Figure 21. STOP Bit

During a read from the FAN53528, the master issues a REPEATED START after sending the register address and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 22.

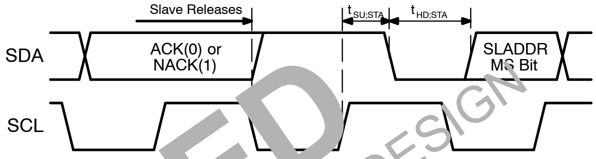


Figure 22. REPEATED START Timing

### High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical; except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition (Figure 20). The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 22) that causes all slaves on the bus to switch to HS Mode. The master then sends I²C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 21) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 22).

### Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as:

- ▨ Master Drives Bus and
- ☐ Slave Drives Bus

All addresses and data are MSB first.

**Table 13. I²C BIT DEFINITIONS FOR FIGURE 23 AND FIGURE 24**

| Symbol | Definition |
|---|---|
| S | START, see Figure 20 |
| P | STOP, see Figure 21 |
| A | ACK. The slave drives SDA to 0 to acknowledge the preceding packet. |
| $\overline{A}$ | NACK. The slave sends a 1 to NACK the preceding packet. |
| R | REPEATED START, see Figure 22 |

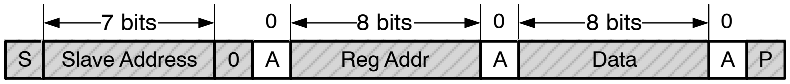


Figure 23. Write Transaction

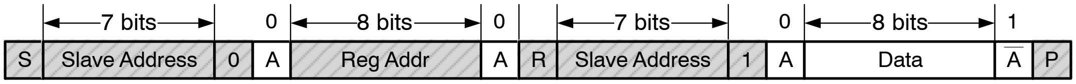


Figure 24. Write Transaction Followed by a Read Transaction

## REGISTER DESCRIPTION

### Table 14. REGISTER MAP

| Hex Address | Name | Function | Binary | Hex |
|---|---|---|---|---|
| 00 | VSEL0 | Controls $V_{OUT}$ settings when VSEL pin = LOW | 1XXXXXXX | XX |
| 01 | VSEL1 | Controls $V_{OUT}$ settings when VSEL pin = HIGH | 1XXXXXXX | XX |
| 02 | CONTROL | Determines whether $V_{OUT}$ output discharge is enabled and also the slew rate of positive transitions | 10000010 | 82 |
| 03 | ID1 | Read−only register identifies vendor and chip | 10000001 | 81 |
| 04 | ID2 | Read−only register identifies die revision | 00001000 | 08 |
| 05 | MONITOR | Indicates device status | 00000000 | 00 |

### Table 15. BIT DEFINITIONS

The following table defines the operation of each register bit. Bold indicates power−on default values.

| Bit | Name | Type | Value | Description |
|---|---|---|---|---|
| **VSEL0** | | | | **Register Address: 00** |
| 7 | BUCK_EN0 | **R/W** | **1** | Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent. |
| 6:0 | NSEL0 | **R/W** | **XXX XXXX** | Sets $V_{OUT}$ value from 0.35 to 1.14375 V (see eq. 2). |
| **VSEL1** | | | | **Register Address: 01** |
| 7 | BUCK_EN1 | **R/W** | **1** | Software buck enable. When EN pin is LOW, the regulator is off. When EN pin is HIGH, BUCK_EN bit takes precedent. |
| 6:0 | NSEL1 | **R/W** | **XXX XXXX** | Sets $V_{OUT}$ value from 0.35 to 1.14375 V (see eq. 2). |
| **CONTROL** | | | | **Register Address: 02** |
| 7 | OUTPUT_ DISCHARGE | **R/W** | 0 | When the regulator is disabled, $V_{OUT}$ is not discharged. |
| | | | **1** | When the regulator is disabled, $V_{OUT}$ discharges through an internal pull−down. |
| 6:4 | SLEW | **R/W** | **000** –111 | Sets the slew rate for positive voltage transitions (see Table 11) |
| 3 | Reserved | | **0** | Always reads back 0. |
| 2 | RESET | **R/W** | **0** | Setting to 1 resets all registers to default values. Always reads back 0. |
| 1:0 | MODE | **R/W** | **10** | In combination with the VSEL pin, these two bits set the operation of the buck to be either in Auto−PFM/PWM Mode during light load or Forced PWM mode. See table below.<br>Mode of Operation<br>**VSEL Pin Binary Operation**<br>Low X0 Auto PFM/PWM<br>Low X1 Forced PWM<br>High 0X Auto PFM/PWM<br>High 1X Forced PWM |

**Table 15. BIT DEFINITIONS** (continued)

The following table defines the operation or each register bit. Bold indicates power−on default values.

| Bit | Name | Type | Value | Description |
|---|---|---|---|---|
| **ID1** | | | | **Register Address: 03** |
| 7:5 | VENDOR | **R** | **100** | Signifies **onsemi** as the IC vendor. |
| 4 | Reserved | **R** | **0** | Always reads back 0. |
| 3:0 | DIE_ID | **R** | **0001** | DIE ID |
| **ID2** | | | | **Register Address: 04** |
| 7:4 | Reserved | **R** | **0000** | Always reads back 0000. |
| 3:0 | DIE_REV | **R** | **1000** | FAN53528 Die Revision |
| **MONITOR** | | | | **Register Address: 05** |
| 7 | PGOOD | **R** | **0** | 1: Buck is enabled and soft−start is completed. |
| 6 | UVLO | **R** | **0** | 1: Signifies the VIN is less than the UVLO threshold. |
| 5 | OVP | **R** | **0** | 1: Signifies the VIN is greater than the OVP threshold. |
| 4 | POS | **R** | **0** | 1: Signifies a positive voltage transition is in progress and the output voltage has not yet reached its new setpoint. This bit is also set during IC soft−start. |
| 3 | NEG | **R** | **0** | 1: Signifies a negative voltage transition is in progress and the output voltage has not yet reached its new setpoint. |
| 2 | RESET_STAT | **R** | **0** | 1: Indicates that a register reset was performed. This bit is cleared after register 5 is read. |
| 1 | OT | **R** | **0** | 1: Signifies the thermal shutdown is active. |
| 0 | BUCK_STATUS | **R** | **0** | 1: Buck enabled; 0: buck disabled. |

## APPLICATION INFORMATION

### Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects the average current limit, the output voltage ripple, and the efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \times \left(\frac{V_{IN} - V_{OUT}}{L \times f_{SW}}\right) \qquad \text{(eq. 3)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current such that:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \qquad \text{(eq. 4)}$$

The FAN53528 is optimized for operation with L=330 nH, but is stable with inductances up to 1.0 µH (nominal). The inductor should be rated to maintain at least 80% of its value at $I_{LIM(PK)}$. Failure to do so decreases the amount of DC current the IC can deliver.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but since ΔI increases, the RMS current increases, as do core and skin−effect losses:

$$I_{RMS} = \sqrt{{I_{OUT(DC)}}^2 + \frac{\Delta I^2}{12}} \qquad \text{(eq. 5)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs and the inductor ESR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current.

**Table 16. EFFECTS OF INDUCTOR VALUE (FROM 330 nH RECOMMENDED) ON REGULATOR PERFORMANCE**

| $I_{MAX(LOAD)}$ | $\Delta V_{OUT}$ (eq. 7) | Transient Response |
|---|---|---|
| Increase | Decrease | Degraded |

### Inductor Current Rating

The current−limit circuit can allow substantial peak currents to flow through L1 under worst−case conditions. If it is possible for the load to draw such currents, the inductor should be capable of sustaining the current or failing in a safe manner.

For space−constrained applications, a lower current rating for L1 can be used. The FAN53528 may still protect these inductors in the event of a short circuit, but may not be able to protect the inductor from failure if the load is able to draw higher currents than the DC rating of the inductor. Refer to Table 2 for the recommended inductors.

### Output Capacitor and $V_{OUT}$ Ripple

If space is at a premium, 0603 capacitors may be used.

Increasing $C_{OUT}$ has negligible effect on loop stability and can be increased to reduce output voltage ripple or to improve transient response. Output voltage ripple, $\Delta V_{OUT}$, is calculated by:

$$\Delta V_{OUT} = \Delta I_L \left[ \frac{f_{SW} \times C_{OUT} \times ESR^2}{2 \times D \times (1 - D)} + \frac{1}{8 \times f_{SW} \times C_{OUT}} \right] \qquad \text{(eq. 6)}$$

where $C_{OUT}$ is the effective output capacitance.

The capacitance of $C_{OUT}$ decreases at higher output voltages, which results in higher $\Delta V_{OUT}$. Equation 6 is only valid for CCM operation, which occurs in PWM Mode.

The FAN53528 can be used with either 2 x 22 μF (0603) or 2 x 47 μF (0603) output capacitor configuration. If a tighter ripple and transient specification is need from the FAN53528, then the 2 x 47 μF is recommended.

The lowest $\Delta V_{OUT}$ is obtained when the IC is in PWM Mode and, therefore, operating at 2.4 MHz. In PFM Mode, $f_{SW}$ is reduced, causing $\Delta V_{OUT}$ to increase.

### ESL Effects

The Equivalent Series Inductance (ESL) of the output capacitor network should be kept low to minimize the square−wave component of output ripple that results from the division ratio $C_{OUT}$ ESL and the output inductor ($L_{OUT}$). The square−wave component due to the ESL can be estimated as:

$$\Delta V_{OUT(SQ)} \approx V_{IN} \times \frac{ESL_{COUT}}{L1} \qquad \text{(eq. 7)}$$

A good practice to minimize this ripple is to use multiple output capacitors to achieve the desired $C_{OUT}$ value. For example, to obtain $C_{OUT}$ = 20 μF, a single 22 μF 0805 would produce twice the square wave ripple as two × 10 μF 0805.

To minimize ESL, try to use capacitors with the lowest ratio of length to width. 0805 s have lower ESL than 1206 s. If low output ripple is a chief concern, some vendors produce 0508 capacitors with ultra−low ESL. Placing additional small−value capacitors near the load also reduces the high−frequency ripple components.

### Input Capacitor

The ceramic input capacitors should be placed as close as possible between the VIN and PGND pins to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional "bulk" capacitance (electrolytic or tantalum) should be placed between CIN and the power source lead to reduce under−damped ringing that can occur between the inductance of the power source leads and $C_{IN}$.

The effective $C_{IN}$ capacitance value decreases as $V_{IN}$ increases due to DC bias effects. This has no significant impact on regulator performance.

### Thermal Considerations

Heat is removed from the IC through the solder bumps to the PCB copper. The junction−to−ambient thermal resistance ($\theta_{JA}$) is largely a function of the PCB layout (size, copper weight, and trace width) and the temperature rise from junction to ambient (ΔT).

For the FAN53528, $\theta_{JA}$ is 42°C/W when mounted on its four−layer with vias evaluation board in still air with 2 oz. outer layer copper weight and 1 oz. inner layer.

For long−term reliable operation, the junction temperature ($T_J$) should be maintained below 125°C.

To calculate maximum operating temperature (<125°C) for a specific application:

1. Use efficiency graphs to determine efficiency for the desired $V_{IN}$, $V_{OUT}$, and load conditions.
2. Calculate total power dissipation using:

$$P_T = V_{OUT} \times I_{LOAD} \times \left( \frac{1}{\eta} - 1 \right) \qquad \text{(eq. 8)}$$

3. Estimate inductor copper losses using:

$$P_L = I_{LOAD}{}^2 \times DCR_L \qquad \text{(eq. 9)}$$

4. Determine IC losses by removing inductor losses (step 3) from total dissipation:

$$P_{IC} = P_T - P_L \qquad \text{(eq. 10)}$$

5. Determine device operating temperature:

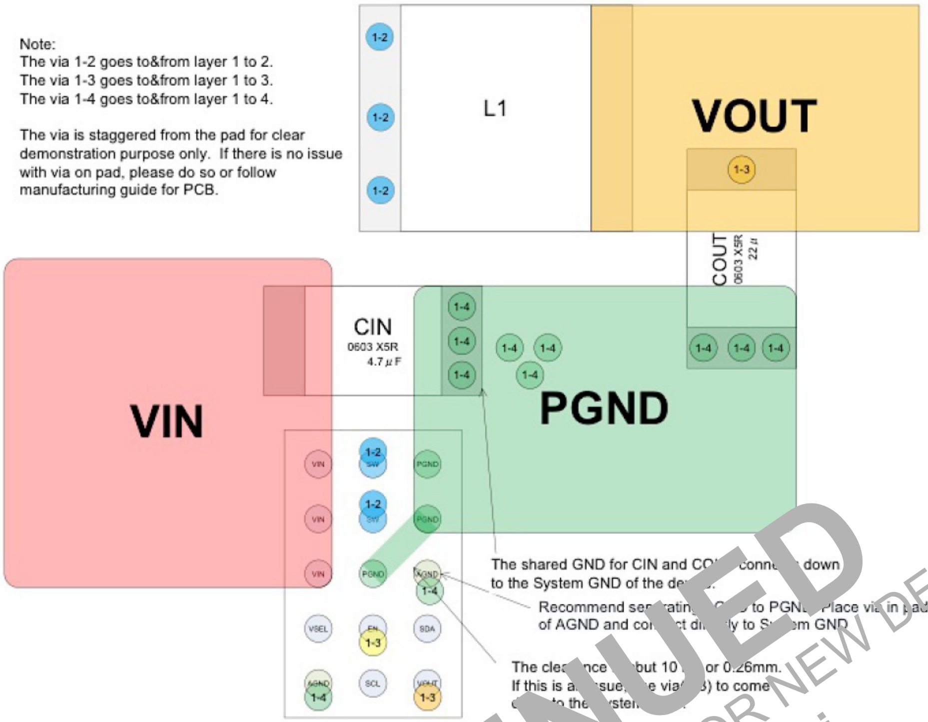
$$\Delta T = P_{IC} \times \Theta_{JA} \qquad T_{IC} = T_A + \Delta T \qquad \text{(eq. 11)}$$

and

note that the $R_{DS(ON)}$ of the power MOSFETs increases linearly with temperature at about 1.4%/°C. This causes the efficiency (η) to degrade with increasing die temperature.

### Layout Recommendations

1. The input capacitor ($C_{IN}$) should be connected as close as possible to the VIN and GND pins. Connect to VIN and GND using only top metal. Do not route through vias.
2. Place the inductor (L) as close as possible to the IC. Use short wide traces for the main current paths.
3. The output capacitor ($C_{OUT}$) should be placed as close as possible to the IC. Connection to GND should be on top metal. Feedback signal connection to VOUT should be routed away from noisy components and traces (e.g. SW line). For remote sensing application, place one or all output capacitors near the load and if there are also output capacitors placed near the inductor, the maximum trace resistance between the inductor and the load should not exceed 30 mΩ.



Note:
The via 1-2 goes to&from layer 1 to 2.
The via 1-3 goes to&from layer 1 to 3.
The via 1-4 goes to&from layer 1 to 4.

The via is staggered from the pad for clear demonstration purpose only. If there is no issue with via on pad, please do so or follow manufacturing guide for PCB.

The shared GND for CIN and COUT connects down to the System GND of the device.

Recommend separating AGND to PGND. Place via in pad of AGND and connect directly to System GND.

The clearance is about 10 mil or 0.26mm. If this is an issue, use via(1-3) to come down to the system GND.

Figure 25. Guidance for Layer 1

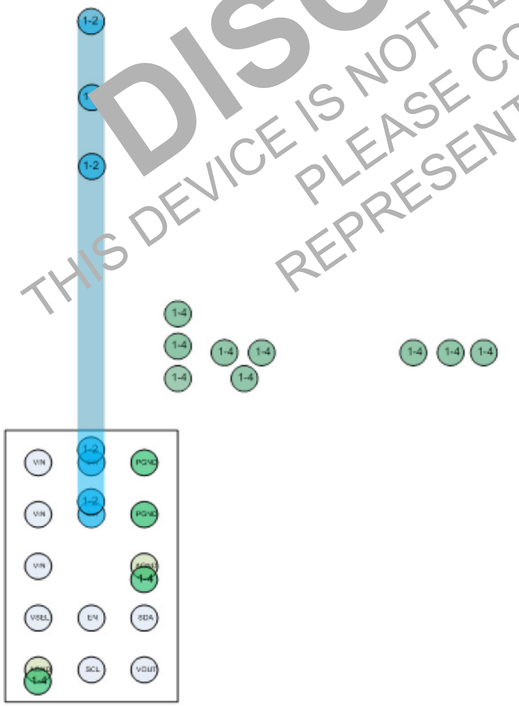
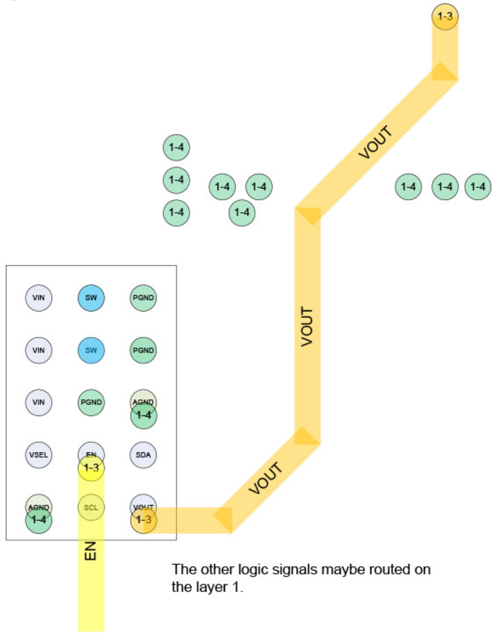


Figure 26. Layer 2



The other logic signals maybe routed on the layer 1.

Figure 27. Layer 3

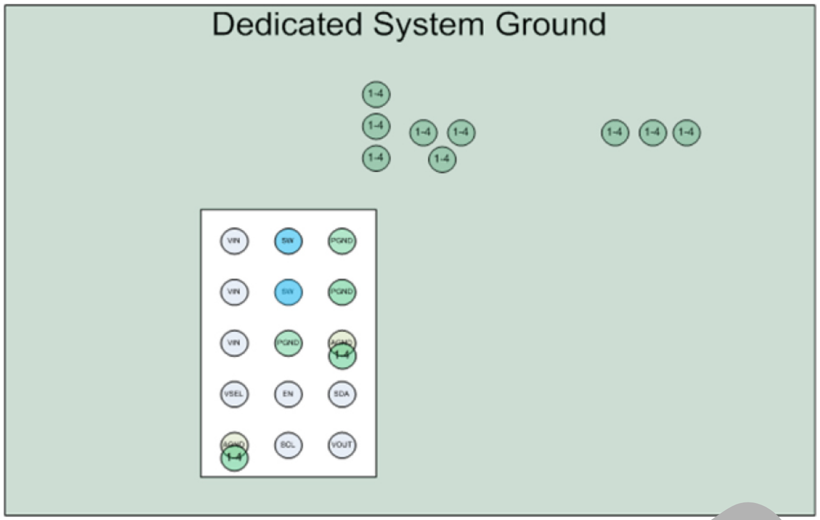
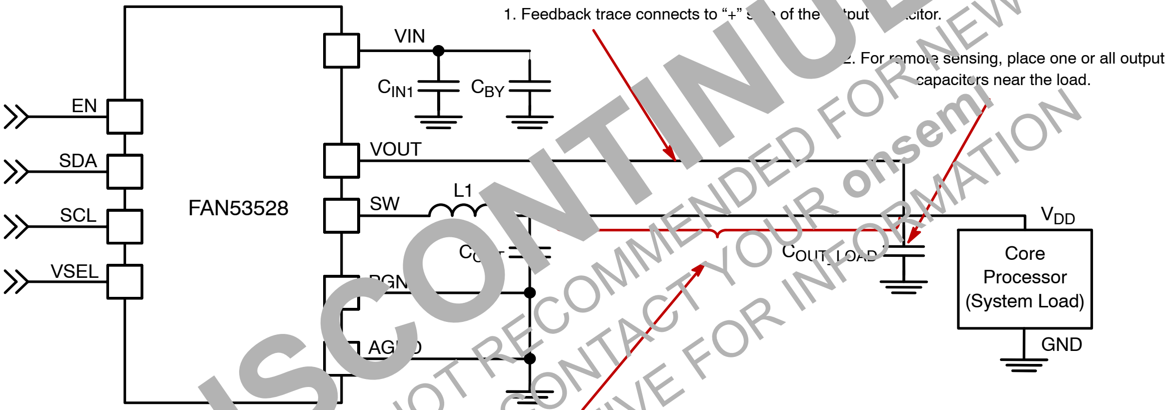


Figure 28. Layer 4



1. Feedback trace connects to "+" side of the output capacitor.

2. For remote sensing, place one or all output capacitors near the load.

3. If there are also output capacitors placed near the inductor, the maximum trace resistance between the inductor and the load should not exceed 30 mΩ.

Figure 29. Remote Sensing Schematic

**Table 17. PRODUCT SPECIFIC DIMENSIONS**

| D | E | X | Y |
|---|---|---|---|
| 2.015 ± 0.03 mm | 1.310 ± 0.03 mm | 0.255 mm | 0.2075 mm |

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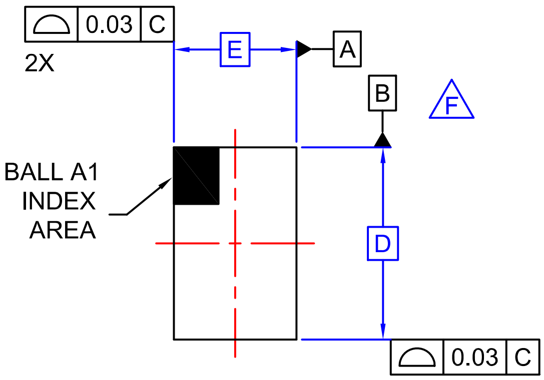
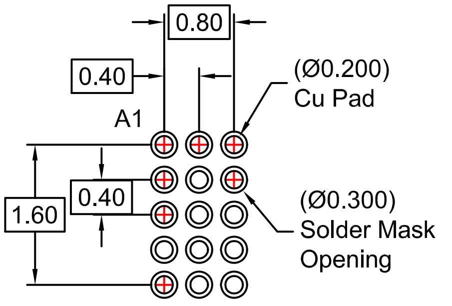
ISSUE O

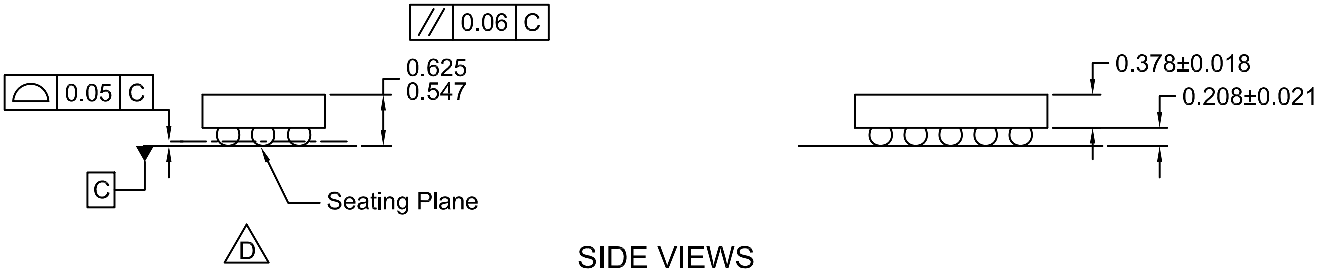
DATE 31 OCT 2016



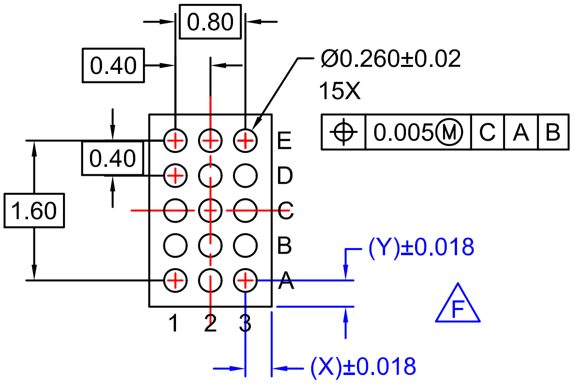
TOP VIEW



RECOMMENDED LAND PATTERN
(NSMD TYPE)



SIDE VIEWS



BOTTOM VIEW

NOTES

A. NO JEDEC REGISTRATION APPLIES.

B. DIMENSIONS ARE IN MILLIMETERS.

C. DIMENSIONS AND TOLERANCE PER ASME Y14.5 - 2009.

D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.

E. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).

F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

| | | |
|---|---|---|
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