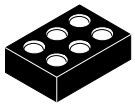
Synchronous Buck Regulator, 2.5 MHz

FAN53741



WLCSP6 1.38x0.94x0.625
CASE 567UH

Description

The FAN53741 is a 2.5 MHz step−down switching voltage regulator, that delivers a fixed output from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53741 is capable of delivering a peak efficiency of 97% and can support a max load of 1300 mA.

The regulator operates at a nominal fixed frequency of 2.5 MHz, which reduces the value of the external components achieving a total solution size of 5.24 mm^2. At moderate and light load, Pulse Frequency Modulation (PFM) is used to operate the device with a low quiescent current of 60 μA. Even with such a low quiescent current, the part exhibits excellent transient response during load swings. At higher loads, the system automatically switches to fixed−frequency control, operating at 2.5 MHz. In Shutdown Mode, the supply current drops below 0.5 μA, reducing power consumption.

The FAN53741 is available in 6−bump, 0.4 mm pitch, Wafer−Level Chip−Scale Package (WLCSP).

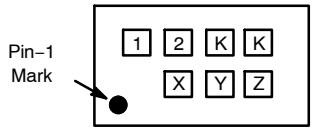
Features

- 60 μA Typical Quiescent Current
- 5.24 mm^2 Total Solution Size
- 1300 mA Output Current Capability
- Programmable Output Voltage 0.6 V to 3.3 V in 25 mV Steps via I^2C Functionality
- Programmable Current Limit 530 mA to 2150 mA in 108 mA Steps via I^2C Functionality
- 2.3 V to 5.5 V Input Voltage Range
- 2.5 MHz Fixed−Frequency Operation
- Best−in−Class Load Transient Response
- Internal Soft−Start Limits Battery Current Below 150 mA to avoid Brown−out Scenarios
- Protection Faults (UVLO, OCP and TSP)
- Thermal Shutdown and Overload Protection
- 6−Bump WLCSP, 0.4 mm Pitch
- This is a Pb−Free Device

Applications

- Smart Phones
- Wearables
- Smart Watch
- Health Monitoring
- Sensor Drive
- Energy Harvesting
- Utility and Safety Modules
- RF Modules

MARKING DIAGRAM



12	= Alphanumeric Device Marking
KK	= Lot Rune Code
X	= Alphabetical Year Code
Y	= 2−weeks Date Code
Z	= Assembly Plant Code

TYPICAL APPLICATION

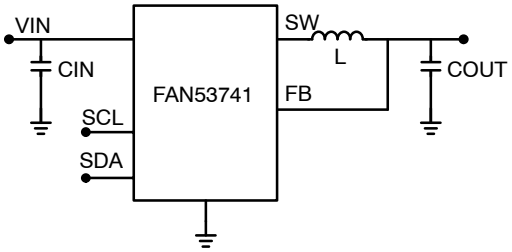


Figure 1. Typical Application

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Part Number	Output Voltage	Max. Output Current	Temperature Range	Package	Shipping†	Device Marking
FAN53741UC108X	0.6 V to 3.3 V	1300 mA	−40 to 85°C	WLCSP	3000 / Tape & Reel	GM

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

RECOMMENDED EXTERNAL COMPONENTS

Table 1. RECOMMENDED EXTERNAL COMPONENTS

Component	Description	Vendor	Parameter	Typ.	Unit
L	0.47 μH, 20%, 3.1 A, 43 mΩ	HTEH20161T−R47MSR−89 (Cyntec)	L	0.47	μH
CIN	2.2 μF, 20%, 6.3 V, X5R, 0402	C1005X5R0J225M050BC (TDK)	C	2.2	μF
COUT	10 μF, 20%, 6.3 V, X5R, 0402	C1005X5R0J106M050BC (TDK)	C	10	

PIN CONFIGURATION

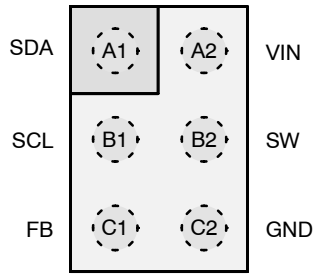


Figure 2. Top View (Bumps Down)

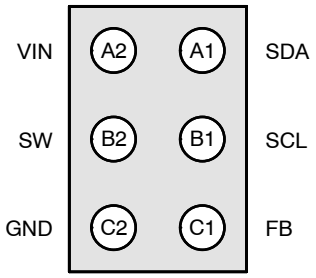


Figure 3. Bottom View (Bumps Up)

PIN DEFINITIONS

Pin #	Name	Description
A1	SDA	*SDA*. Serial Interface Data. Do not leave this pin floating.
A2	VIN	*Input Voltage*. Connect to input power source on positive terminal of input capacitor.
B1	SCL	*SCL*. Serial Interface Clock. Do not leave this pin floating.
B2	SW	*Switching Node*. Connect to SW pad of inductor.
C1	FB	*Feedback*. Connect to positive side of output capacitor.
C2	GND	*Ground*. Power and IC ground. All signals are referenced to this pin.

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VIN	Input Voltage	−0.3	6.5	V
V_{SW}	Voltage on SW Pin	−0.3	VIN + 0.3 (Note 1)	V
V_{CTRL}	SDA and SDA Pin Voltage	−0.3	VIN + 0.3 (Note 1)	V
	Other Pins	−0.3	VIN + 0.3 (Note 1)	V
ESD	Human Body Model per JESD22−A114	2.0		kV
	Charged Device Model per JESD22−C101	1.0		
T_J	Junction Temperature	−40	+150	°C
T_{STG}	Storage Temperature	−40	+150	°C
T_L	Lead Soldering Temperature, 10 Seconds	−	+260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Lesser of 6 V or VIN + 0.3 V.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Min	Max	Max	Unit
VIN	Supply Voltage Range	2.3	−	5.5	V
IOUT	Output Current	−	−	1300	mA
CIN	Input Capacitor	−	2.2	−	μF
COUT	Output Capacitor	−	10	−	μF
L	Inductor	−	0.47	−	μH
T_A	Operating Ambient Temperature	−40	−	+85	°C
T_J	Operating Junction Temperature	−40	−	+125	°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

THERMAL PROPERTIES

Symbol	Parameter	Min	Max	Max	Unit
θ_{JA}	Junction−to−Ambient Thermal Resistance (Note 2)	−	125	−	°C/W

2. Junction−to−ambient thermal resistance is a function of application and board layout. This data is simulated with four−layer 2s2p boards without vias in accordance to JESD51− JEDEC standard. Special attention must be paid not to exceed the junction temperature.

ELECTRICAL CHARACTERISTICS (Minimum and maximum values are at VIN = 3.8 V, T_A = −40°C to +85°C, unless otherwise noted. Typical values are at T_A = 25°C, VIN = 3.8 V, VOUT = 3.3 V.)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
$I_{Q,PFM}$	PFM Quiescent Current	ENABLE Bit = 1, PFM Mode, no load, non−switching	–	60	90	μA
I_{SD}	Shutdown Supply Current	ENABLE Bit = 0, no load	–	0.5	2	μA
V_{UVLO_RISE}	Under−Voltage Lockout Threshold	VIN Rising	2.10	2.15	2.22	V
V_{UVLO_FALL}		VIN Falling	2.00	2.05	2.11	V
V_{UVLO_HYS}	UVLO Hysteresis			100		mV
F_{SW}	Switching Frequency	PWM, no load	2.25	2.50	2.75	MHz
V_{OACC}	Output Voltage Accuracy	VOUT = 0.6 V to 2.0 V, IOUT = 0 A, PWM Mode	−20	–	+20	mV
		VOUT = 2.0 V to 3.3 V, IOUT = 0 A, PWM Mode	−1	–	+1	%
		VOUT = 0.6 V to 2.0 V, IOUT = 0 A, PFM Mode	−50	–	+50	mV
		VOUT = 2.0 V to 3.3 V, IOUT = 0 A, PFM Mode	−2.5	–	+2.5	%
I_{LIM_ACC}	Peak Inductor Current Limit Accuracy	Programmed to 1934 mA Current Limit Setting	1550	1934	2350	mA
I_{LIM_PRG}	Programmable Peak Inductor Current Limit Range		530	–	2150	mA
I_{LIM_NEG}	Negative Current Limit		–	−1000	–	mA
R_{DSON}	PMOS Resistance	VIN = VGS = 3.6 V	–	0.125	–	Ω
R_{DSON}	NMOS Resistance	VIN = VGS = 3.6 V	–	0.082	–	Ω

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

SYSTEM CHARACTERISTICS (The following System Characteristics are guaranteed by design and are not performed in production testing. Recommended operating conditions, unless otherwise noted, V_{IN} = 2.3 V to 5.5 V, T_A = −40°C to 85°C, V_{OUT} = 3.3 V. Typical values are given V_{IN} = 3.6 V, V_{OUT} = 3.3 V and T_A = 25°C. System Characteristics are based on circuit per Figure 1. L = 0.47 μH (0603 DFE160808S−R47M − MURATA, 3.4 A / 53 mΩ) CIN = 2.2 μF (0402 − C1005X5R0J225M050BC − TDK) COUT = 10 μF (0402 C1005X5R0J106M050BC −TDK).)

Symbol	Parameter	Condition	Min	Typ	Max	Unit
Eff	Efficiency	I_{OUT} = 1 mA	–	87	–	%
		I_{OUT} = 100 mA	–	96	–	
		I_{OUT} = 300 mA	–	97	–	
		I_{OUT} = 500 mA	–	96	–	
		I_{OUT} = 700 mA	–	95	–	
IOUT	IOUT MAX		1300		–	mA
$LOAD_{REG}$	Load Regulation	0 mA < IOUT < 1200 mA, VIN = 3.8 V	–	26	–	mV/A
$LINE_{REG}$	Line Regulation	3.8 V < VIN < 4.35 V, IOUT = 300 mA, PWM Mode	–	−0.6	–	mV/V
V_{TRRP}	Load Transient	I_{OUT} = 10 mA ⇔ 150 mA, T_R = T_F = 1 μs, Auto Mode, VIN = 3.8 V	–	±0	–	mV
V_{TRRP}	Load Transient	I_{OUT} = 100 mA ⇔ 1200 mA, T_R = T_F = 5 μs, Auto Mode, VIN = 3.8 V	–	±60	–	mV
V_{OUT_RIPPLE}	Ripple Voltage	I_{OUT} = 20 mA, PFM Mode, VIN = 4.35 V	–	50	–	mV
		I_{OUT} = 200 mA, PWM Mode, VIN = 4.35 V	–	12	–	

System Characteristics are tested closed loop while using the recommended external components table.

TYPICAL CHARACTERISTICS

(Unless otherwise specified, V_{IN} = 3.8 V, V_{OUT} = 3.3 V, Auto Mode, T_A = 25°C; circuit and components according to Figure 1 and Table 1.)

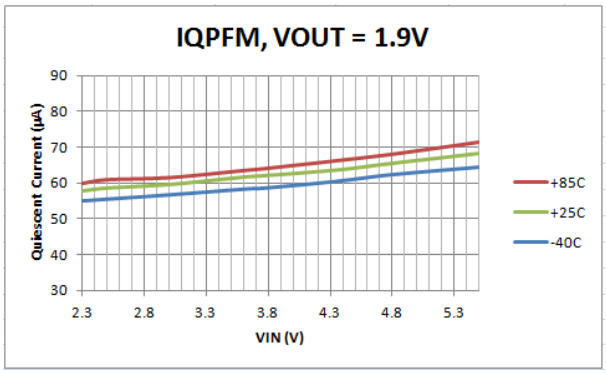


Figure 4. Quiescent Current vs. Input Voltage and Temperature, V_{OUT} = 1.9 V, Auto Mode

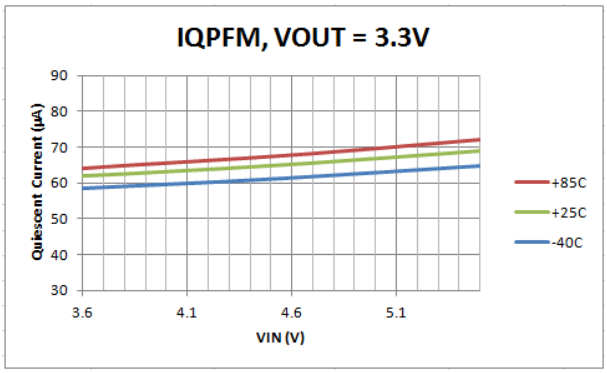


Figure 5. Quiescent Current vs. Input Voltage and Temperature, V_{OUT} = 3.3 V, Auto Mode

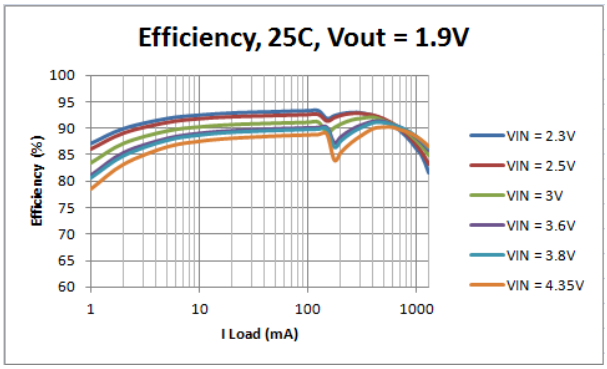


Figure 6. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 1.9 V, Auto Mode

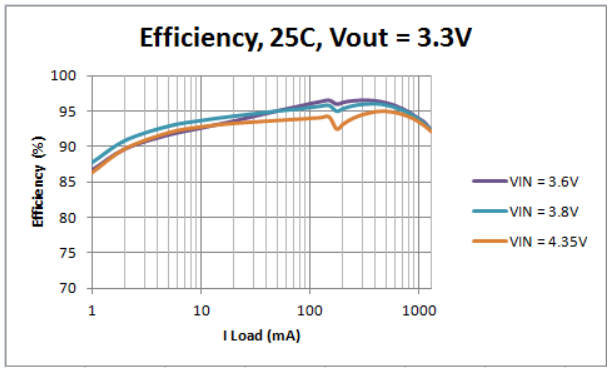


Figure 7. Efficiency vs. Load Current and Input Voltage, V_{OUT} = 3.3 V, Auto Mode

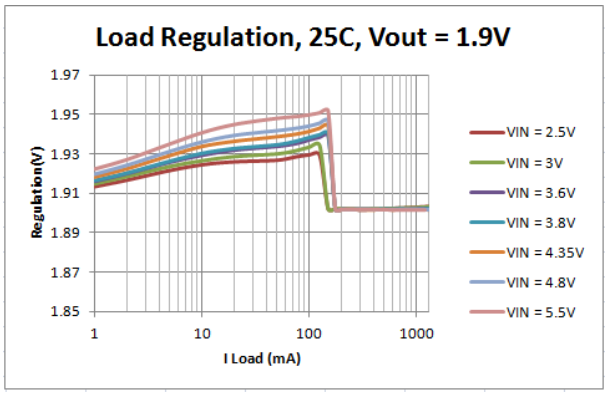


Figure 8. Load Regulation vs. Load Current and Input Voltage, V_{OUT} = 1.9 V, Auto Mode

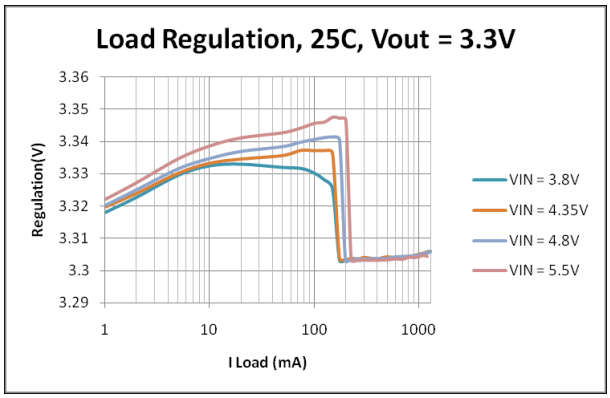


Figure 9. Load Regulation vs. Load Current and Input Voltage, V_{OUT} = 3.3 V, Auto Mode

OPERATION DESCRIPTION

The FAN53741 is a 2.5 MHz, step−down switching voltage regulator from an input voltage supply of 2.3 V to 5.5 V. Using a proprietary architecture with synchronous rectification, the FAN53741 is capable of delivering a peak efficiency of 97%. The regulator operates at a nominal fixed frequency of 2.5 MHz, which reduces the value of the external components to 0.47 μH for the output inductor and 10 μF for the output capacitor.

The FAN53741 provides a fixed output voltage ranging from 0.6 V to 3.3 V, and can be programmed in 25 mV steps via I^2C. The FAN53741 can support a max current 1300 mA.

MODES OF OPERATIONS

PFM Mode

At light load operation in AUTO Mode, the device enters PFM mode when load current is below 124 mA typically. PFM mode reduces switching frequency as well as battery current draw, which yields high efficiency.

PWM Mode

During PWM mode, the device switches at a nominal fixed frequency of 2.5 MHz, which reduces the values of the external components. The part enters PWM when load currents exceed 140 mA typically. In PWM mode, the device has excellent load regulation ideal for power sensitive accurate loads. The FAN53741 can be forced into PWM regardless of the load current by inserting a 1 to the FORCE_PWM register bit.

PROTECTION FEATURES

VOUT Fault

If the VOUT fails to reach 95% of VOUT target in 7 ms, a VOUT fault is declared. During the fault condition the part restarts every 20 ms to achieve the 95% target voltage. Once the output voltage reaches the 95% VOUT target voltage the VOUT fault clears.

Over−Current Limit (OCP)

A heavy load or short circuit on the output causes the current in the inductor to increase until a maximum current threshold is reached in the high−side switch. Upon reaching this point, the high−side switch turns off, preventing high currents from causing damage. After 500 μs of current limit, the regulator triggers an over−current fault, causing the regulator to shut down for about 20 ms before attempting a restart. If the fault is caused by short circuit, the soft−start circuit attempts to restart and produces an over−current fault after about 20 ms. The Peak Inductor Current Limit can be programmed via I^2C and range from 530 mA to 2150 mA max in 108 mA steps.

Under−Voltage Lockout (UVLO)

When EN is HIGH, the under−voltage lockout keeps the part from operating until the input supply voltage rises high enough to properly operate. This ensures no misbehavior of the regulator during startup or shutdown.

Thermal Shutdown Protection (TSP)

When the die temperature increases, due to a high load condition and/or a high ambient temperature, the output switching is disabled until the die temperature falls sufficiently. The junction temperature at which the thermal shutdown activates is nominally 150°C with a 15°C hysteresis.

Negative Current Limit

The FAN53741 has a negative current limit protection which limits the current through the NFET. If a voltage is applied to output of buck which is higher than VOUT target while in PWM, then a negative current is detected. Once the inductor current hits −1 A for one cycle, then the output begins to tristate until the applied voltage is released and the output voltage falls below the regulated voltage.

In PFM mode, the Zero Crossing Detection does not allow any negative current to flow within inductor , any voltage higher > vout target applied to output will cause the regulator to enter tri−state and block current back through inductor

If voltage applied to VOUT is greater than VIN, then body diode of high side FET will conduct.

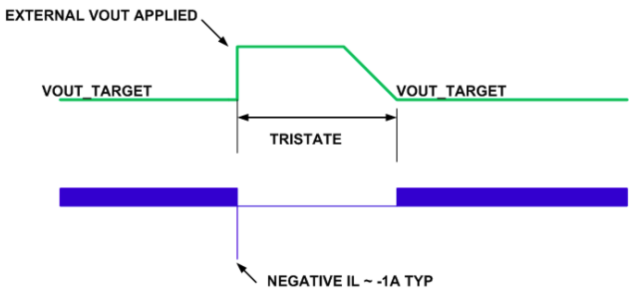


Figure 10.

OPERATION MODE

Programmable Output Voltage

The FAN53741 output voltage can be programmed via I^2C from 0.6 V to 3.3 V in 25 mV steps. The voltage transition going from a lower to a higher voltage is a single step with transition time dependent on output current and output capacitance. The output current drives the voltage slew rate from higher to lower voltage transitions. The FAN53741 does not have DVS functionality.

Startup Description

To enable the FAN53741, the ENABLE reg must be set to 1. FAN53741 has internal soft−start which limits the battery current to 150 mA minimizing any brown out applications.

Once the target VOUT voltage reaches 95% then the full current limit operation enters. The device starts up within 600 μs typical with the recommended external components table.

If the part fails to startup within about 7 ms, then the part will declare a startup fault and will reattempt to start within 20 ms.

Shutdown

To disable the FAN53741, the ENABLE reg should be configured to code 0. When part is disabled, output voltage will tristate and discharge via load or pull down resistor.

Active Pull Down

The FAN53741 has an active pull down to discharge the output capacitance. During a negative VOUT transition or when the ENABLE reg is set from 1 to 0, within one clock cycle, the active pull down is active and discharges the VOUT via a internal resistor. This functionality is enabled by setting Reg6[2] to 1 if required while having four options of pull down strength to choose from in Reg6[1:0]: Open, 50 Ω, 100 Ω, and 200 Ω.

I^2C

Slave Address

The hex slave address is different for all parts in the family. Other slave addresses can be accommodated upon request. Contact your **onsemi** representative.

Device	Hex	Decimal	Binary
FAN53741	7h'52	82	1010010

I^2C Slave Address Byte for FAN53741.

7	6	5	4	3	2	1	0
1	0	1	0	0	1	0	R/W

Read = 1, Write = 0

TIMING DIAGRAMS

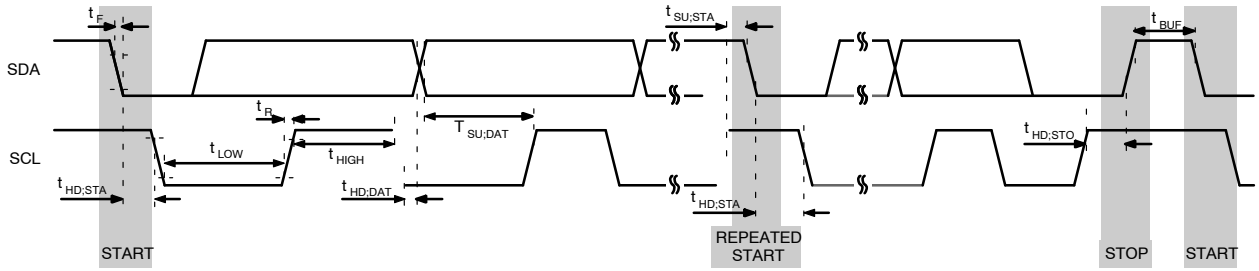
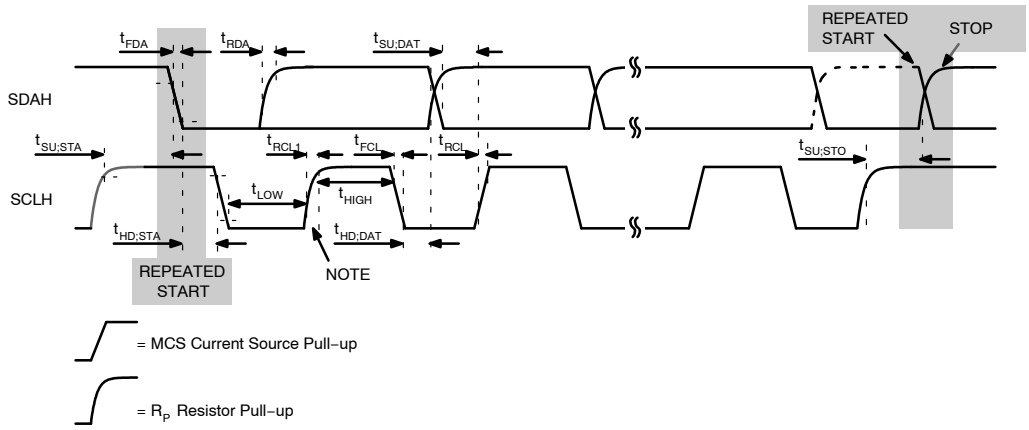


Figure 11. I²C Interface Timing for Fast Plus, Fast, and Slow Modes



NOTE: First rising edge of SCLH after Repeated Start and after each ACK bit.

Figure 12. I²C Interface Timing for High−Speed Mode

Bus Timing

As shown in Figure 13 data is normally transferred when SCL is LOW. Data is clocked in on the rising edge of SCL. Typically, data transitions shortly at or after the falling edge of SCL to allow sufficient time for the data to set up before the next SCL rising edge.

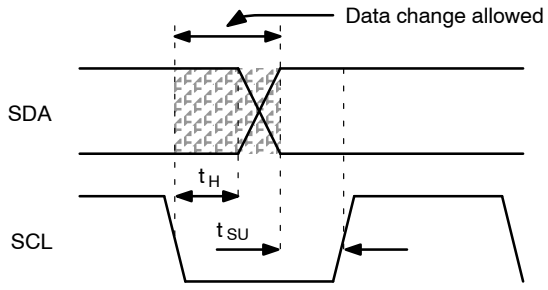


Figure 13. Data Transfer Timing

Each bus transaction begins and ends with SDA and SCL HIGH. A transaction begins with a START condition, which is defined as SDA transitioning from 1 to 0 with SCL HIGH, as shown in Figure 14.

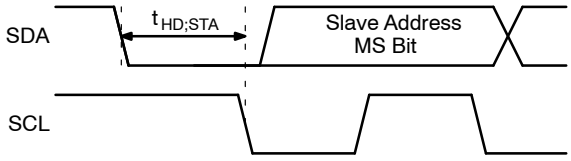


Figure 14. START Bit

A transaction ends with a STOP condition, defined as SDA transitioning from 0 to 1 with SCL high, as shown in Figure 15.

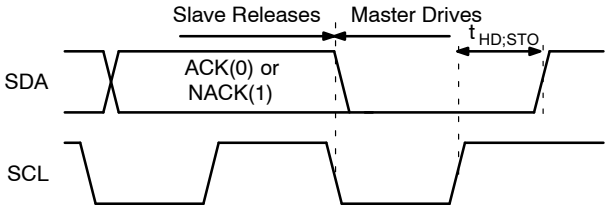


Figure 15. STOP Bit

During a read from the FAN53741, the master issues a REPEATED START after sending the register address and before resending the slave address. The REPEATED START is a 1 to 0 transition on SDA while SCL is HIGH, as shown in Figure 16.

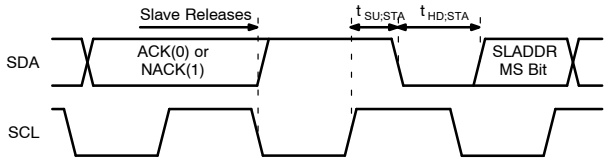


Figure 16. REPEATED START Timing

High−Speed (HS) Mode

The protocols for High−Speed (HS), Low−Speed (LS), and Fast−Speed (FS) Modes are identical; except the bus speed for HS Mode is 3.4 MHz. HS Mode is entered when the bus master sends the HS master code 00001XXX after a START condition (Figure 14). The master code is sent in Fast or Fast−Plus Mode (less than 1 MHz clock); slaves do not ACK this transmission.

The master generates a REPEATED START condition (Figure 16) that causes all slaves on the bus to switch to HS Mode. The master then sends I^2C packets, as described above, using the HS Mode clock rate and timing.

The bus remains in HS Mode until a STOP bit (Figure 15) is sent by the master. While in HS Mode, packets are separated by REPEATED START conditions (Figure 16).

Read and Write Transactions

The following figures outline the sequences for data read and write. Bus control is signified by the shading of the packet, defined as Master Drives Bus and Slave Driver Bus. All addresses and data are MSB first.

Table 2. I^2C BIT DEFINITIONS FOR FIGURE 17 AND FIGURE 18

Symbol	Definition
S	START, *see Figure 14*
P	STOP, *see Figure 15*
R	REPEATED START, *see Figure 16*
A	ACK. The slave drives SDA to 0 to acknowledge the preceding packet.
$\overline{A}$	NACK. The slave sends a 1 to NACK the preceding packet.

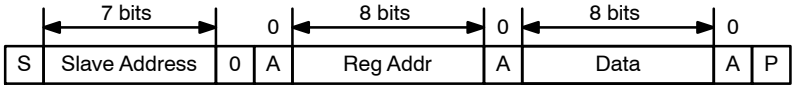


Figure 17. Write Transaction

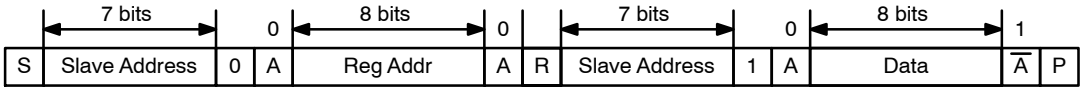


Figure 18. Write Transaction Followed by a Read Transaction

REGISTER MAP

Table 3. REGISTER MAP

					Read Only	Write Only	Read / Write	Read / Clear	Write / Clear
Address	**Name**	**Bit[7]**	**Bit[6]**	**Bit[5]**	**Bit[4]**	**Bit[3]**	**Bit[2]**	**Bit[1]**	**Bit[0]**
0x00	Product ID_REV	Product ID				Silicon Revision			
0x01	Fault Flag Status	0		POR	UVLO Fault	Over Temp Fault	Current Limit Fault	Startup Timeout Fault	Vout Short Fault
0x02	Fault Live Status	0			UVLO	Over Temp	Current Limit	Startup Timeout	Vout Short
0x03	MODE	0						ENABLE	FORCE_PWM
0x04	VSEL	0	BUCK_VOUT						
0x05	ILIMIT	0				ILIM			
0x06	PULLDOWN	0					PULLDOWN	PULL DOWN SEL	
0x07	RESET	SOFT_RESET							

REGISTER DETAILS

Table 4. REGISTER DETAILS 1

0x00 Product ID_REV				Default = 00010000
Bit	**Name**	**Default**	**Type**	**Description**
7:4	Product ID	0001	Read	Capture Product configuration to allow customers to identify a device (if they have access to I^2C) and allow read−back of desired configuration in the event of a customer return *Code* *<<Effect>>* 0000 – 0001 FAN53741 0010 Reserved 0011 Reserved 0100 Reserved 0101 Reserved 0110 Reserved 0111 Reserved 1000 Reserved 1001 Reserved 1010 Reserved 1011 Reserved 1100 Reserved 1101 Reserved 1110 Reserved 1111 Reserved
3:0	Silicon Revision	0000	Read	To allow identification of silicon revision through ATE test. Customer visible when there is I^2C bus that the customer has access to *Code* *<<Effect>>* 000 Initial Silicon 001 Increment register with each iteration 010 011 100 101 110 111

Table 5. REGISTER DETAILS 2

0x01 Fault Flag Status				Default = 00100000
Bit	**Name**	**Default**	**Type**	**Description**
7:6	Unused			
5	POR	1	R/CL R	Displays POR fault status. This indicator is latched when POR occurs and causes a fault. The flag is clear upon read. *Code* ||–– *Effect* ––|| 0 Default 1 Power−on reset occurred
4	UVLO Fault	0	R/CL R	Displays UVLO fault status. This indicator is latched when UVLO occurs and causes a fault. The flag is clear upon read. *Code* ||–– *Effect* ––|| 0 No UVLO fault 1 A UVLO fault occurred
3	Over Temp Fault	0	R/CL R	Displays over temp fault status. This indicator is latched when over temp occurs and causes a fault. The flag is clear upon read. *Code* ||–– *Effect* ––|| 0 No over temp fault 1 An over temp fault occurred
2	Current Limit Fault	0	R/CL R	Displays over current fault status. This indicator is latched when over current occurs and causes a fault. The flag is cleared upon read. *Code* ||–– *Effect* ––|| 0 No over current fault 1 An over current fault occurred
1	Startup Timeout Fault	0	R/CL R	Displays startup timeout fault status. This indicator is latched when startup timeout occurs and causes a fault. The flag is cleared upon read. *Code* ||–– *Effect* ––|| 0 No startup timeout fault 1 A startup timeout fault occurred
0	Vout Short Fault	0	R/CL R	Displays Vout short fault status. This indicator is latched when Vout short occurs and causes a fault. The flag is clear upon read. *Code* ||–– *Effect* ––|| 0 No Vout short fault 1 A Vout short fault occurred

Table 6. REGISTER DETAILS 3

0x02 Fault Live Status				Default = 00011000
Bit	**Name**	**Default**	**Type**	**Description**
7:5	Unused			
4	UVLO	1	Read	Displays UVLO comparator status only when EN is set HIGH. Otherwise, this bit reads as 1. *Code* ||-- *Effect* --|| 0 No UVLO fault 1 UVLO fault
3	Over Temp	1	Read	Displays over temp comparator status only when EN is set HIGH. Otherwise, this bit reads as 1. *Code* ||-- *Effect* --|| 0 No over temp fault 1 Over temp fault
2	Current Limit	0	Read	Displays over current comparator status only. A 1 will only be captured at the moment that a fault is declared which last for one clock cycle. Thereafter, it will go into FAULT state while setting this Live Flag to 0. *Code* ||-- *Effect* --|| 0 No over current fault 1 Over current fault
1	Startup Time	0	Read	Displays startup timeout timer status. A 1 will only be captured at the moment that a fault is declared which last for one clock cycle. Thereafter, it will go into FAULT state while setting this Live Flag to 0. *Code* ||-- *Effect* --|| 0 No startup timeout fault 1 Startup timeout fault
0	Vout Short	0	Read	Displays Vout short comparator status. A 1 will only be captured at the moment that a fault is declared which last for one clock cycle. Thereafter, it will go into FAULT state while setting this Live Flag to 0. *Code* ||-- *Effect* --|| 0 No Vout short fault 1 Vout short fault

Table 7. REGISTER DETAILS 4

0x03 MODE				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:3	Unused			
1	ENABLE	0	R/W	This register enables/disables the buck regulator. Setting a code 0, shutdowns the device, where as code 1 enables the device. *Code* *Effect* 0 Regulation Disabled 1 Regulation Enabled
0	FORCE_PWM	0	R/W	Forces the part to operate in PWM mode regardless of the load current. *Code* *Effect* 0 Auto (PFM / PWM depending on load current) 1 PWM

Table 8. REGISTER DETAILS 5

0x04 VSEL				Default = 0111 101			
Bit	**Name**	**Default**	**Type**	**Description**			
7	Unused						
6:0	BUCK_VOUT	1111011	R/W	Sets buck regulation target voltage.			
				Hex	*VOUT*	*Hex*	*VOUT*
				00	Reserved	40	1.825 V
				01	Reserved	41	1.850 V
				02	Reserved	42	1.875 V
				03	Reserved	43	1.900 V
				04	Reserved	44	1.925 V
				05	Reserved	45	1.950 V
				06	Reserved	46	1.975 V
				07	Reserved	47	2.000 V
				08	Reserved	48	2.025 V
				09	Reserved	49	2.050 V
				0A	Reserved	4A	2.075 V
				0B	Reserved	4B	2.100 V
				0C	Reserved	4C	2.125 V
				0D	Reserved	4D	2.150 V
				0E	Reserved	4E	2.175 V
				0F	600 mV	4F	2.200 V
				10	625 mV	50	2.225 V
				11	650 mV	51	2.250 V
				12	675 mV	52	2.275 V
				13	700 mV	53	2.300 V
				14	725 mV	54	2.325 V
				15	750 mV	55	2.350 V
				16	775 mV	56	2.375 V
				17	800 mV	57	2.400 V
				18	825 mV	58	2.425 V
				19	850 mV	59	2.450 V
				1A	875 mV	5A	2.475 V
				1B	900 mV	5B	2.500 V
				1C	925 mV	5C	2.525 V
				1D	950 mV	5D	2.550 V
				1E	975 mV	5E	2.575 V
				1F	1.000 V	5F	2.600 V
				20	1.025 V	60	2.625 V
				21	1.050 V	61	2.650 V
				22	1.075 V	62	2.675 V
				23	1.100 V	63	2.700 V
				24	1.125 V	64	2.725 V
				25	1.150 V	65	2.750 V
				26	1.175 V	66	2.775 V
				27	1.200 V	67	2.800 V
				28	1.225 V	68	2.825 V
				29	1.250 V	69	2.850 V
				2A	1.275 V	6A	2.875 V
				2B	1.300 V	6B	2.900 V
				2C	1.325 V	6C	2.925 V
				2D	1.350 V	6D	2.950 V
				2E	1.375 V	6E	2.975 V
				2F	1.400 V	6F	3.000 V
				30	1.425 V	70	3.025 V
				31	1.450 V	71	3.050 V
				32	1.475 V	72	3.075 V

Table 8. REGISTER DETAILS 5 (continued)

0x04 VSEL				Default = 0111 101			
Bit	**Name**	**Default**	**Type**	**Description**			
6:0	BUCK_ VOUT	1111011	R/W	*Hex*	*VOUT*	*Hex*	*VOUT*
				33	1.500 V	73	3.100 V
				34	1.525 V	74	3.125 V
				35	1.550 V	75	3.150 V
				36	1.575 V	76	3.175 V
				37	1.600 V	77	3.200 V
				38	1.625 V	78	3.225 V
				39	1.650 V	79	3.250 V
				3A	1.675 V	7A	3.275 V
				3B	1.700 V	7B	3.300 V
				3C	1.725 V	7C	Reserved
				3D	1.750 V	7D	Reserved
				3E	1.775 V	7E	Reserved
				3F	1.800 V	7F	Reserved

Table 9. REGISTER DETAILS 6

0x05 ILIMIT				Default = 00001111	
Bit	**Name**	**Default**	**Type**	**Description**	
7:4	Unused				
3:0	ILIM	1111	R/W	This Register sets the peak inductor current limit thresholds. The Range is from 530 mA to 2150 mA in 108 mA steps.	
				Code	||–– *Effect* ––||
				0000	530 mA Current Limit (Open Loop)
				0010	746 mA Current Limit (Open Loop)
				0011	854 mA Current Limit (Open Loop)
				0100	962 mA Current Limit (Open Loop)
				1000	1394 mA Current Limit (Open Loop)
				1111	2150 mA Current Limit (Open Loop)

Table 10. REGISTER DETAILS 7

0x06 PULLDOWN				Default = 00000000	
Bit	**Name**	**Default**	**Type**	**Description**	
7:3	Unused				
2	Pull Down	0	R/w	This register activates/deactivates the internal pull down resistor. Setting to Code 1, the pull down is active when ENABLE goes from 1 to 0 and on any negative V_{OUT} transitions.	
				Code	*Status of Pull down*
				0	Pull down not used (OFF)
				1	Pull down active during transition
1:0	Pull Down SEL	00	R/w	This register sets the strength of the pull down resistor.	
				Code	*Strength of Pull down*
				00	OPEN
				01	200 Ω
				10	100 Ω
				11	50 Ω

Table 11. REGISTER DETAILS 7

0x07 RESET				Default = 00000000
Bit	**Name**	**Default**	**Type**	**Description**
7:0	SOFT_RESET	00000000	Write	The software reset register allows all I^2C settings to be reverted to POR defaults when *0x60h* code is written to it.

APPLICATIONS INFORMATION

Selecting the Inductor

The output inductor must meet both the required inductance and the energy−handling capability of the application. The inductor value affects average current limit, output voltage ripple, and efficiency.

The ripple current (ΔI) of the regulator is:

$$\Delta I \approx \frac{V_{OUT}}{V_{IN}} \cdot \left(\frac{V_{IN} - V_{OUT}}{L \cdot f_{SW}}\right) \quad \text{(eq. 1)}$$

The maximum average load current, $I_{MAX(LOAD)}$, is related to the peak current limit, $I_{LIM(PK)}$, by the ripple current, given by:

$$I_{MAX(LOAD)} = I_{LIM(PK)} - \frac{\Delta I}{2} \quad \text{(eq. 2)}$$

The transition between PFM and PWM operation is determined by the point at which the inductor valley current crosses zero. The regulator DC current when the inductor current crosses zero, I_{DCM}, is:

$$I_{DCM} = \frac{\Delta I}{2} \quad \text{(eq. 3)}$$

The FAN53741 is optimized for operation with L = 0.47 μH. The inductor should be rated to maintain at least 80% of its value at I_{LIM_ACC}. It is recommended to select an inductor where its saturation current is above the I_{LIM_ACC} MAX value.

Efficiency is affected by the inductor DCR and inductance value. Decreasing the inductor value for a given physical size typically decreases the DCR; but because ΔI increases, the RMS current increases, as do the core and skin effect losses.

$$I_{RMS} = \sqrt{I_{OUT(DC)}^{\ 2} + \frac{\Delta I^2}{12}} \quad \text{(eq. 4)}$$

The increased RMS current produces higher losses through the $R_{DS(ON)}$ of the IC MOSFETs, as well as the inductor DCR.

Increasing the inductor value produces lower RMS currents, but degrades transient response. For a given physical inductor size, increased inductance usually results in an inductor with lower saturation current and higher DCR.

Table 12 shows the effects of inductance higher or lower than the recommended 1.0 mH on regulator performance.

Output Capacitor

Increasing C_{OUT} has no effect on loop stability and can therefore be increased to reduce output voltage ripple or to improve transient response. Vice versa, lower C_{OUT} can be used but with a compromise of load transient response. Output voltage ripple, ΔV^{OUT}, is:

$$\Delta V_{OUT} = \Delta I_L \left[\frac{f_{SW} \cdot C_{OUT} \cdot ESR^2}{2 \cdot D \cdot (1 - D)} + \frac{1}{8 \cdot f_{SW} \cdot C_{OUT}}\right] \quad \text{(eq. 5)}$$

Input Capacitor

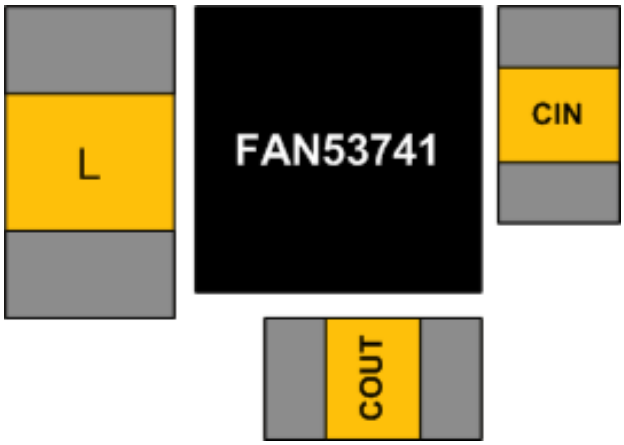
The 2.2 μF ceramic input capacitor should be placed as close as possible between the VIN pin and GND to minimize the parasitic inductance. If a long wire is used to bring power to the IC, additional “bulk” capacitance (electrolytic or tantalum) should be placed between C_{IN} and the power source lead to reduce the ringing that can occur between the inductance of the power source leads and C_{IN}.

The effective capacitance value decreases as V_{IN} increases due to DC bias effects.

Table 12. EFFECTS OF CHANGES IN INDUCTOR VALUE (FROM 0.47 μH RECOMMENDED VALUE) ON REGULATOR PERFORMANCE

Inductor Value	$I_{MAX(LOAD)}$	ΔV_{OUT}	Transient Response
Increase	Increase	Decrease	Degraded
Decrease	Decrease	Increase	Improved

RECOMMENDED LAYOUT



LAYOUT CONSIDERATION

To minimize spikes at VOUT, COUT must be placed as close as possible to PGND and VOUT, as shown in Recommended Layout. For thermal reasons, it is suggested to maximize the pour area for all planes other than SW. Especially the ground pour should be set to fill all available PCB surface area and tied to internal layers with a cluster of thermal via

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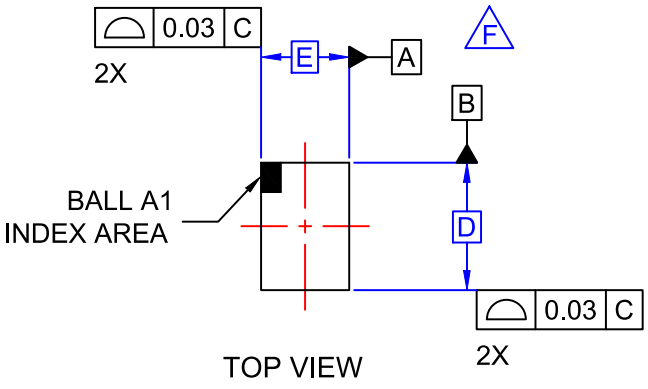
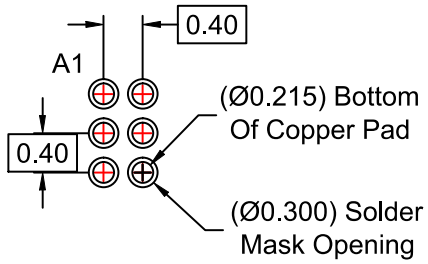
CASE 567UH
ISSUE O

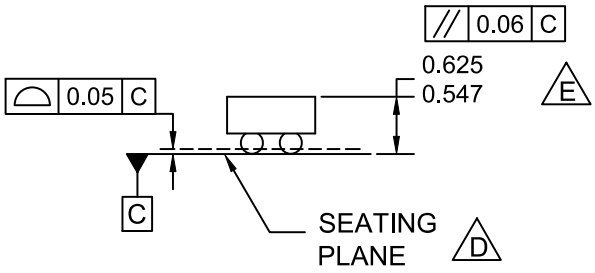
DATE 31 APR 2017

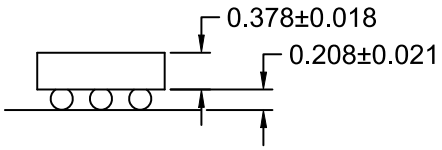


TOP VIEW

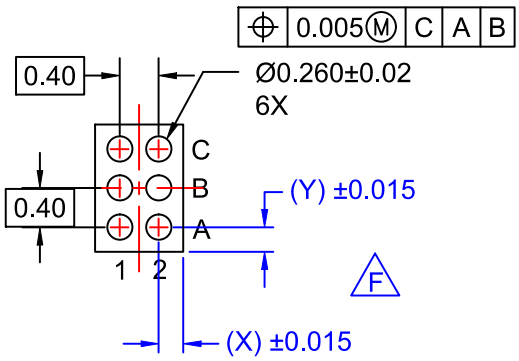


RECOMMENDED LAND PATTERN
(NSMD PAD TYPE)





SIDE VIEWS



BOTTOM VIEW

NOTES
A. NO JEDEC REGISTRATION APPLIES.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCE PER ASME Y14.5M, 2009.
D. DATUM C IS DEFINED BY THE SPHERICAL CROWNS OF THE BALLS.
E. PACKAGE NOMINAL HEIGHT IS 586 ± 39 MICRONS (547-625 MICRONS).
F. FOR DIMENSIONS D,E,X, AND Y SEE PRODUCT DATASHEET.

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