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# FAN73901

## High- and Low-Side, Gate-Drive IC

### Features

- Floating Channels for Bootstrap Operation to +600 V
- Typically 2.5 A / 2.5 A Sourcing/Sinking Current Driving Capability
- Common-Mode dv/dt Noise Canceling Circuit
- Built-in Under-Voltage Lockout for Both Channels
- Matched Propagation Delay for Both Channels
- 3.3 V and 5 V Input Logic Compatible
- Output In-Phase with Input

### Applications

- Half-Bridge Driver
- HID Lamp Ballast
- SMPS
- Motor Driver

### Description

The FAN73901 is a monolithic high- and low-side gate-drive IC, which can drive high-speed MOSFETs and IGBTs that operate up to +600 V. It has a buffered output stage with all NMOS transistors designed for high pulse current driving capability and minimum cross-conduction.

Fairchild's high-voltage process and common-mode noise canceling techniques provide stable operation of the high-side driver under high dv/dt noise circumstances. An advanced level-shift circuit offers high-side gate driver operation up to  $V_S = -9.8$  V (typical) for  $V_{BS} = 15$  V.

The UVLO circuit prevents malfunction when  $V_{DD}$  and  $V_{BS}$  are lower than the specified threshold voltage.

The high current and low output voltage drop features make sFAN73901 suitable for switching power supply, motor driver, and high-power DC-DC converter applications.

8-SOP



### Ordering Information

Part Number	Package	Operating Temperature Range	Packing Method
FAN73901M	8-SOP	-40°C ~ 125°C	Tube
FAN73901MX			Tape & Reel

### Typical Application Circuit

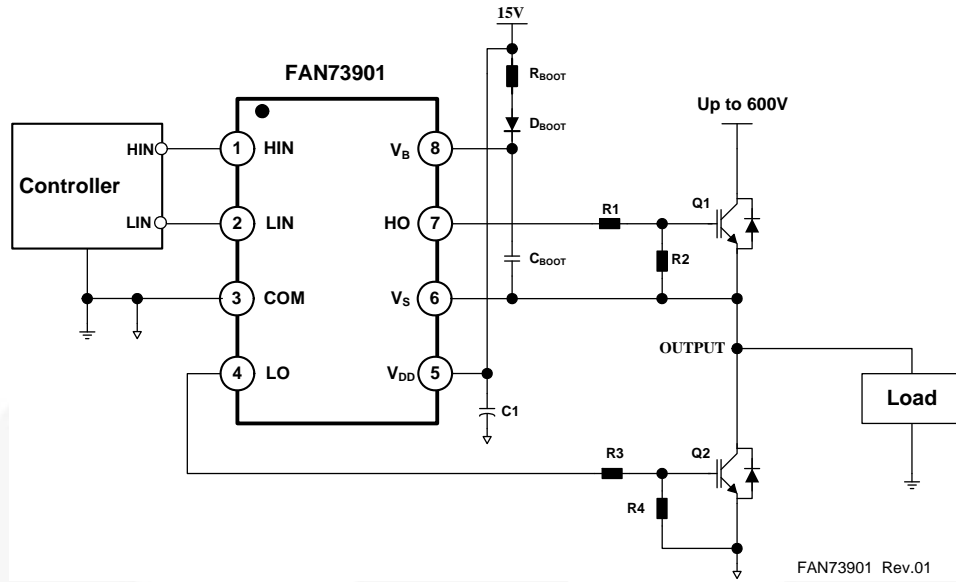


Figure 1. Application Circuit for Half-Bridge

### Internal Block Diagram

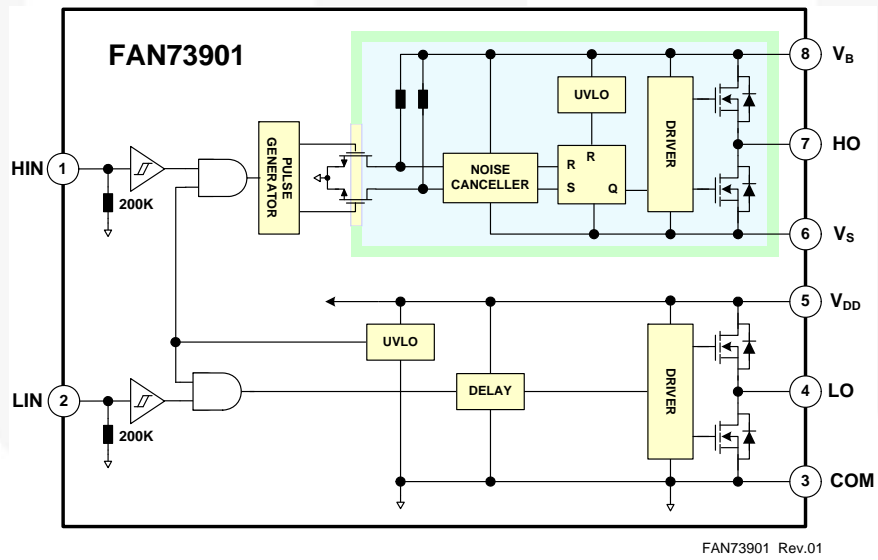
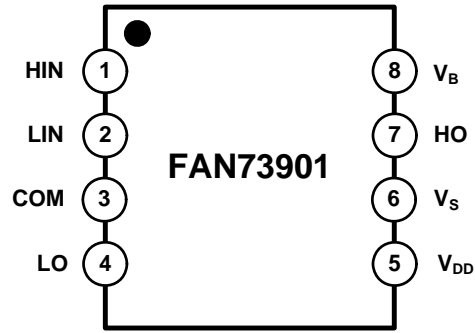


Figure 2. Functional Block Diagram

## Pin Configuration



FAN73901 Rev.01

Figure 3. Pin Assignments (Top View)

## Pin Definitions

Pin #	Name	Description
1	HIN	Logic Input for High-Side Gate Driver Output
2	LIN	Logic Input for Low-Side Gate Driver Output
3	COM	Low-Side Driver Return
4	LO	Low-Side Driver Output
5	$V_{DD}$	Low-Side and Logic Part Supply Voltage
6	$V_S$	High-Voltage Floating Supply Return
7	HO	High-Side Driver Output
8	$V_B$	High-Side Floating Supply

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.  $T_A=25^{\circ}\text{C}$ , unless otherwise specified.

Symbol	Characteristics	Min.	Max.	Unit
$V_S$	High-Side Floating Supply Offset Voltage	$V_B-25$	$V_B+0.3$	V
$V_B$	High-Side Floating Supply Voltage	-0.3	625.0	V
$V_{HO}$	High-Side Floating Output Voltage HO	$V_S-0.3$	$V_B+0.3$	V
$V_{DD}$	Low-Side and Logic Fixed Supply Voltage	-0.3	25.0	V
$V_{LO}$	Low-Side Output Voltage LO	-0.3	$V_{DD}+0.3$	V
$V_{IN}$	Logic Input Voltage (HIN and LIN)	-0.3	$V_{DD}+0.3$	V
$dV_S/dt$	Allowable Offset Voltage Slew Rate		50	V/ns
$P_D$	Power Dissipation <sup>(1)(2)(3)</sup>		0.625	W
$\theta_{JA}$	Thermal Resistance, Junction-to-Ambient		200	$^{\circ}\text{C}/\text{W}$
$T_J$	Junction Temperature		+150	$^{\circ}\text{C}$
$T_{STG}$	Storage Temperature		+150	$^{\circ}\text{C}$

### Notes:

- Mounted on 76.2 x 114.3 x 1.6 mm PCB (FR-4 glass epoxy material).
- Refer to the following standards:
  - JESD51-2: Integral circuits thermal test method environmental conditions - natural convection
  - JESD51-3: Low effective thermal conductivity test board for leaded surface mount packages.
- Do not exceed  $P_D$  under any circumstances.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to absolute maximum ratings.

Symbol	Parameter	Min.	Max.	Unit
$V_B$	High-Side Floating Supply Voltage	$V_S+10$	$V_S+20$	V
$V_S$	High-Side Floating Supply Offset Voltage	$6-V_{DD}$	600	V
$V_{HO}$	High-Side Output Voltage	$V_S$	$V_B$	V
$V_{DD}$	Low-Side and Logic Supply Voltage	10	20	V
$V_{LO}$	Low-Side Output Voltage	COM	$V_{DD}$	V
$V_{IN}$	Logic Input Voltage (HIN and LIN)	COM	$V_{DD}$	V
$T_A$	Operating Ambient Temperature	-40	+125	$^{\circ}\text{C}$

## Electrical Characteristics

$V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ )=15.0 V,  $V_S$ =COM,  $T_A$ =25°C, unless otherwise specified. The  $V_{IL}$ ,  $V_{IH}$ , and  $I_{IN}$  parameters are referenced to COM and are applicable to the respective input signals HIN and LIN. The  $V_O$  and  $I_O$  parameters are referenced to COM and  $V_S$  is applicable to the respective output signals HO and LO.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
<b>POWER SUPPLY SECTION (<math>V_{DD}</math> AND <math>V_{BS}</math>)</b>						
$V_{DDUV+}$ $V_{BSUV+}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Positive-Going Threshold		8.0	8.8	9.8	V
$V_{DDUV-}$ $V_{BSUV-}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Negative-Going Threshold		7.4	8.3	9.0	V
$V_{DDUVH}$ $V_{BSUVH}$	$V_{DD}$ and $V_{BS}$ Supply Under-Voltage Lockout Hysteresis Voltage			0.5		V
$I_{LK}$	Offset Supply Leakage Current	$V_B=V_S=600$ V			50	$\mu$ A
$I_{QBS}$	Quiescent $V_{BS}$ Supply Current	$V_{IN}=0$ V or 5 V		45	80	$\mu$ A
$I_{QDD}$	Quiescent $V_{DD}$ Supply Current	$V_{IN}=0$ V or 5 V		75	110	$\mu$ A
$I_{PBS}$	Operating $V_{BS}$ Supply Current	$f_{IN}=20$ kHz, rms value		530	640	$\mu$ A
$I_{PDD}$	Operating $V_{DD}$ Supply Current	$f_{IN}=20$ kHz, rms value		530	640	$\mu$ A
<b>LOGIC INPUT SECTION (HIN, LIN)</b>						
$V_{IH}$	Logic "1" Input Voltage		2.5			V
$V_{IL}$	Logic "0" Input Voltage				1.2	V
$I_{IN+}$	Logic "1" Input Bias Current	$V_{IN}=5$ V		25	50	$\mu$ A
$I_{IN-}$	Logic "0" Input Bias Current	$V_{IN}=0$ V		1.0	2.0	$\mu$ A
$R_{IN}$	Input Pull-Down Resistance		100	200		K $\Omega$
<b>GATE DRIVER OUTPUT SECTION (HO, LO)</b>						
$V_{OH}$	High-Level Output Voltage, $V_{BIAS}-V_O$	No Load			1.0	V
$V_{OL}$	Low-Level Output Voltage, $V_O$	No Load			35	mV
$I_{O+}$	Output High, Short-Circuit Pulsed Current <sup>(4)</sup>	$V_O=0$ V, $V_{IN}=5$ V with $PW<10$ $\mu$ s	1.8	2.5		A
$I_{O-}$	Output Low, Short-Circuit Pulsed Current <sup>(4)</sup>	$V_O=15$ V, $V_{IN}=0$ V with $PW<10$ $\mu$ s	1.8	2.5		A
$V_S$	Allowable Negative $V_S$ Pin Voltage for HIN Signal Propagation to HO			-9.8	-7.0	V

**Note:**

4. This parameter guaranteed by design.

## Dynamic Electrical Characteristics

$V_{BIAS}$  ( $V_{DD}$ ,  $V_{BS}$ )=15.0 V,  $V_S$ =COM=0 V,  $C_L$ =1000 pF and  $T_A$ =25°C unless otherwise specified.

Symbol	Characteristics	Test Condition	Min.	Typ.	Max.	Unit
$t_{on}$	Turn-on Propagation Delay	$V_S=0$ V		140	200	ns
$t_{off}$	Turn-off Propagation Delay	$V_S=0$ V		140	200	ns
MT	Delay Matching, HS & LS Turn-on/off			0	50	ns
$t_r$	Turn-on Rise Time			25	50	ns
$t_f$	Turn-off Fall Time			20	45	ns

## Typical Characteristics

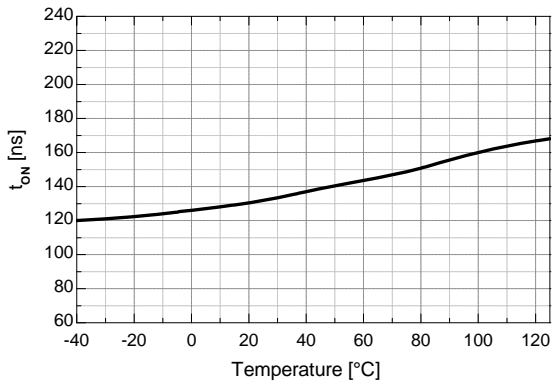


Figure 4. Turn-on Propagation Delay vs. Temperature

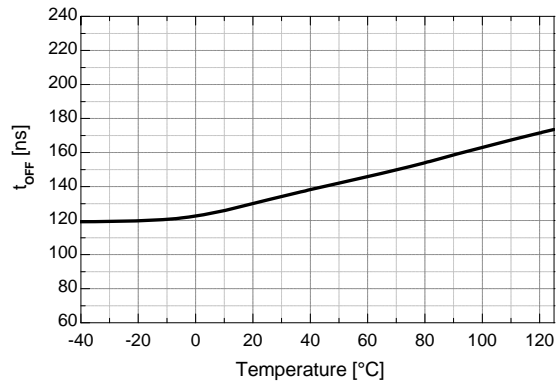


Figure 5. Turn-off Propagation Delay vs. Temperature

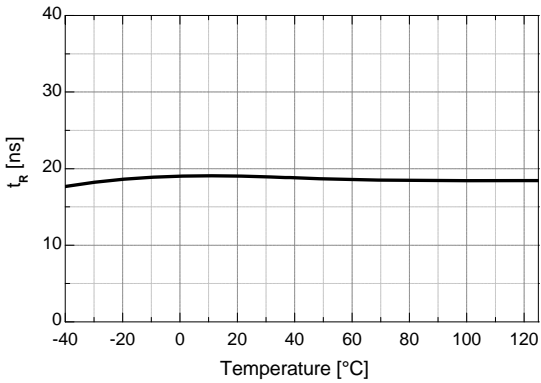


Figure 6. Turn-on Rise Time vs. Temperature

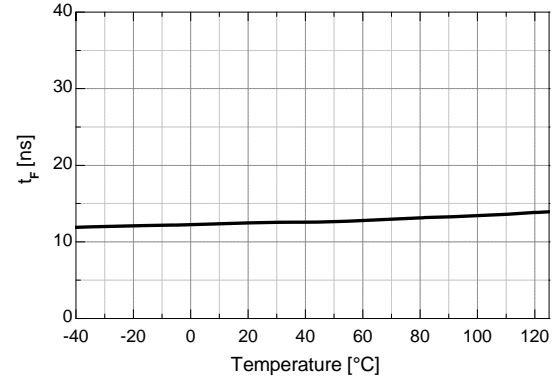


Figure 7. Turn-off Fall Time vs. Temperature

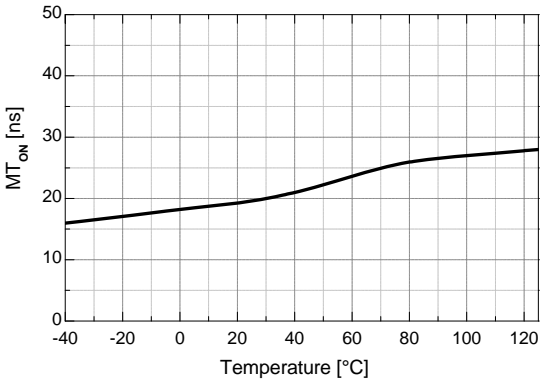


Figure 8. Turn-on Delay Matching vs. Temperature

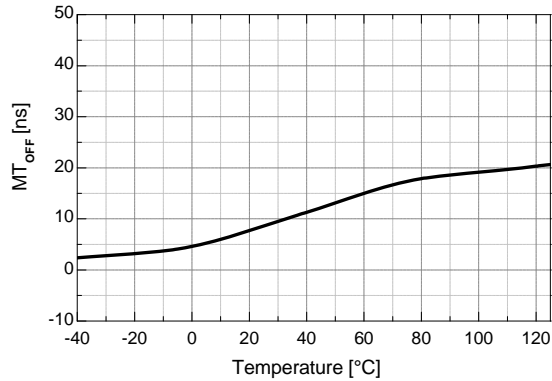


Figure 9. Turn-off Delay Matching vs. Temperature

Typical Characteristics (Continued)

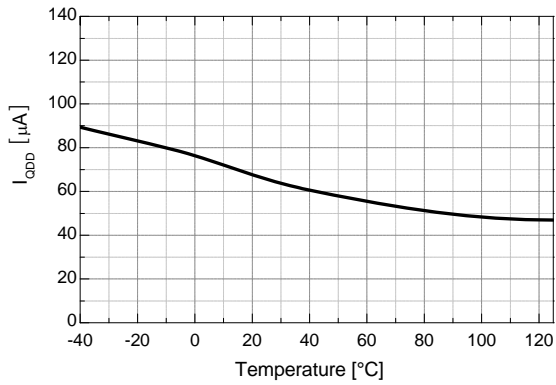


Figure 10. Quiescent  $V_{DD}$  Supply Current vs. Temperature

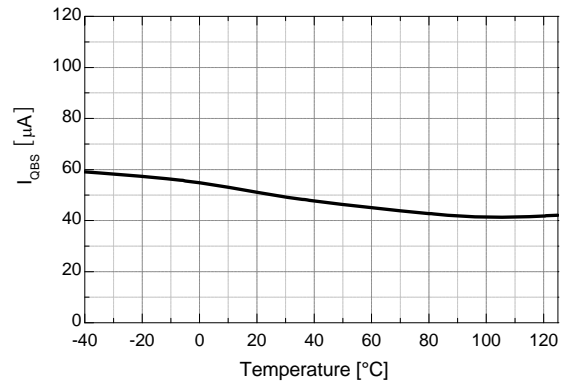


Figure 11. Quiescent  $V_{BS}$  Supply Current vs. Temperature

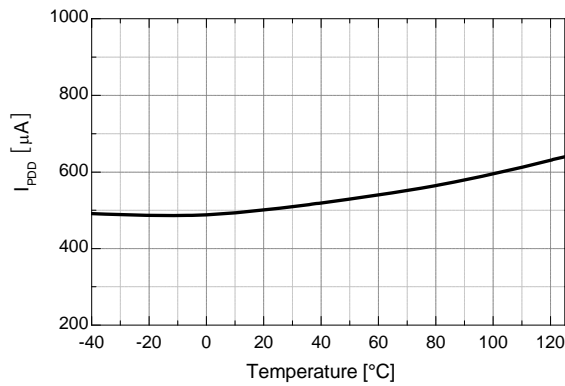


Figure 12. Operating  $V_{DD}$  Supply Current vs. Temperature

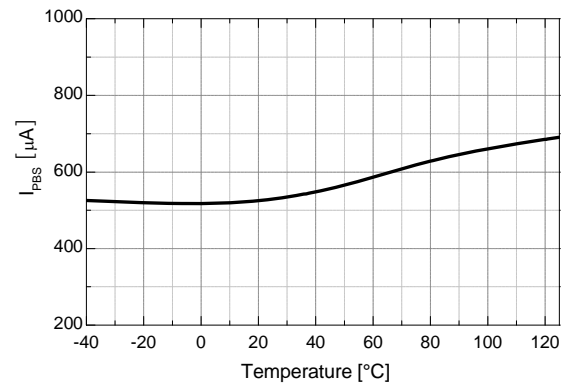


Figure 13. Operating  $V_{BS}$  Supply Current vs. Temperature

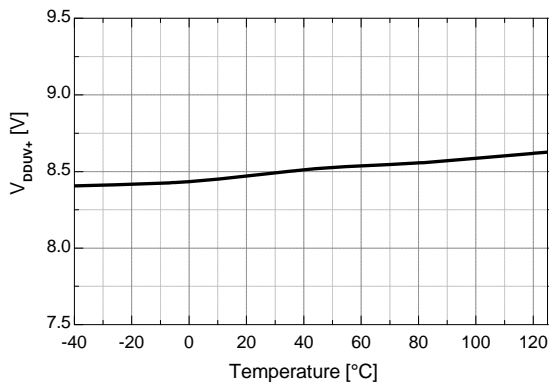


Figure 14.  $V_{DD}$  UVLO+ vs. Temperature

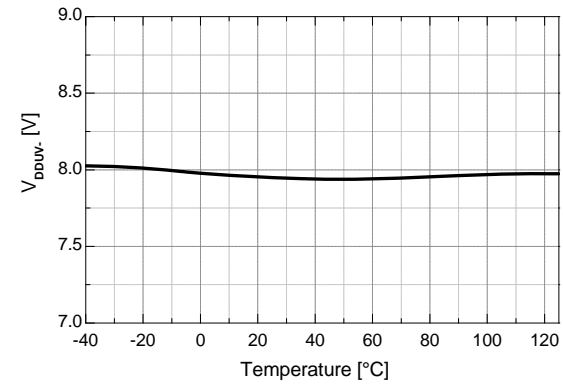


Figure 15.  $V_{DD}$  UVLO- vs. Temperature



Typical Characteristics (Continued)

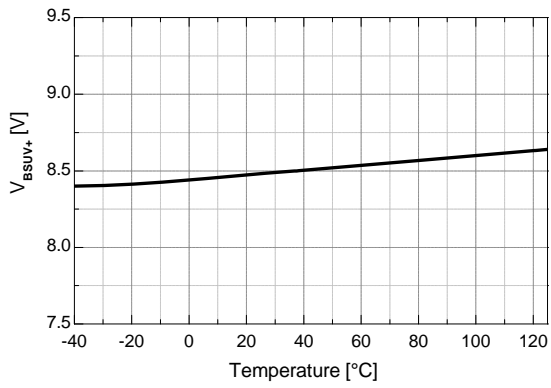


Figure 16.  $V_{BS}$  UVLO+ vs. Temperature

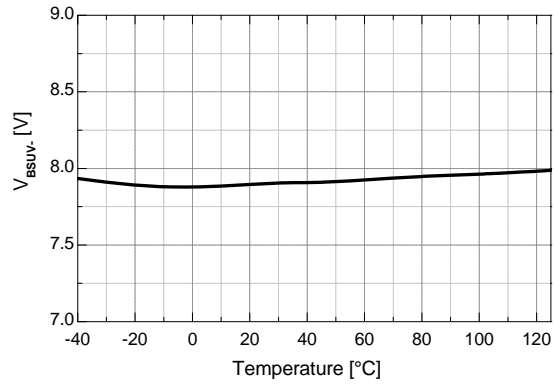


Figure 17.  $V_{BS}$  UVLO- vs. Temperature

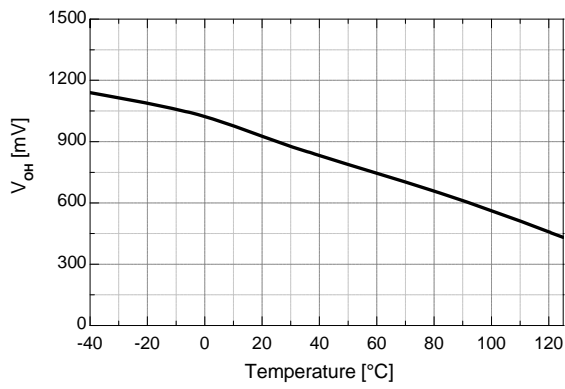


Figure 18. High-Level Output Voltage vs. Temperature

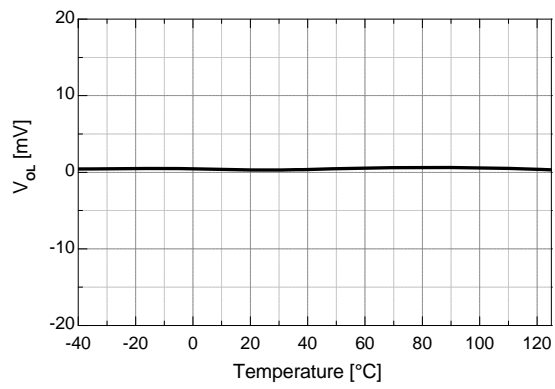


Figure 19. Low-Level Output Voltage vs. Temperature

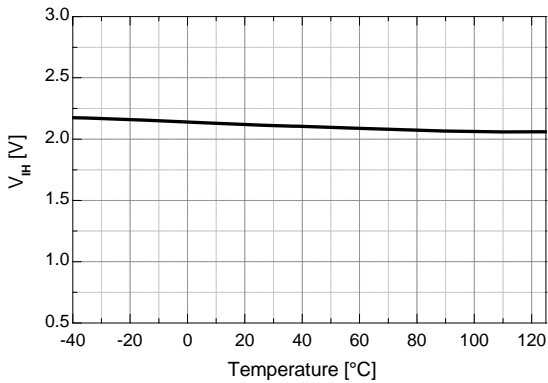


Figure 20. Logic High Input Voltage vs. Temperature

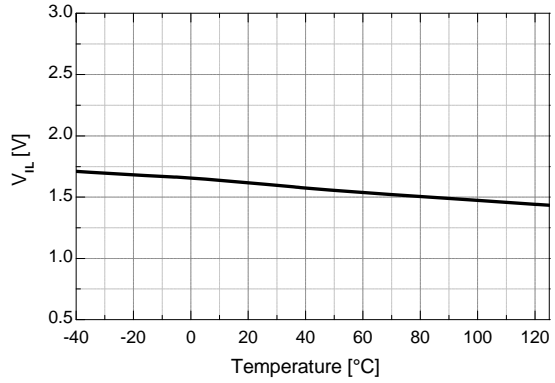


Figure 21. Logic Low Input Voltage vs. Temperature

Typical Characteristics (Continued)

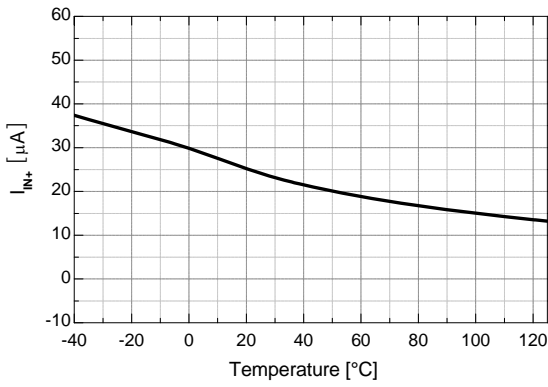


Figure 22. Logic Input High Bias Current vs. Temperature

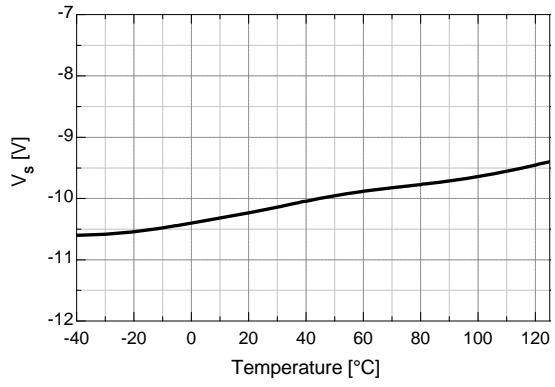


Figure 23. Allowable Negative  $V_S$  Voltage vs. Temperature

## Switching Time Definitions

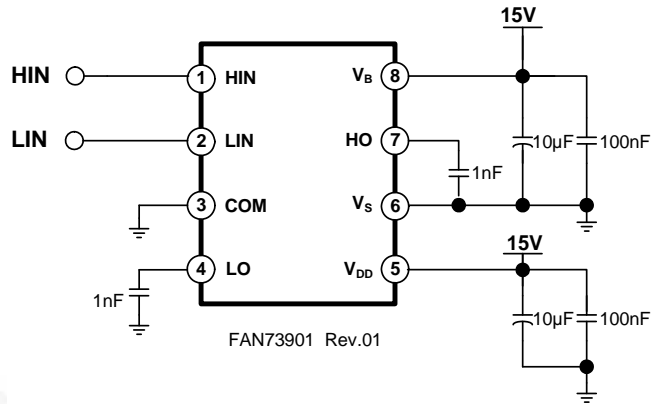


Figure 24. Switching Time Test Circuit

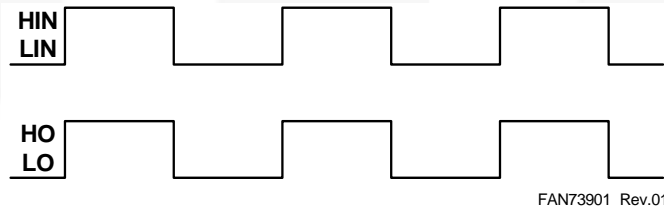


Figure 25. Input / Output Timing Diagram

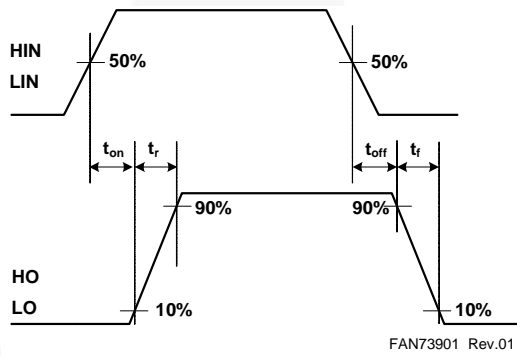


Figure 26. Switching Time Waveform Definitions

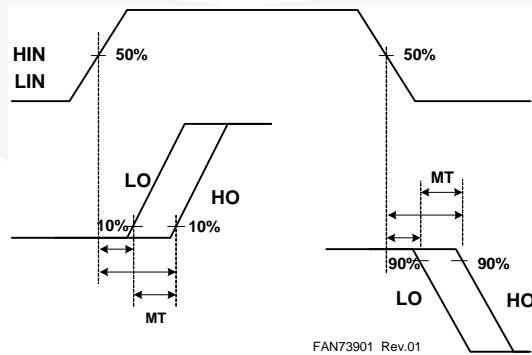
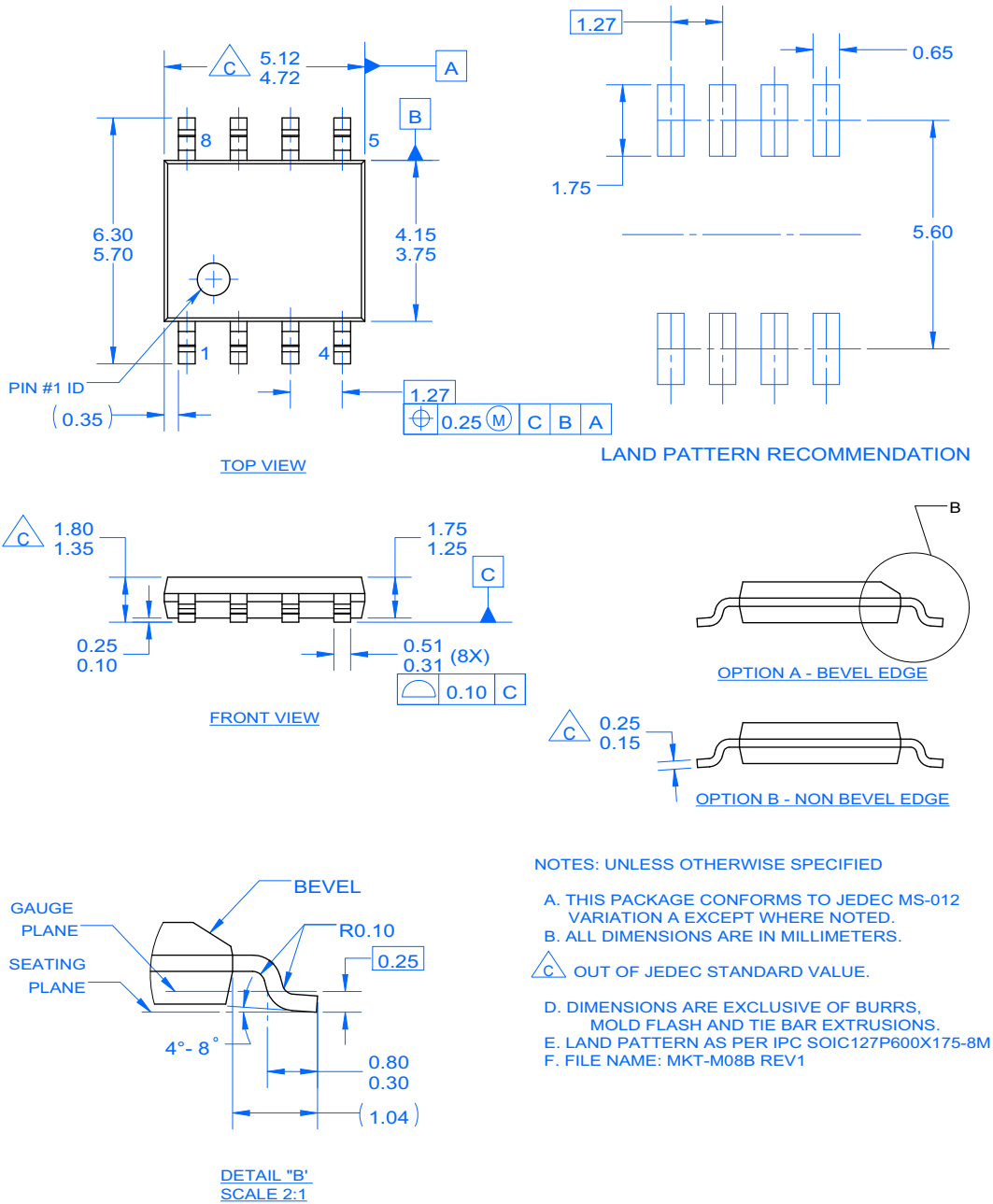


Figure 27. Delay Matching Waveform Definitions

**Mechanical Dimensions**



**Figure 28. 8-Lead Small Outline Package (SOP)**

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| Fairchild®               | MicroPak2™                                     | SuperSOT™-3                           | Ultra FRFET™     |
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Preliminary	First Production	Datasheet contains preliminary data; supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve design.
No Identification Needed	Full Production	Datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice to improve the design.
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