

MOSFET – N-Channel, SUPERFET®

600 V, 20 A, 190 mΩ

FCA20N60

Description

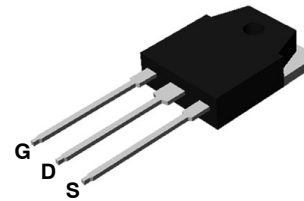
SUPERFET MOSFET is onsemi's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance, dv/dt rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.

Features

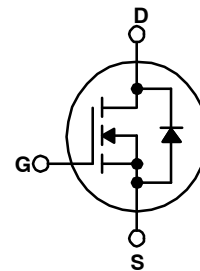
- 650 V @ $T_J = 150^\circ\text{C}$
- Typ. $R_{DS(on)} = 150\text{ m}\Omega$
- Ultra Low Gate Charge (Typ. $Q_g = 75\text{ nC}$)
- Low Effective Output Capacitance (Typ. $C_{oss(eff.)} = 165\text{ pF}$)
- 100% Avalanche Tested
- This Device is Pb-Free

Applications

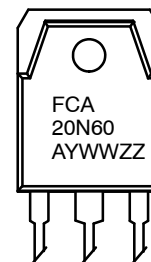
- Solar Inverter
- AC-DC Power Supply



TO-3P-3L
CASE 340BZ



MARKING DIAGRAM



FCA20N60 = Specific Device Code
A = Assembly Location
YWW = Date Code (Year and Week)
ZZ = Assembly Lot Code

ORDERING INFORMATION

Device	Package	Shipping [†]
FCA20N60	TO-3P-3L (Pb-Free)	450 Units / Tube
FCA20N60-F109	TO-3P-3L (Pb-Free)	450 Units / Tube

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FCA20N60

MOSFET MAXIMUM RATINGS

($T_C = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Value	Unit
V_{DSS}	Drain to Source Voltage	600	V
V_{GSS}	Gate-Source Voltage	± 30	V
I_D	Drain Current – Continuous ($T_C = 25^\circ\text{C}$) – Continuous ($T_C = 100^\circ\text{C}$)	20 12.5	A
I_{DM}	Drain Current – Pulsed (Note 1)	60	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)	690	mJ
I_{AR}	Avalanche Current (Note 1)	20	A
E_{AR}	Repetitive Avalanche Energy (Note 1)	20.8	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)	4.5	V/ns
P_D	Power Dissipation – ($T_C = 25^\circ\text{C}$) – Derate Above 25°C	208 1.67	W W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range	-55 to $+150$	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max	0.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	41.7	

ELECTRICAL CHARACTERISTICS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain–Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$, $T_J = 25^\circ\text{C}$	600	–	–	V
		$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$, $T_J = 150^\circ\text{C}$	–	650	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	–	0.6	–	V/°C
BV_{DS}	Drain–Source Avalanche Breakdown Voltage	$V_{GS} = 0\ \text{V}$, $I_D = 20\ \text{A}$	–	700	–	V
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 600\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	–	1	μA
		$V_{DS} = 480\ \text{V}$, $T_C = 125^\circ\text{C}$	–	–	10	
I_{GSS}	Gate to Body Leakage Current	$V_{GS} = \pm 30\ \text{V}$, $V_{DS} = 0\ \text{V}$	–	–	± 100	nA

On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250\ \mu\text{A}$	3.0	–	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 10\ \text{A}$	–	0.15	0.19	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\ \text{V}$, $I_D = 10\ \text{A}$	–	17	–	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 25\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	2370	3080	pF
C_{oss}	Output Capacitance		–	1280	1665	pF
C_{rss}	Reverse Transfer Capacitance		–	95	–	pF
C_{oss}	Output Capacitance	$V_{DS} = 480\ \text{V}$, $V_{GS} = 0\ \text{V}$, $f = 1\ \text{MHz}$	–	65	85	pF
$C_{oss(eff.)}$	Effective Output Capacitance	$V_{DS} = 0\ \text{V}$ to $400\ \text{V}$, $V_{GS} = 0\ \text{V}$	–	165	–	pF
Q_g	Total Gate Charge at 10 V	$V_{DS} = 480\ \text{V}$, $I_D = 20\ \text{A}$, $V_{GS} = 10\ \text{V}$ (Note 4)	–	75	98	nC
Q_{gs}	Gate to Source Charge		–	13.5	18	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	36	–	nC

Switching Characteristics

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = 300\ \text{V}$, $I_D = 20\ \text{A}$, $V_{GS} = 10\ \text{V}$, $R_G = 25\ \Omega$ (Note 4)	–	62	135	ns
t_r	Turn–On Rise Time		–	140	290	ns
$t_{d(off)}$	Turn–Off Delay Time		–	230	470	ns
t_f	Turn–Off Fall Time		–	65	140	ns

Drain–Source Diode Characteristics and Maximum Ratings

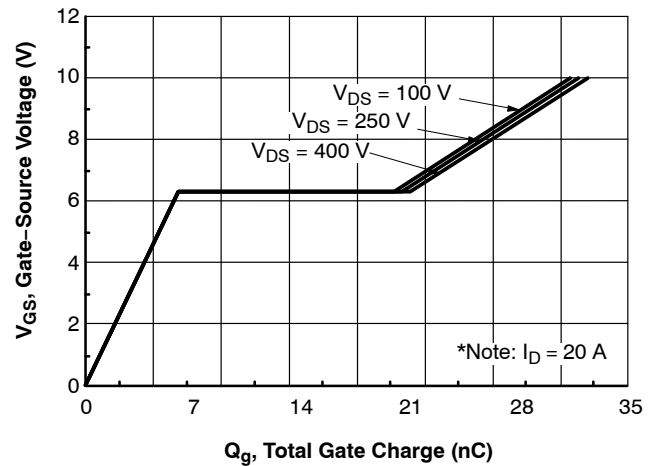
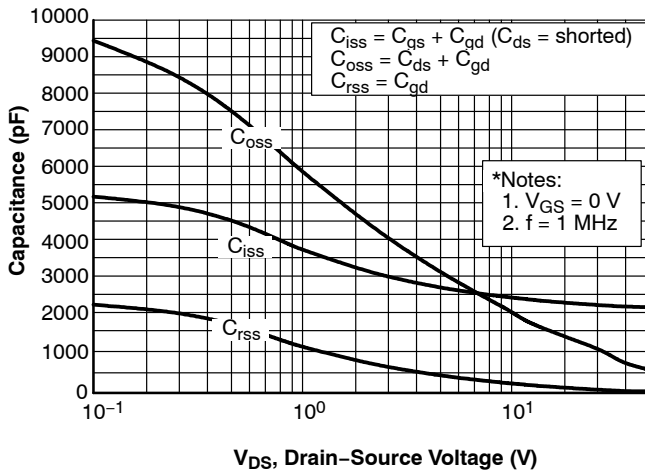
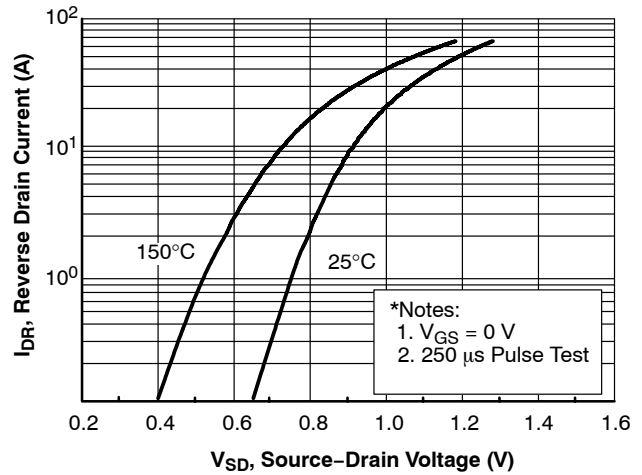
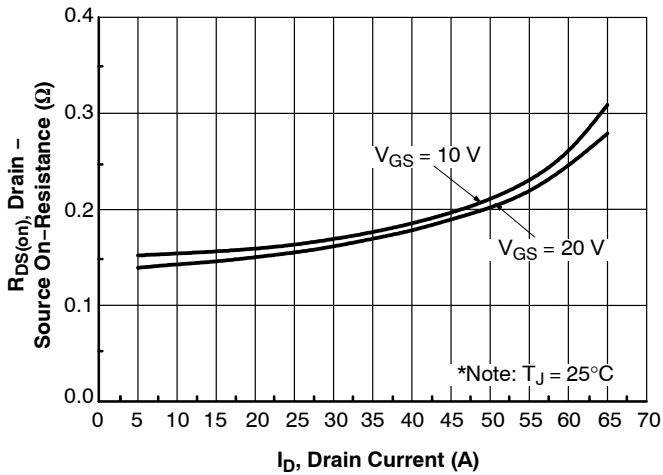
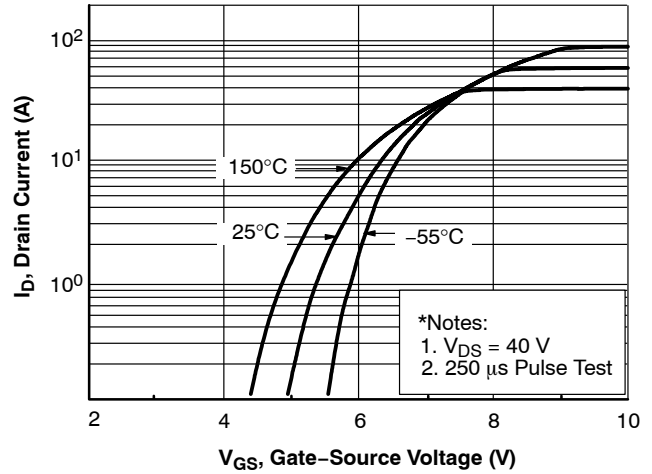
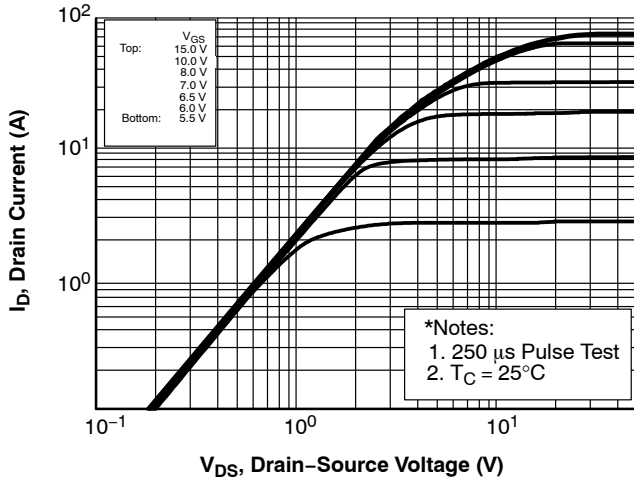
I _S	Maximum Continuous Drain to Source Diode Forward Current		–	–	20	A
I _{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	60	A
V _{SD}	Drain–Source Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 20 A	–	–	1.4	V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, I _{SD} = 20 A, dI _F /dt = 100 A/μs	–	530	–	ns
Q _{rr}	Reverse Recovery Charge		–	10.5	–	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. Repetitive Rating: Pulse width–limited by maximum junction temperature.
2. $I_{AS} = 10\ \text{A}$, $V_{DD} = 50\ \text{V}$, $R_G = 25\ \Omega$, starting $T_J = 25^\circ\text{C}$.
3. $I_{SD} \leq 20\ \text{A}$, $di/dt \leq 200\ \text{A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
4. Essentially independent of operating temperature typical Characteristics.

TYPICAL CHARACTERISTICS



TYPICAL CHARACTERISTICS (CONTINUED)

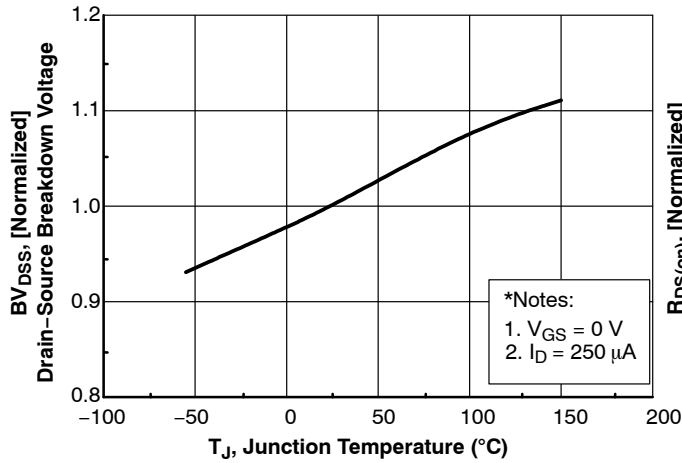


Figure 7. Breakdown Voltage Variation vs Temperature

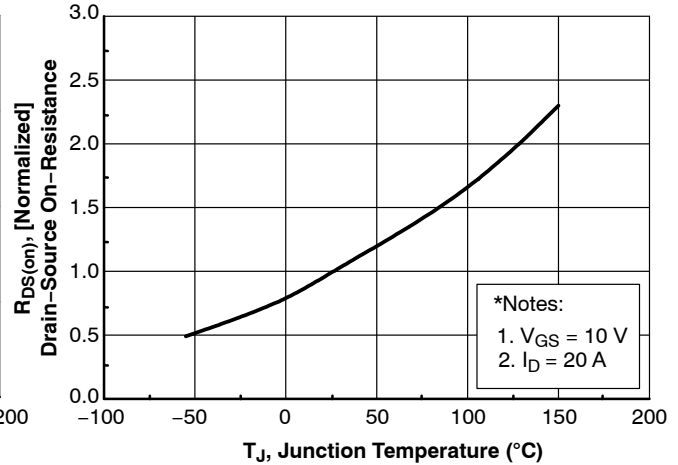


Figure 8. On-Resistance Variation vs Temperature

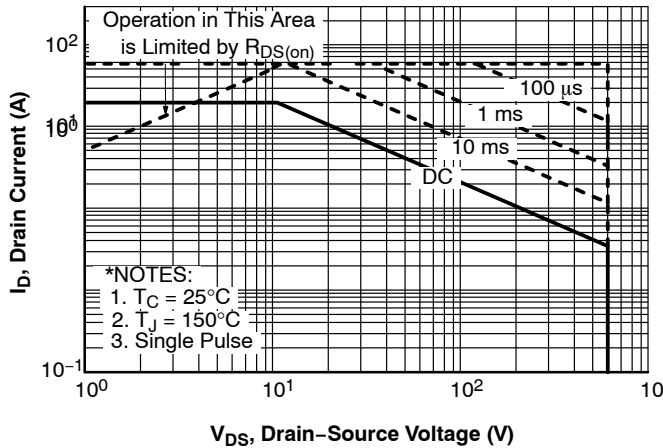


Figure 9. Maximum Safe Operating Area

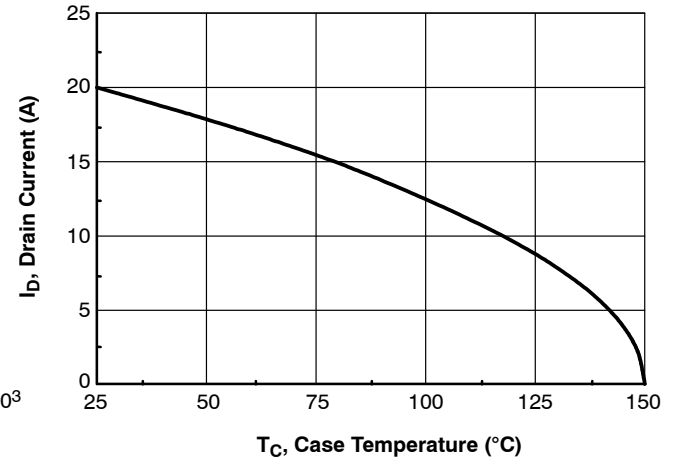


Figure 10. Maximum Drain Current vs. Case Temperature

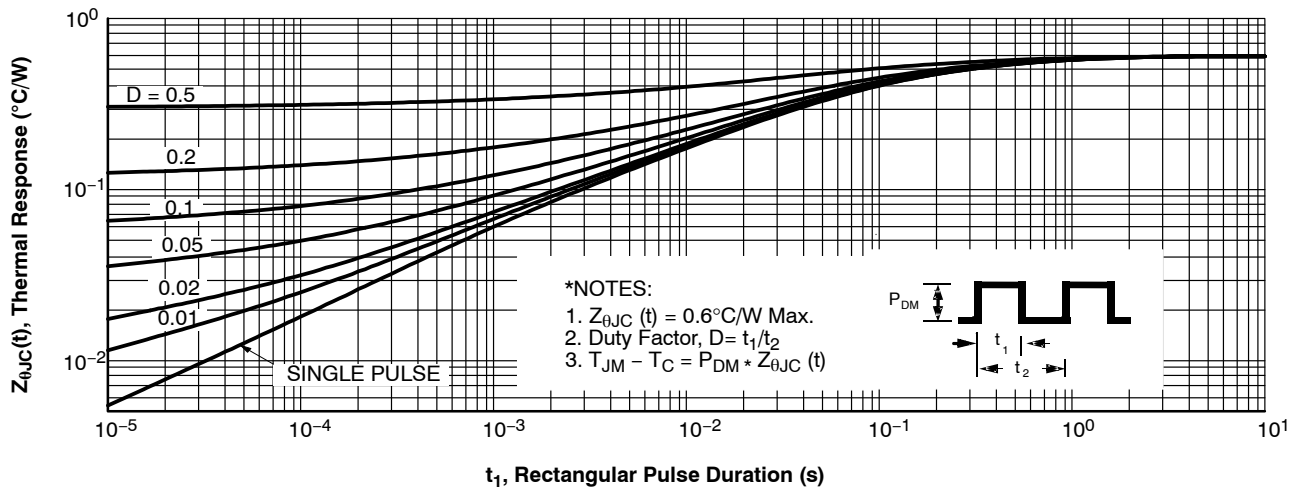


Figure 11. Transient Thermal Response Curve

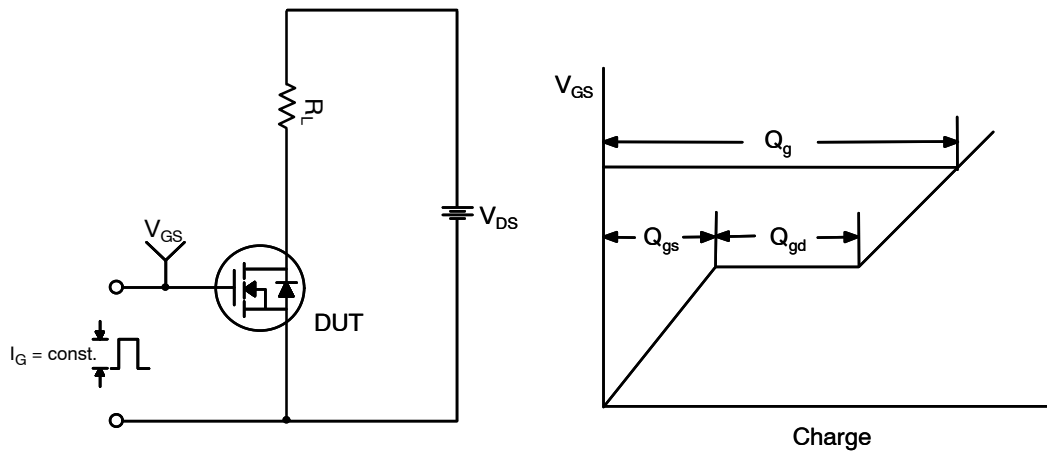


Figure 12. Gate Charge Test Circuit & Waveform

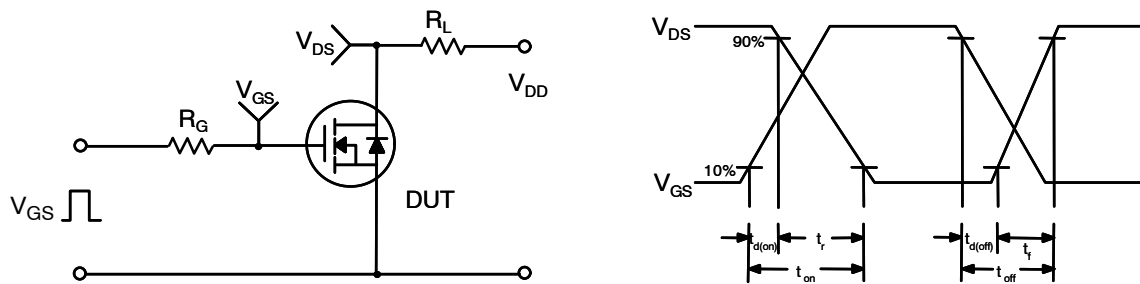


Figure 13. Resistive Switching Test Circuit & Waveforms

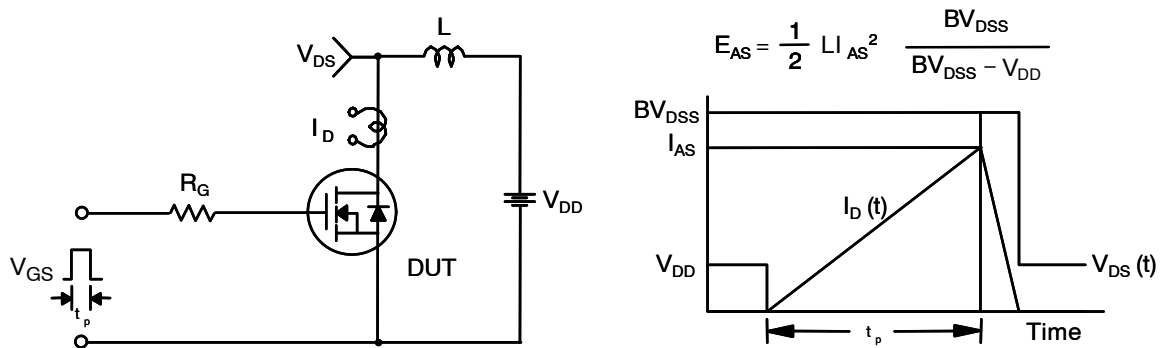


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FCA20N60

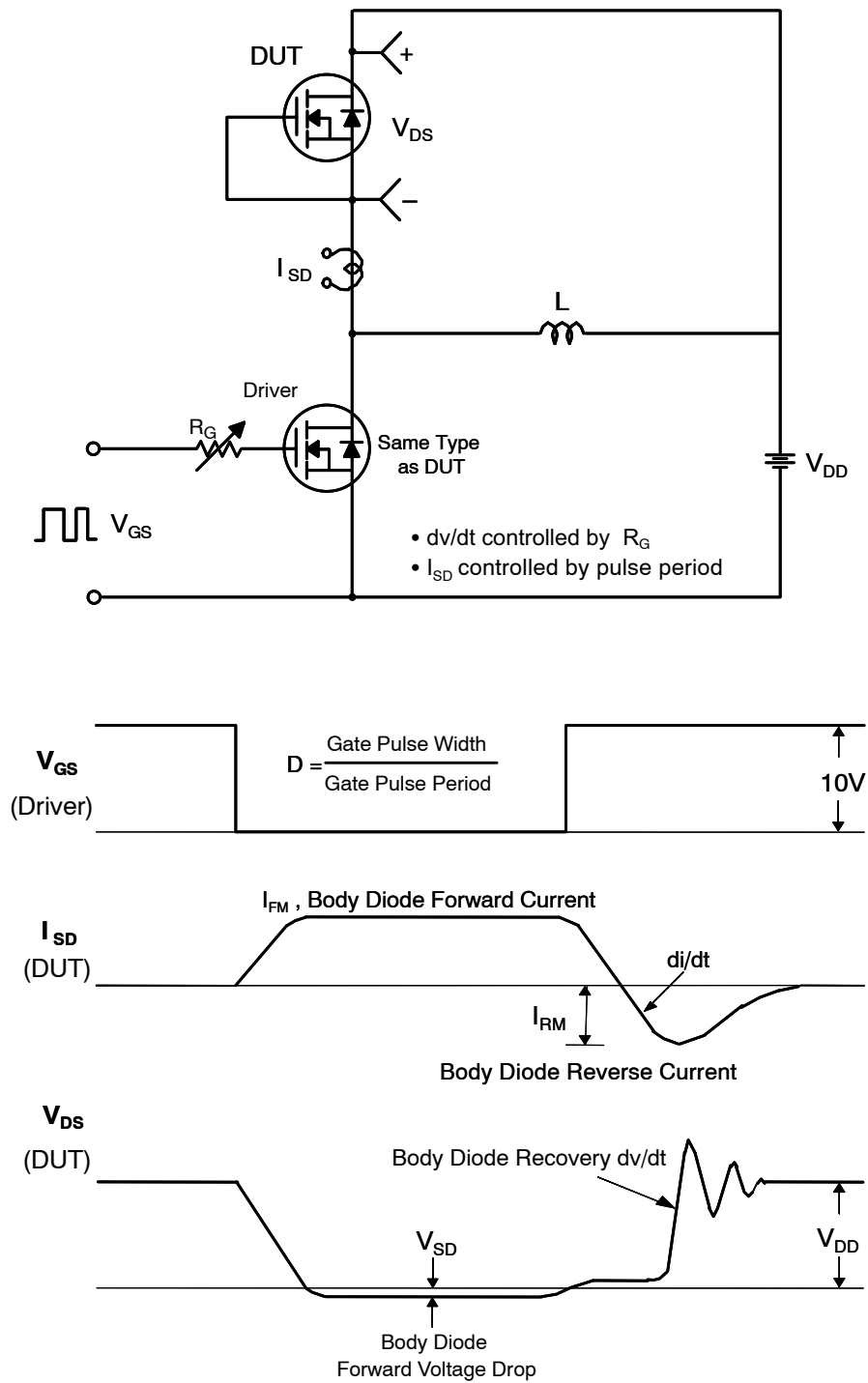
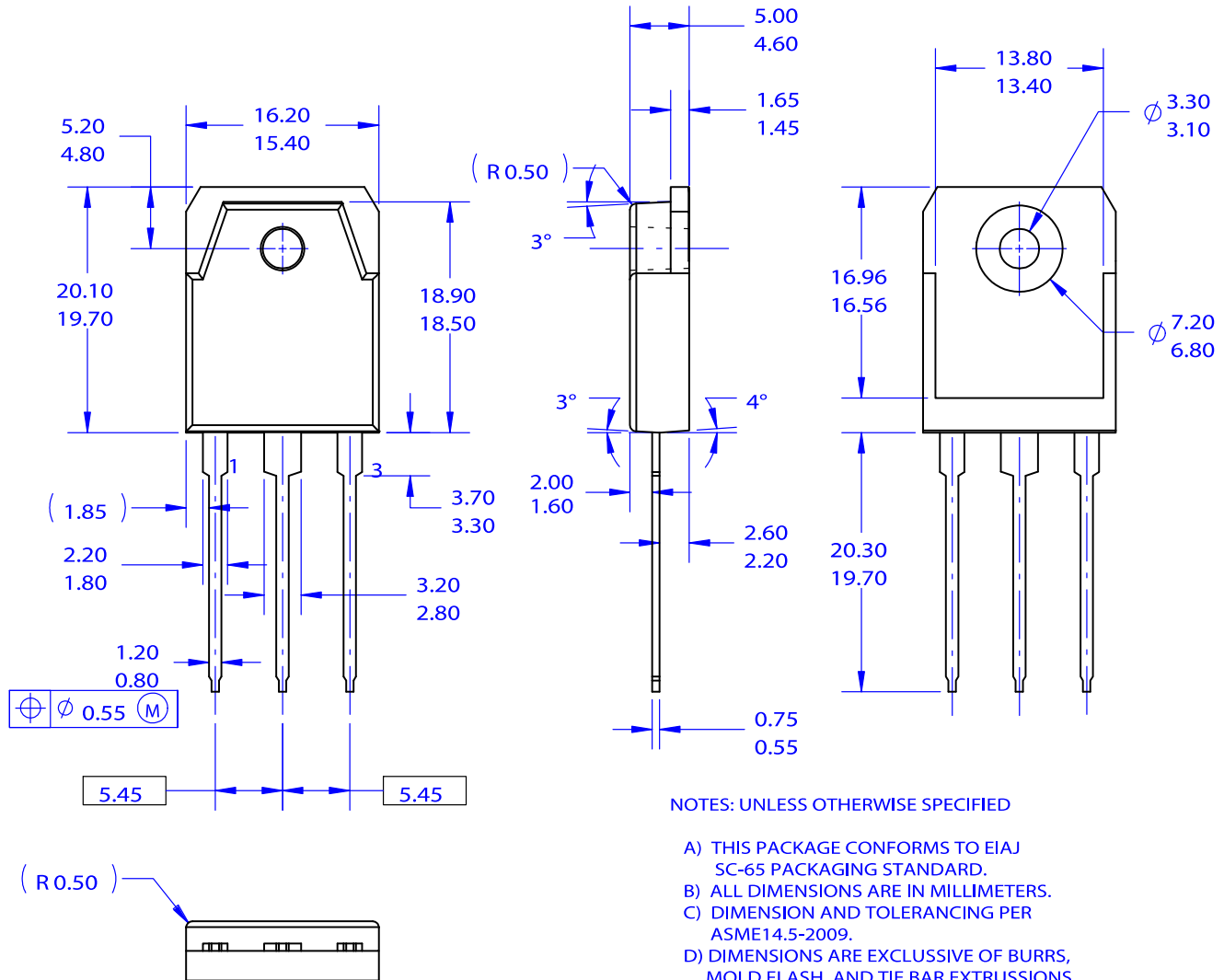


Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ
ISSUE O

DATE 31 OCT 2016



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