MOSFET – Power, N-Channel, SUPERFET[®] III, Easy Drive

650 V, 24 A, 125 m Ω

FCH125N65S3R0

Description

SUPERFET III MOSFET is **onsemi**'s brand-new high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This advanced technology is tailored to minimize conduction loss, provide superior switching performance, and withstand extreme dv/dt rate. Consequently, SUPERFET III MOSFET Easy drive series helps manage EMI issues and allows for easier design implementation.

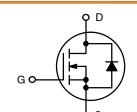
Features

- 700 V @ T_J = 150°C
- Typ. $R_{DS(on)} = 105 \text{ m}\Omega$
- Ultra Low Gate Charge (Typ. Q_g = 46 nC)
- Low Effective Output Capacitance (Typ. C_{oss(eff.)} = 439 pF)
- 100% Avalanche Tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- Telecom / Server Power Supplies
- Industrial Power Supplies
- UPS / Solar

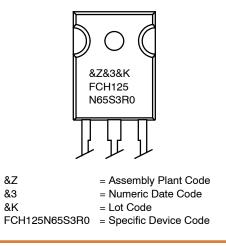
V _{DSS}	R _{DS(ON)} MAX	I _D MAX
650 V	125 m Ω @ 10 V	24 A



N-Channel MOSFET



MARKING DIAGRAM



ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

Symbol	Paramet	er	Value	Unit	
V _{DSS}	Drain to Source Voltage		650	V	
V _{GSS}	Gate to Source Voltage	DC	±30	V	
		AC (f > 1 Hz)	±30	V	
Ι _D	Drain Current	Continuous (T _C = 25°C)	24	A	
		Continuous (T _C = 100°C)	15		
I _{DM}	Drain Current	Pulsed (Note 1)	60	А	
E _{AS}	Single Pulsed Avalanche Energy (Note 2)		115	mJ	
I _{AS}	Avalanche Current (Note 2)		3.7	А	
E _{AR}	Repetitive Avalanche Energy (Note 1)		1.81	mJ	
dv/dt	MOSFET dv/dt		100	V/ns	
	Peak Diode Recovery dv/dt (Note 3)		20	1	
PD	Power Dissipation	(T _C = 25°C)	181	W	
	Derate Above 25°C		1.45	W/°C	
T _J , T _{STG}	Operating and Storage Temperature Rang	e	–55 to +150	°C	
ΤL	Maximum Lead Temperature for Soldering	, 1/8″ from Case for 5 s	300	°C	

ABSOLUTE MAXIMUM RATINGS (T_C = 25°C, Unless otherwise specified)

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected. 1. Repetitive rating: pulse-width limited by maximum junction temperature. 2. $I_{AS} = 3.7 \text{ A}, R_G = 25 \Omega$, starting $T_J = 25^{\circ}\text{C}$. 3. $I_{SD} \le 12 \text{ A}, \text{ di/dt} \le 200 \text{ A/}\mu\text{s}, \text{V}_{DD} \le 400 \text{ V}, \text{ starting } T_J = 25^{\circ}\text{C}$.

THERMAL CHARACTERISTICS

Symbol Parameter		Value	Unit
$R_{ ext{ heta}JC}$	Thermal Resistance, Junction to Case, Max.	0.69	°C/W
$R_{ hetaJA}$	Thermal Resistance, Junction to Ambient, Max.	40	C/W

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Marking	Package	Quantity
FCH125N65S3R0-F155	FCH125N65S3R0	TO-247-3LD (Pb-Free)	30 Units / Tube



ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Тур	Max	Unit
OFF CHARACT	TERISTICS	-				
BV _{DSS}	Drain to Source Breakdown Voltage	V_{GS} = 0 V, I_D = 1 mA, T_J = 25°C	650			V
		V_{GS} = 0 V, I_D = 1 mA, T_J = 150°C	700			V
$\Delta \text{BV}_{\text{DSS}} / \Delta \text{T}_{\text{J}}$	Breakdown Voltage Temperature Coefficient	$I_D = 1$ mA, Referenced to 25°C		0.68		V/°C
I _{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 650 \text{ V}, V_{GS} = 0 \text{ V}$			1	μΑ
		V_{DS} = 520 V, T_{C} = 125°C		1.35		
I _{GSS}	Gate to Body Leakage Current	V_{GS} = ±30 V, V_{DS} = 0 V			±100	nA
	, ,					

V _{GS(th)}	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_{D} = 0.59 \text{ mA}$	2.5		4.5	V
R _{DS(on)}	Static Drain to Source On Resistance	V_{GS} = 10 V, I _D = 12 A		105	125	mΩ
9 _{FS}	Forward Transconductance	V_{DS} = 20 V, I _D = 12 A		16		S

DYNAMIC CHARACTERISTICS

C _{iss}	Input Capacitance	V_{DS} = 400 V, V_{GS} = 0 V, f = 1 MHz	1940	pF
C _{oss}	Output Capacitance		40	pF
C _{oss(eff.)}	Effective Output Capacitance	$V_{DS} = 0$ V to 400 V, $V_{GS} = 0$ V	439	pF
C _{oss(er.)}	Energy Related Output Capacitance	$V_{DS} = 0$ V to 400 V, $V_{GS} = 0$ V	62	pF
Q _{g(tot)}	Total Gate Charge at 10V	$V_{DS} = 400 \text{ V}, \text{ I}_{D} = 12 \text{ A}, \text{ V}_{GS} = 10 \text{ V}$	46	nC
Q _{gs}	Gate to Source Gate Charge	(Note 4)	12	nC
Q _{gd}	Gate to Drain "Miller" Charge	1	19	nC
ESR	Equivalent Series Resistance	f = 1 MHz	0.5	Ω

SWITCHING CHARACTERISTICS

t _{d(on)}	Turn-On Delay Time	$V_{DD} = 400 \text{ V}, \text{ I}_{D} = 12 \text{ A},$	21	ns
t _r	Turn-On Rise Time	$V_{GS} = 10 \text{ V}, \text{ R}_{g} = 4.7 \Omega$ (Note 4)	19	ns
t _{d(off)}	Turn-Off Delay Time		48	ns
t _f	Turn-Off Fall Time		4.6	ns

SOURCE-DRAIN DIODE CHARACTERISTICS

۱ _S	Maximum Continuous Source to Drain Diode Forward Current			24	А
I _{SM}	Maximum Pulsed Source to Drain Diode Forward Current			60	Α
V _{SD}	Source to Drain Diode Forward Voltage	V _{GS} = 0 V, I _{SD} = 12 A		1.2	V
t _{rr}	Reverse Recovery Time	$V_{DD} = 400 \text{ V}, \text{ I}_{SD} = 12 \text{ A}, \text{ dI}_{\text{F}}/\text{dt} = 100 \text{ A}/\mu\text{s}$	339		ns
Q _{rr}	Reverse Recovery Charge		5.7		μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.



TYPICAL PERFORMANCE CHARACTERISTICS

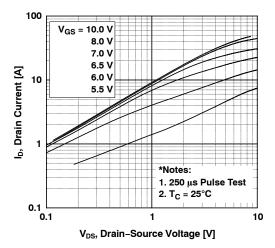


Figure 1. On-Region Characteristics

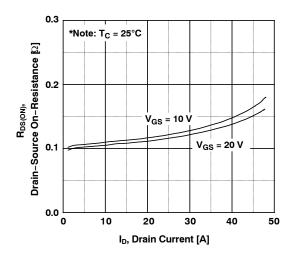


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

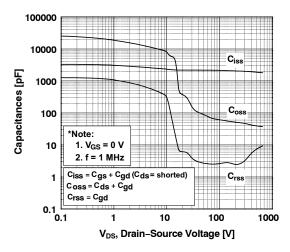


Figure 5. Capacitance Characteristics

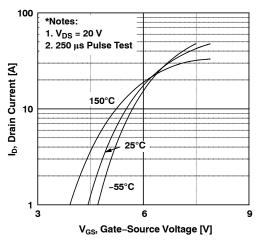


Figure 2. Transfer Characteristics

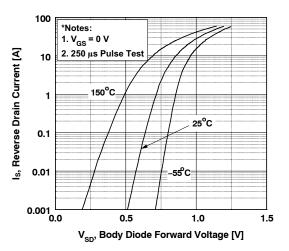


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

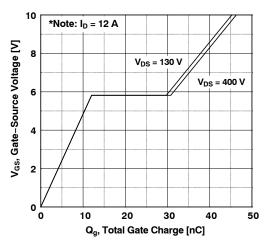


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

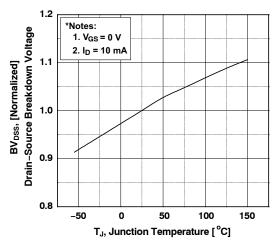


Figure 7. Breakdown Voltage Variation vs. Temperature

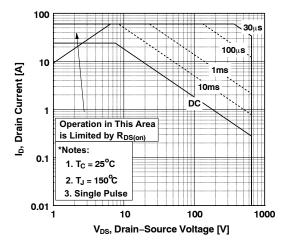


Figure 9. Maximum Safe Operation Area

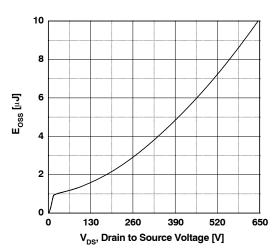


Figure 11. E_{OSS} vs. Drain to Source Voltage

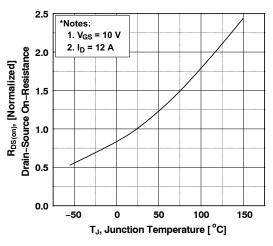


Figure 8. On-Resistance Variant vs. Temperature

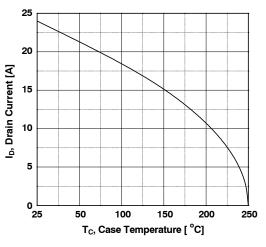


Figure 10. Maximum Drain Current vs. Case Temperature



TYPICAL PERFORMANCE CHARACTERISTICS (Continued)

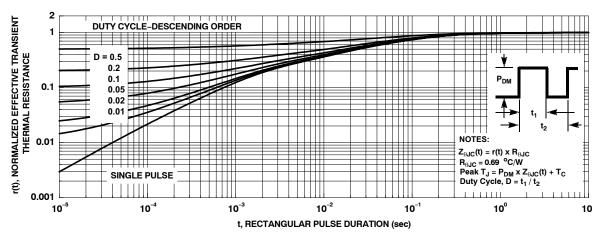


Figure 12. Transient Thermal Response Curve



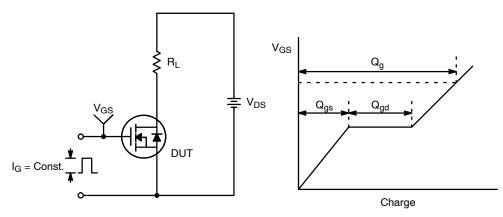


Figure 13. Gate Charge Test Circuit & Waveform

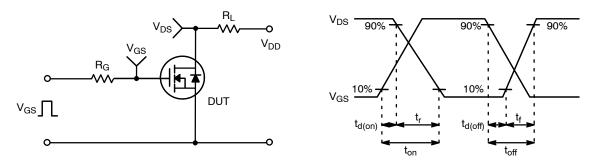


Figure 14. Resistive Switching Test Circuit & Waveforms

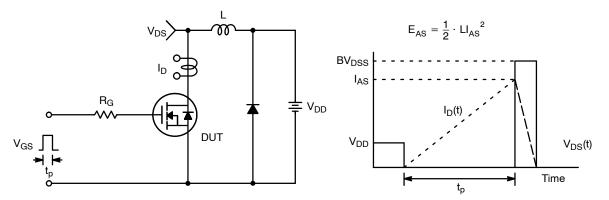


Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms



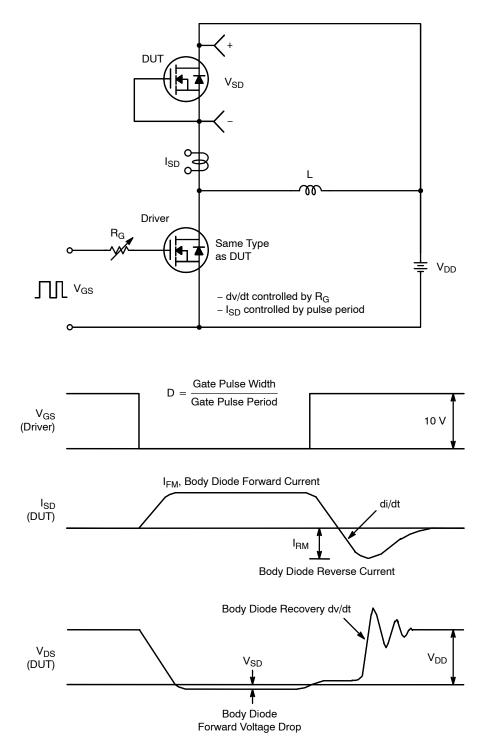


Figure 16. Peak Diode Recovery dt/dt Test Circuit & Waveforms

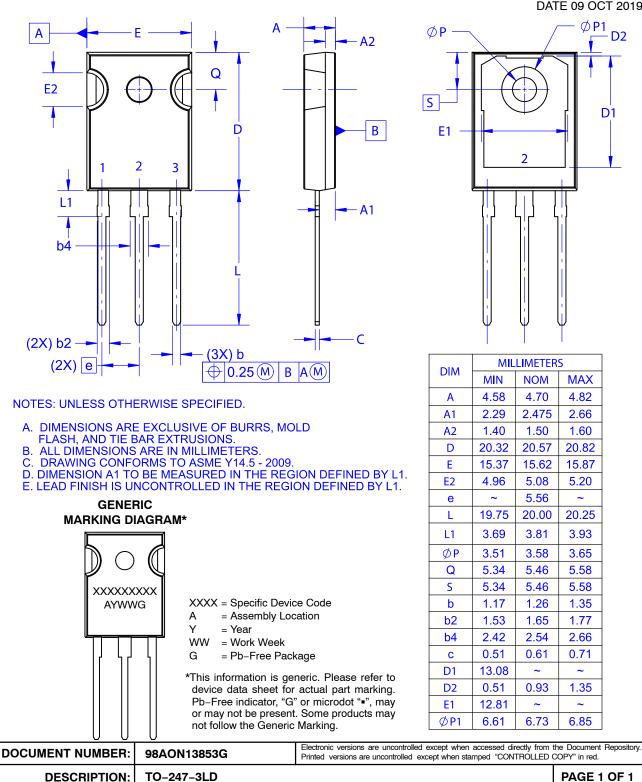
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