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June 2014

# FDA20N50F

## N-Channel UniFET™ FRFET® MOSFET

500 V, 22 A, 260 mΩ

### Features

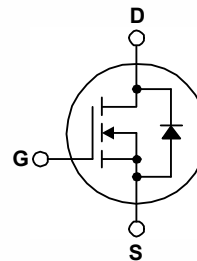
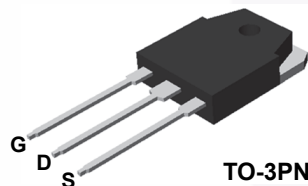
- $R_{DS(on)} = 220 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 11 \text{ A}$
- Low Gate Charge (Typ. 50 nC)
- Low  $C_{rss}$  (Typ. 27 pF)
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

### Applications

- PDP TV
- Uninterruptible Power Supply
- AC-DC Power Supply

### Description

UniFET™ MOSFET is Fairchild Semiconductor's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. The body diode's reverse recovery performance of UniFET FRFET® MOSFET has been enhanced by lifetime control. Its trr is less than 100nsec and the reverse dv/dt immunity is 15V/ns while normal planar MOSFETs have over 200nsec and 4.5V/nsec respectively. Therefore, it can remove additional component and improve system reliability in certain applications in which the performance of MOSFET's body diode is significant. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FDA20N50F	Unit
$V_{DSS}$	Drain to Source Voltage	500	V
$V_{GSS}$	Gate to Source Voltage	$\pm 30$	V
$I_D$	Drain Current	- Continuous ( $T_C = 25^\circ\text{C}$ )	22
		- Continuous ( $T_C = 100^\circ\text{C}$ )	13
$I_{DM}$	Drain Current	- Pulsed (Note 1)	88
$E_{AS}$	Single Pulsed Avalanche Energy	(Note 2)	1110
$I_{AR}$	Avalanche Current	(Note 1)	22
$E_{AR}$	Repetitive Avalanche Energy	(Note 1)	39
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	20
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	388
		- Derate above $25^\circ\text{C}$	3.1
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering Purpose, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FDA20N50F	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.44	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	40	

FDA20N50F — N-Channel UniFET™ FRFET® MOSFET

## Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDA20N50F	FDA20N50F	TO-3PN	Tube	N/A	30 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Unit
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### Off Characteristics

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}, T_J = 25^\circ\text{C}$	500	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$ , Referenced to $25^\circ\text{C}$	-	0.6	-	V/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 500\text{V}, V_{GS} = 0\text{V}$	-	-	10	$\mu\text{A}$
		$V_{DS} = 400\text{V}, T_C = 125^\circ\text{C}$	-	-	100	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 30\text{V}, V_{DS} = 0\text{V}$	-	-	$\pm 100$	nA

### On Characteristics

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 11\text{A}$	-	0.22	0.26	$\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 40\text{V}, I_D = 11\text{A}$	-	24	-	S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 25\text{V}, V_{GS} = 0\text{V}$ $f = 1\text{MHz}$	-	2550	3390	pF
$C_{oss}$	Output Capacitance		-	350	465	pF
$C_{rss}$	Reverse Transfer Capacitance		-	27	40	pF
$Q_{g(tot)}$	Total Gate Charge at 10V	$V_{DS} = 400\text{V}, I_D = 20\text{A}$ $V_{GS} = 10\text{V}$	-	50	65	nC
$Q_{gs}$	Gate to Source Gate Charge		-	14	-	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		(Note 4)	-	20	-

### Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 250\text{V}, I_D = 20\text{A}$ $R_G = 25\Omega$	-	45	100	ns
$t_r$	Turn-On Rise Time		-	120	250	ns
$t_{d(off)}$	Turn-Off Delay Time		-	100	210	ns
$t_f$	Turn-Off Fall Time		(Note 4)	-	60	130

### Drain-Source Diode Characteristics

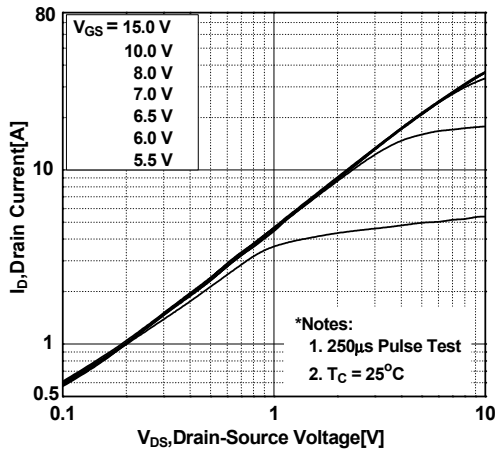
$I_S$	Maximum Continuous Drain to Source Diode Forward Current	-	-	22	A	
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current	-	-	88	A	
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0\text{V}, I_{SD} = 22\text{A}$	-	-	1.5	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0\text{V}, I_{SD} = 20\text{A}$ $di_F/dt = 100\text{A}/\mu\text{s}$	-	154	-	ns
$Q_{rr}$	Reverse Recovery Charge		-	0.5	-	$\mu\text{C}$

#### Notes:

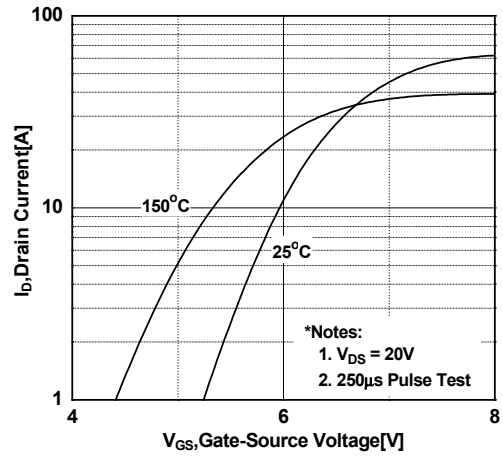
- 1: Repetitive Rating: Pulse width limited by maximum junction temperature
- 2:  $L = 5\text{mH}, I_{AS} = 20\text{A}, V_{DD} = 50\text{V}, R_G = 25\Omega$ , Starting  $T_J = 25^\circ\text{C}$
- 3:  $I_{SD} \leq 22\text{A}, di/dt \leq 200\text{A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , Starting  $T_J = 25^\circ\text{C}$
- 4: Essentially Independent of Operating Temperature Typical Characteristics

## Typical Characteristics

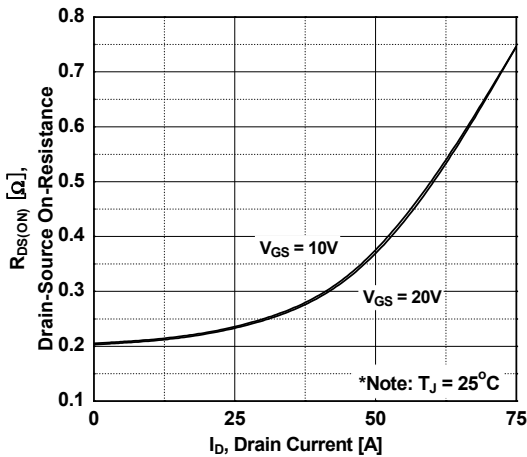
**Figure 1. On-Region Characteristics**



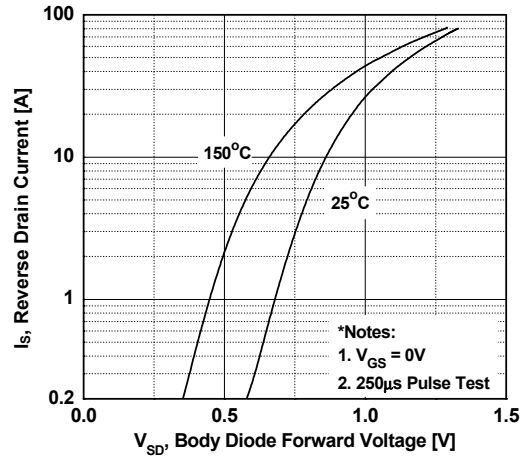
**Figure 2. Transfer Characteristics**



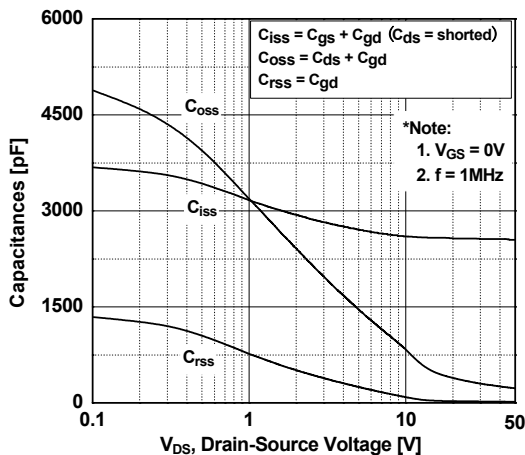
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



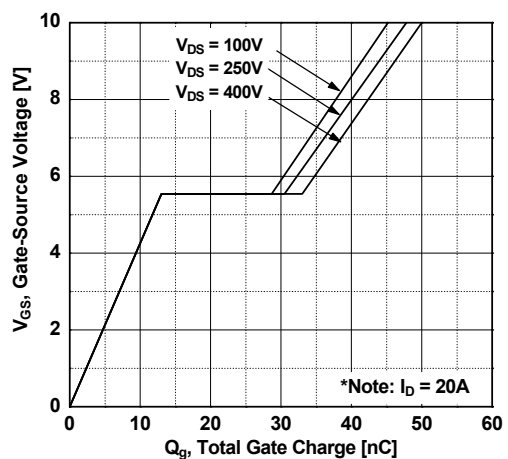
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

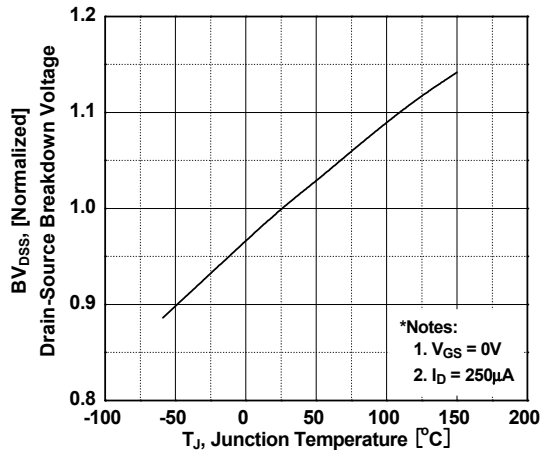


Figure 8. Maximum Safe Operating Area

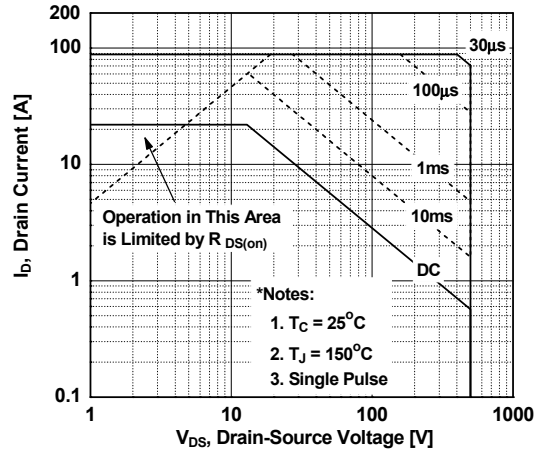


Figure 9. Maximum Drain Current vs. Case Temperature

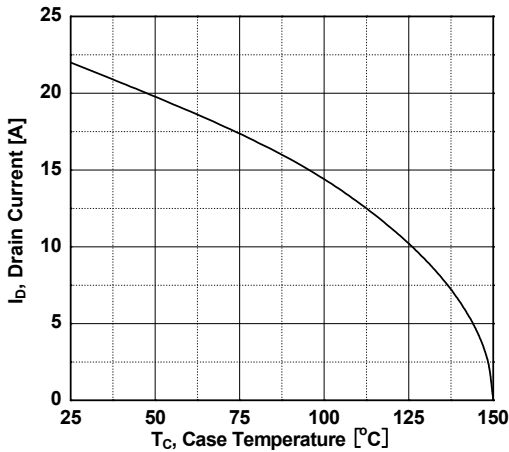
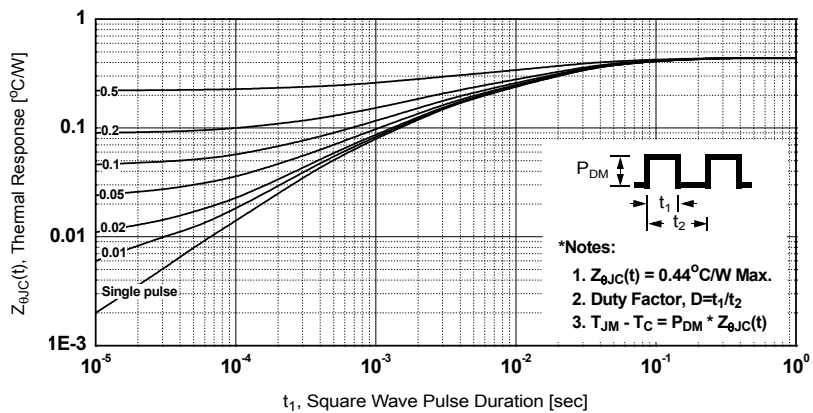
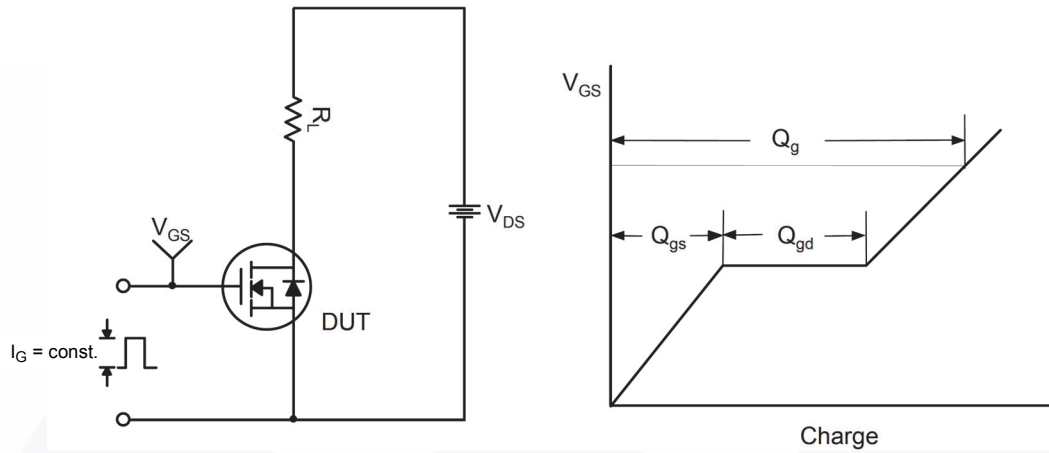


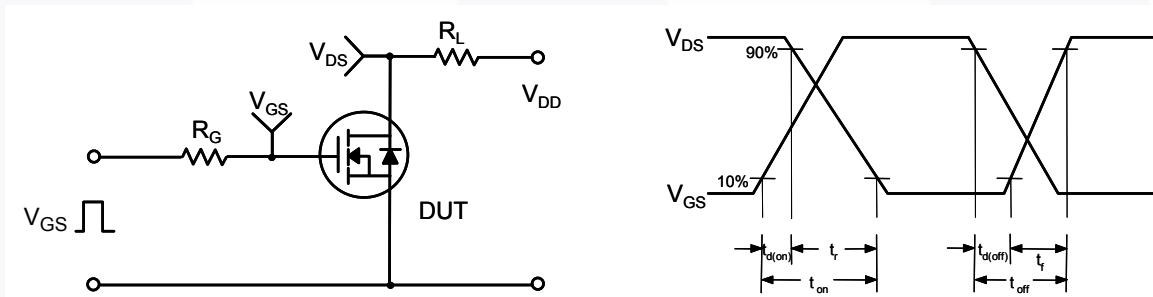
Figure 10. Transient Thermal Response Curve



**Figure 11. Gate Charge Test Circuit & Waveform**



**Figure 12. Resistive Switching Test Circuit & Waveforms**



**Figure 13. Unclamped Inductive Switching Test Circuit & Waveforms**

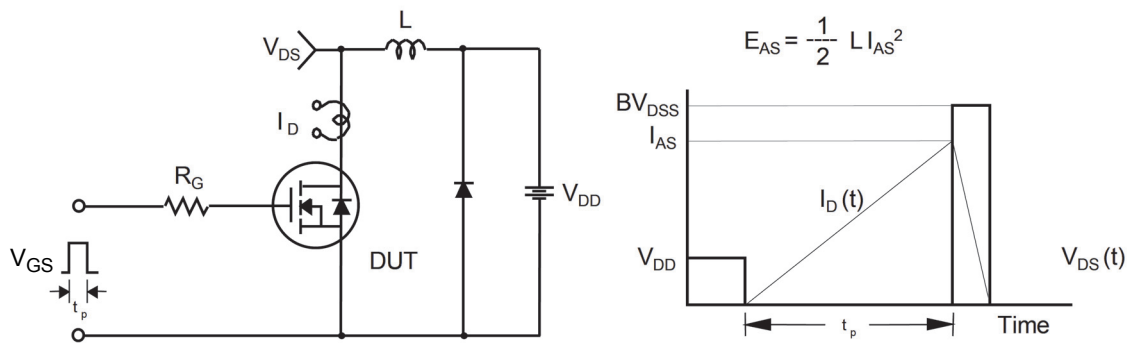
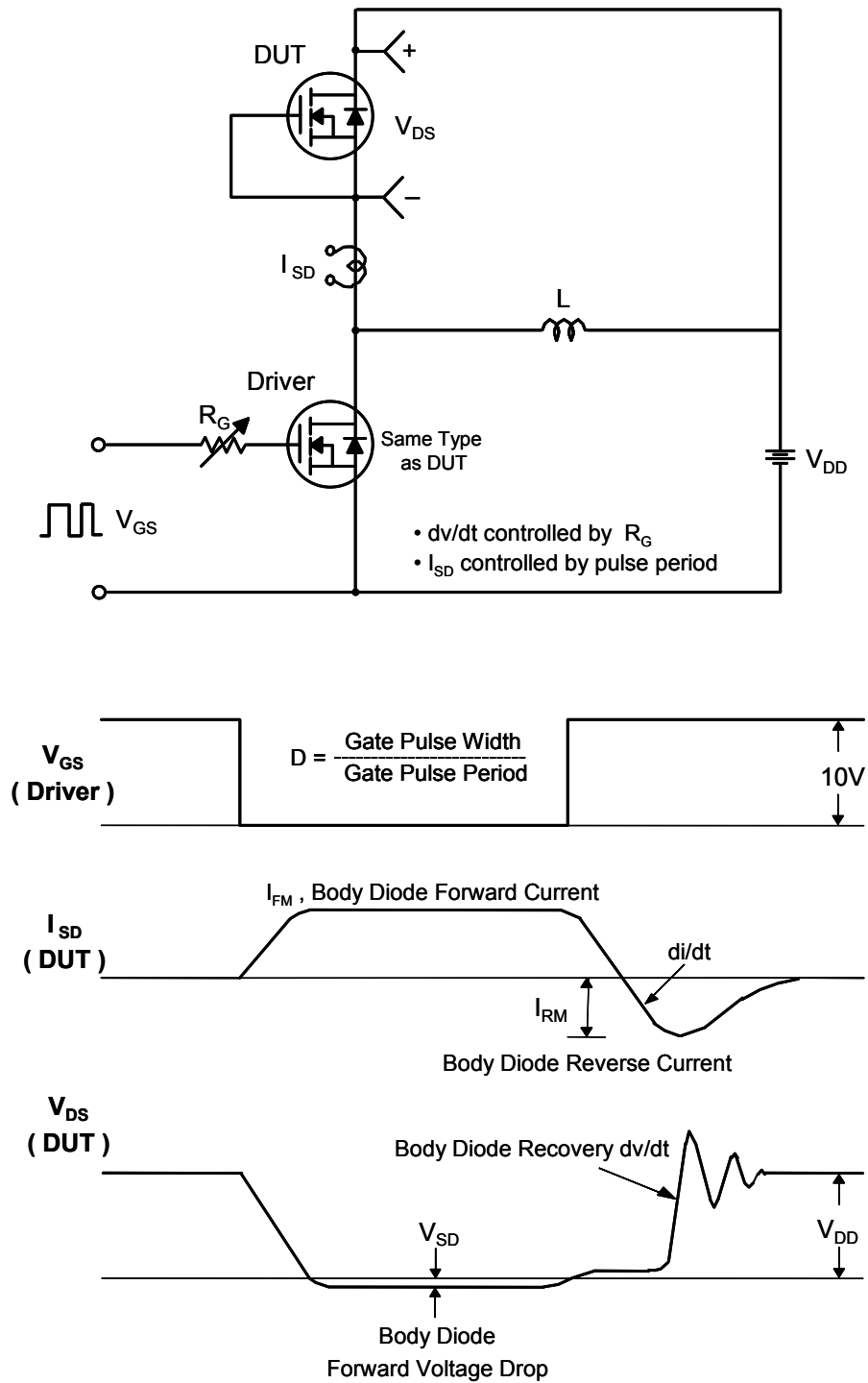
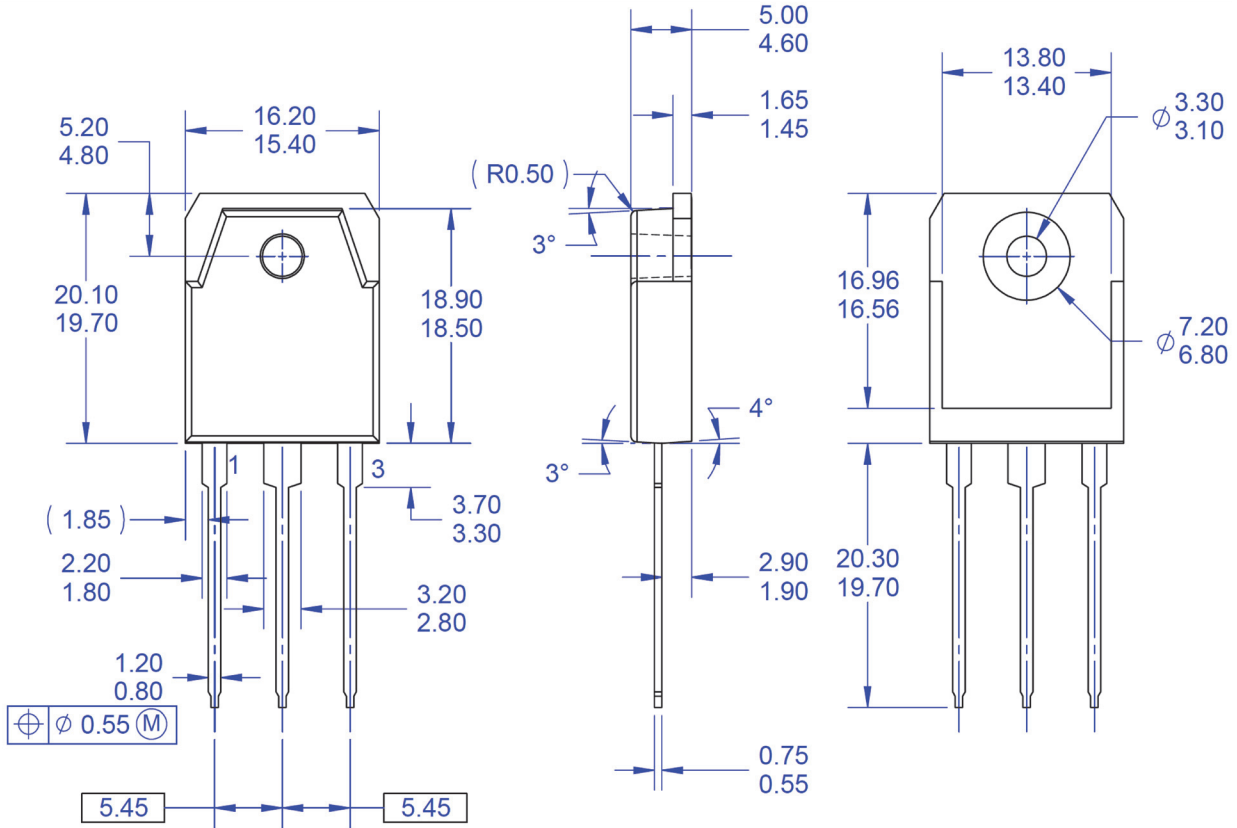


Figure 14. Peak Diode Recovery dv/dt Test Circuit & Waveforms



Mechanical Dimensions



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- E) DRAWING FILE NAME: TO3PN03AREV1.
- F) FAIRCHILD SEMICONDUCTOR.

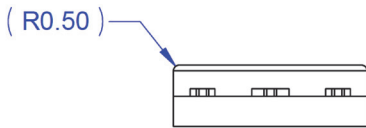


Figure 15. TO3PN, 3-Lead, Plastic, EIAJ SC-65

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