MOSFET – N-Channel, POWERTRENCH®

100 V, 214 A, 3.5 mΩ

FDB035N10A

Description

This N−Channel MOSFET is produced using **onsemi**'s advance POWERTRENCH process that has been tailored to minimize the on−state resistance while maintaining superior switching performance.

Features

- $R_{DS(on)}$ = 3.0 mΩ (Typ.) @ V_{GS} = 10 V, I_D = 75 A
- Fast Switching Speed
- Low Gate Charge, Q_G = 89 nC (Typ.)
- High Performance Trench Technology for Extremely Low $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
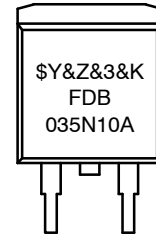- Micro Solar Inverter

V_{DSS}	$R_{DS(ON)}$ MAX	I_D MAX
100 V	3.5 mΩ @ 10 V	214 A*

*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.
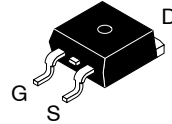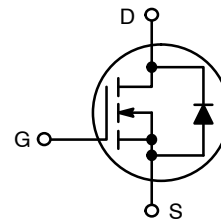

D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ

MARKING DIAGRAM

$Y&Z&3&K
FDB
035N10A

$Y	= Logo
&Z	= Assembly Plant Code
&3	= 3−Digit Date Code Format
&K	= 2−Digits Lot Run Traceability Code
FDB035N10A	= Device Code

N−Channel

ORDERING INFORMATION

FDB035N10A

MOSFET MAXIMUM RATINGS (T_C = 25°C unless otherwise noted)

Symbol	Parameter		FDB035N10A	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		±20	V
I_D	Drain Current	– Continuous (T_C = 25°C, Silicon Limited)	214*	A
		– Continuous (T_C = 100°C, Silicon Limited)	151*	
		– Continuous (T_C = 25°C, Package Limited)	120	
I_{DM}	Drain Current	– Pulsed (Note 1)	856	A
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		658	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		6.0	V/ns
P_D	Power Dissipation	(T_C = 25°C)	333	W
		– Derate Above 25°C	2.22	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		−55 to +175	°C
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.
*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.
1. Repetitive rating: pulse−width limited by maximum junction temperature.
2. Starting T_J = 25°C, L = 1 mH, I_{AS} = 36.3 A.
3. $I_{SD} \leq$ 75 A, di/dt $\leq$ 200 A/μs, $V_{DD} \leq$ BV$_{DSS}$, starting T_J = 25°C.

THERMAL CHARACTERISTICS

Symbol	Parameter	FDB035N10A	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	0.45	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Minimum Pad of 2−oz Copper), Max.	62.5	
	Thermal Resistance, Junction to Ambient (1 in^2 Pad of 2−oz Copper), Max.	40	

ELECTRICAL CHARACTERISTICS (T_C = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V, T_C = 25°C	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	0.07	–	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 80 V, V_{GS} = 0 V	–	–	1	μA
		V_{DS} = 80 V, T_C = 150°C	–	–	500	
I_{GSS}	Gate to Body Leakage Current	V_{GS} = ±20 V, V_{DS} = 0 V	–	–	±100	nA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	2.0	–	4.0	V
$R_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = 10 V, I_D = 75 A	–	3.0	3.5	mΩ
g_{FS}	Forward Transconductance	V_{DS} = 10 V, I_D = 75 A	–	167	–	S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = 25 V, V_{GS} = 0 V, f = 1 MHz	–	5485	7295	pF
C_{oss}	Output Capacitance		–	2430	3230	pF
C_{rss}	Reverse Transfer Capacitance		–	210	–	pF
$Q_{g(tot)}$	Total Gate Charge at 10 V	V_{DS} = 80 V, I_D = 75 A, V_{GS} = 10 V (Note 4)	–	89	116	nC
Q_{gs}	Gate to Source Gate Charge		–	24	–	nC
Q_{gs2}	Gate Charge Threshold to Plateau		–	8	–	nC
Q_{gd}	Gate to Drain "Miller" Charge		–	25	–	nC
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 50 V, I_D = 75 A, V_{GS} = 10 V, R_G = 4.7 Ω (Note 4)	–	22	54	ns
t_r	Turn–On Rise Time		–	54	118	ns
$t_{d(off)}$	Turn–Off Delay Time		–	37	84	ns
t_f	Turn–Off Fall Time		–	11	32	ns
ESR	Equivalent Series Resistance (G–S)	f = 1 MHz	–	1.2	–	Ω
DRAIN–SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain to Source Diode Forward Current		–	–	214*	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current		–	–	856	A
V_{SD}	Drain to Source Diode Forward Voltage	V_{GS} = 0 V, I_{SD} = 75 A	–	–	1.25	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_{SD} = 75 A, V_{DD} = 80 V, dI_F/dt = 100 A/μs	–	72	–	ns
Q_{rr}	Reverse Recovery Charge		–	129	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.
*Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 120 A.
4. Essentially independent of operating temperature typical characteristics.

FDB035N10A

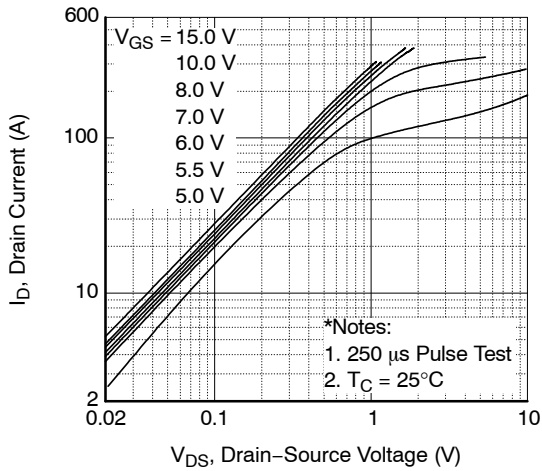## TYPICAL PERFORMANCE CHARACTERISTICS
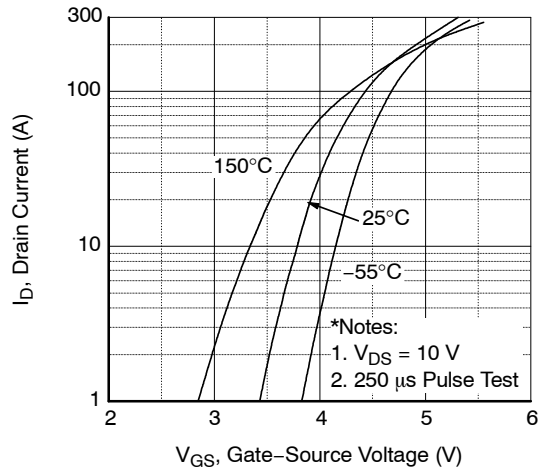
Figure 1. On−Region Characteristics
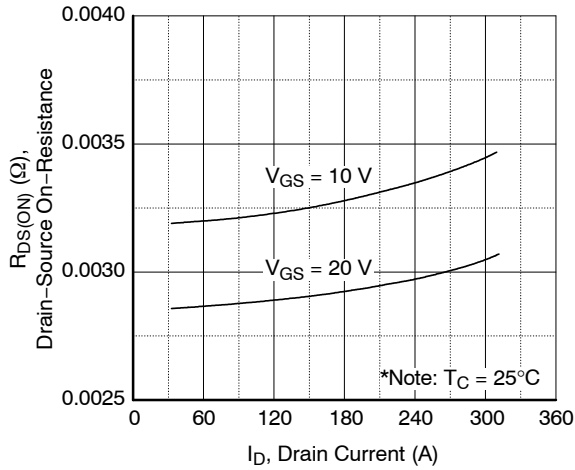
Figure 2. Transfer Characteristics

Figure 3. On−Resistance Variation vs. Drain Current and Gate Voltage
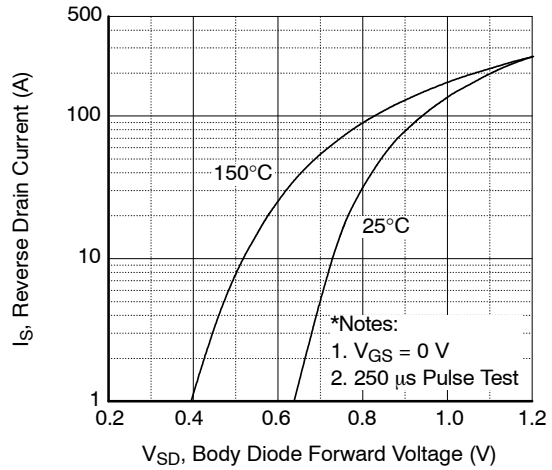
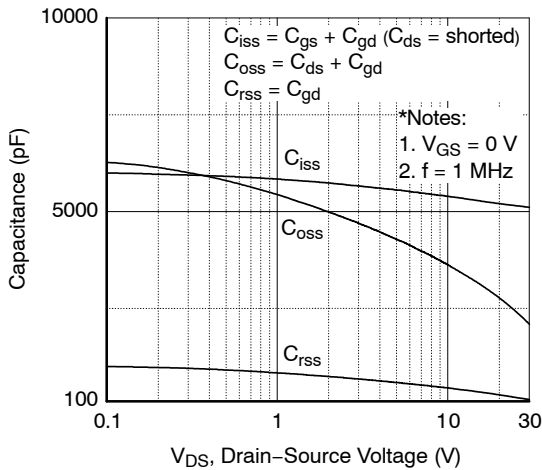**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**
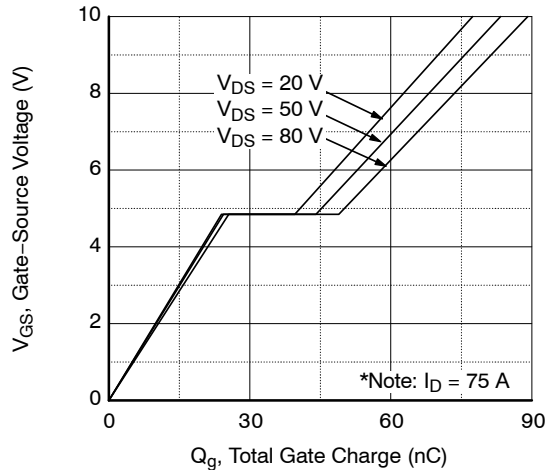
Figure 5. Capacitance Characteristics

Figure 6. Gate Charge Characteristics

FDB035N10A

TYPICAL PERFORMANCE CHARACTERISTICS (continued)
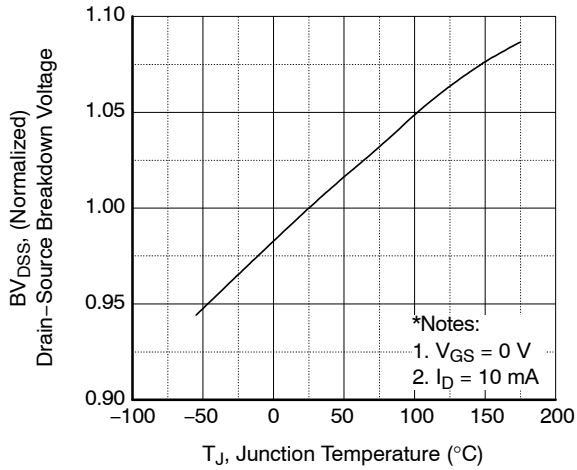
Figure 7. Breakdown Voltage Variation vs.
Temperature
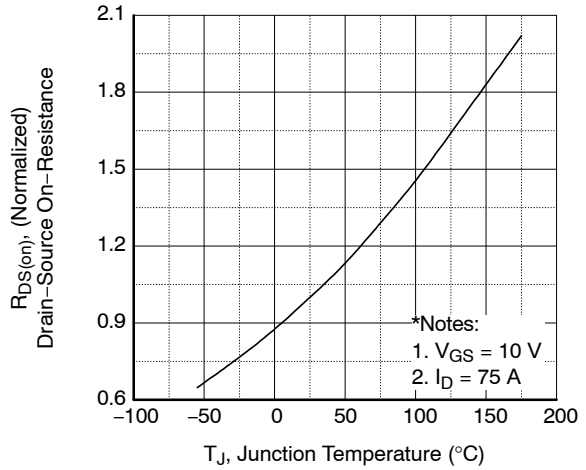
Figure 8. On−Resistance Variation vs.
Temperature
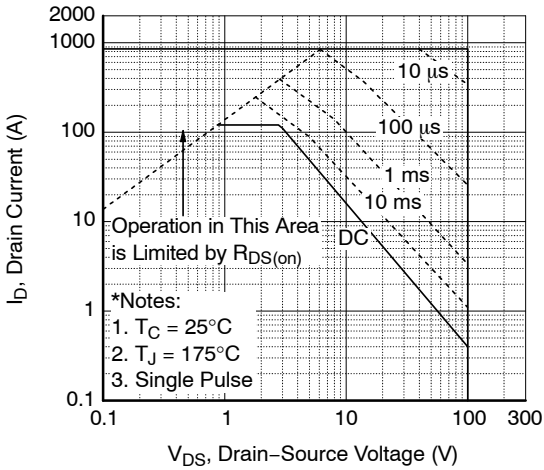
Figure 9. Maximum Safe Operating Area
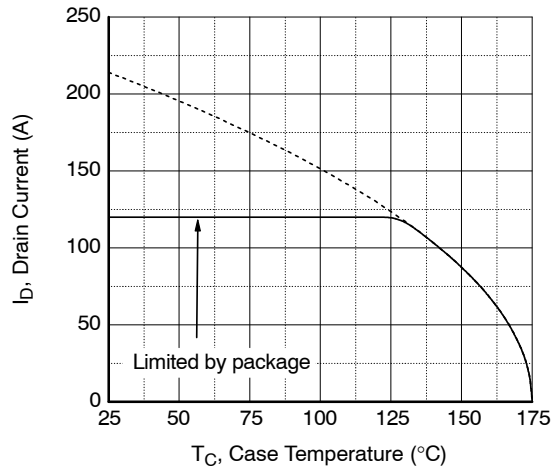
Figure 10. Maximum Drain Current vs.
Case Temperature
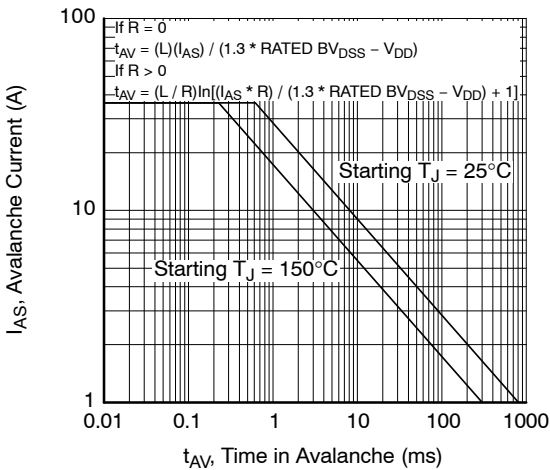
Figure 11. Unclamped Inductive Switching
Capability

TYPICAL PERFORMANCE CHARACTERISTICS (continued)
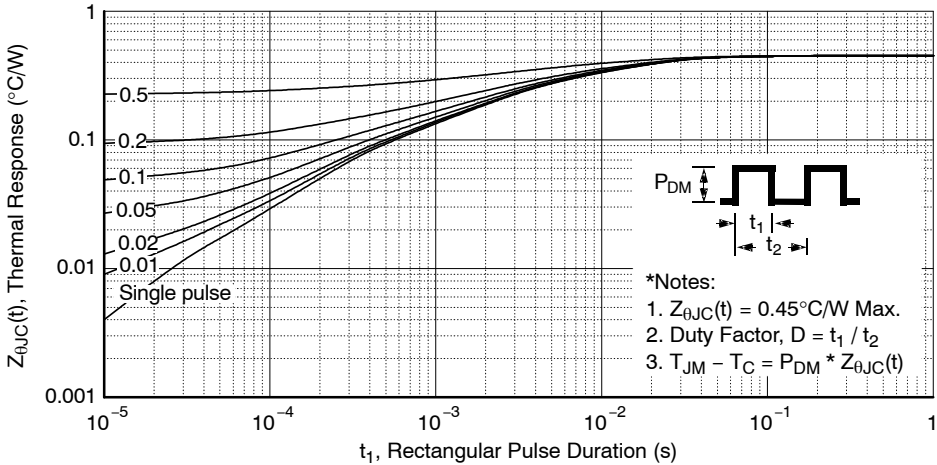
Figure 12. Transient Thermal Response Curve

The chart shows $Z_{\theta JC}(t)$, Thermal Response (°C/W) versus t_1, Rectangular Pulse Duration (s), with curves for duty factors 0.5, 0.2, 0.1, 0.05, 0.02, 0.01, and Single pulse.

*Notes:
1. $Z_{\theta JC}(t) = 0.45°C/W$ Max.
2. Duty Factor, $D = t_1 / t_2$
3. $T_{JM} - T_C = P_{DM} * Z_{\theta JC}(t)$
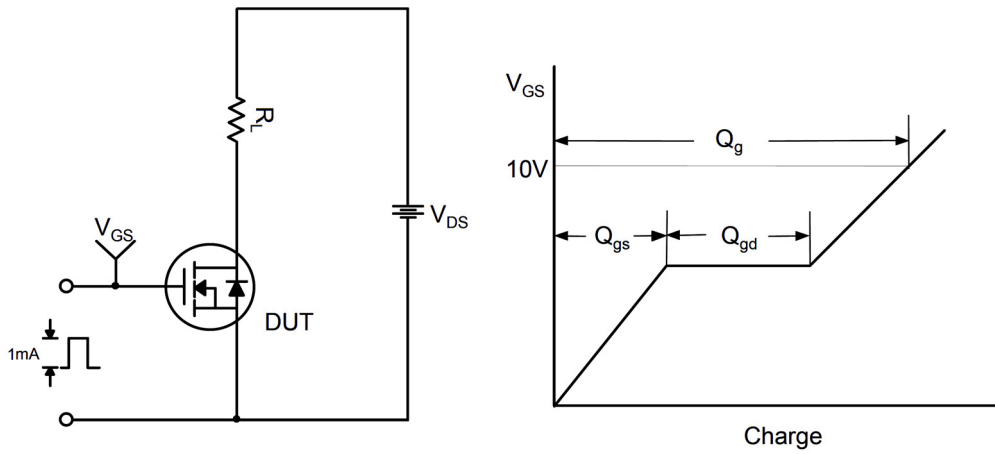
Figure 13. Gate Charge Test Circuit & Waveform
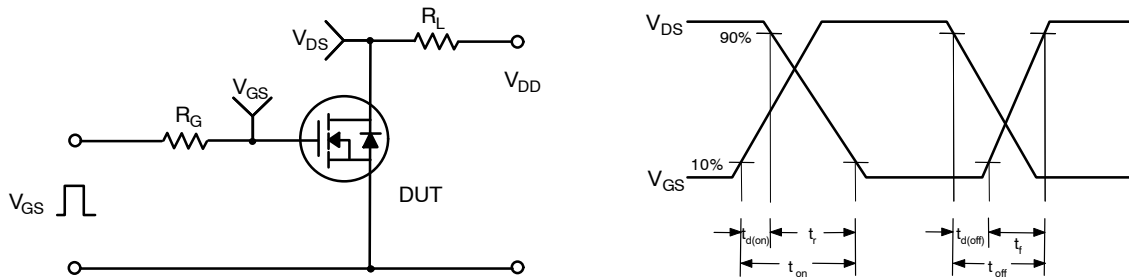
Figure 14. Resistive Switching Test Circuit & Waveforms

$$E_{AS} = \frac{1}{2} L I_{AS}^2$$
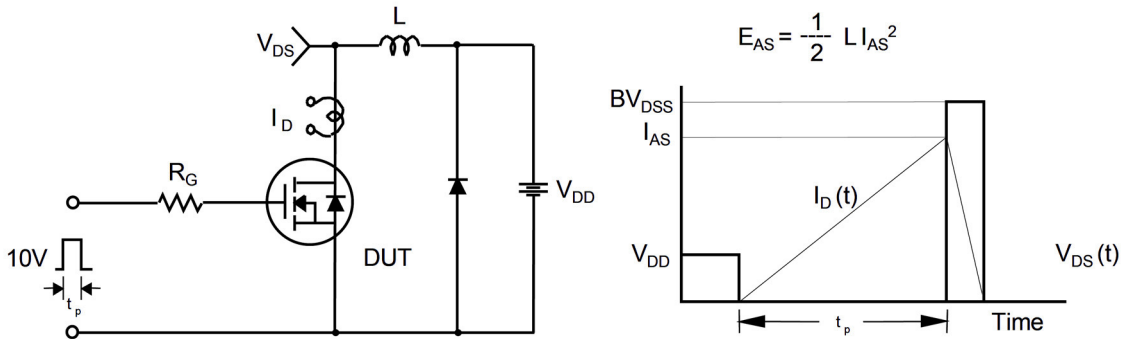
Figure 15. Unclamped Inductive Switching Test Circuit & Waveforms

FDB035N10A

$$D = \frac{\text{Gate Pulse Width}}{\text{Gate Pulse Period}}$$
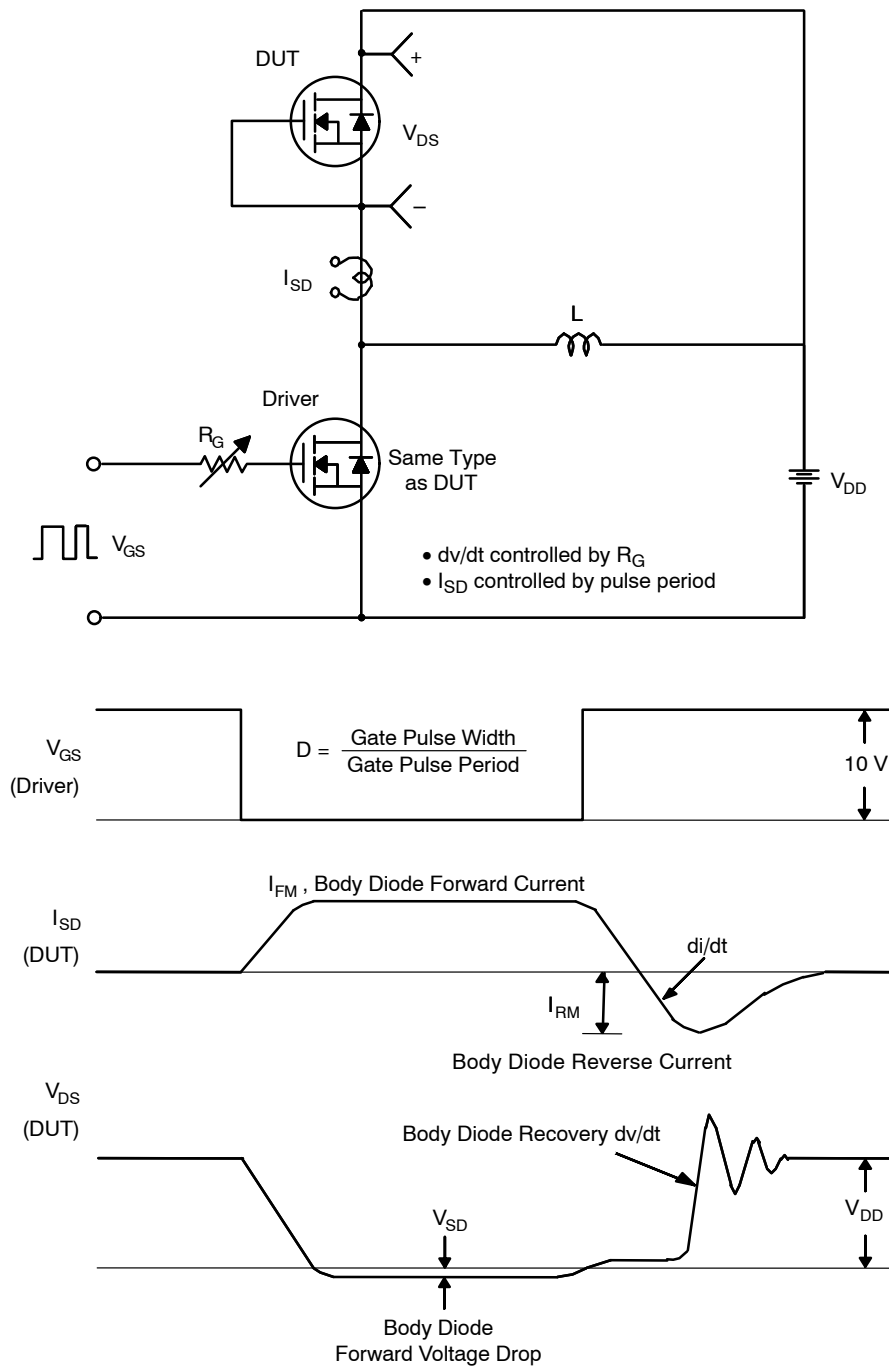
Figure 16. Peak Diode Recovery dv/dt Test Circuit & Waveforms

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping[†]
FDB035N10A	FDB035N10A	D^2−PAK	330 mm	24 mm	800 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

D²PAK−3 (TO−263, 3−LEAD)
CASE 418AJ
ISSUE F

DATE 11 MAR 2021

SCALE 1:1

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.

2. CONTROLLING DIMENSION: INCHES

3. CHAMFER OPTIONAL.

4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.

5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.

6. OPTIONAL MOLD FEATURE.

7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100 BSC		2.54 BSC	
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010 BSC		0.25 BSC	
M	0°	8°	0°	8°

0.436

0.366

0.653

0.169

2X 0.063

0.100 PITCH

RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SEATING PLANE

A

NOTE 3

c2

DETAIL C

A

GAUGE PLANE

L3

M

L

A1

SEATING PLANE

DETAIL C TIP LEADFORM ROTATED 90° CW

E

E/2

L1

H

NOTE 6

D

L2

e

2X b

⊕ 0.10 Ⓜ B A Ⓜ

VIEW A−A

(L1)

D1

E1

⊕ 0.10 Ⓜ B A Ⓜ

① ② ③ ④

VIEW A−A OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*

XX
XXXXXXXXX
AWLYWWG

XXXXXXXXG
AYWW

AYWW
XXXXXXXXG
AKA
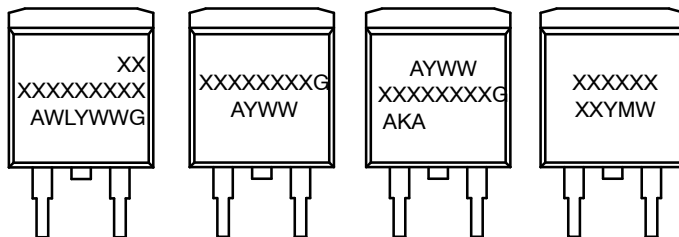
XXXXXX
XXYMW

IC   **Standard**   **Rectifier**   **SSG**

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb−Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪ ", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D²PAK−3 (TO−263, 3−LEAD)		PAGE 1 OF 1

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