

FDB9509L-F085

Power MOSFET, Single P-Channel

-40 V, -83 A, 8.0 mΩ

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	-40	V
Gate-to-Source Voltage	V_{GS}	± 16	V
Continuous Drain Current $R_{\theta JC}$ (Notes 1, 3)	I_D	$T_C = 25^\circ\text{C}$	-83
		$T_C = 100^\circ\text{C}$	-59
Power Dissipation $R_{\theta JC}$ (Note 1)	P_D	$T_C = 25^\circ\text{C}$	93.8
		$T_C = 100^\circ\text{C}$	46.9
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 3)	I_D	$T_C = 25^\circ\text{C}$	-16.1
		$T_C = 100^\circ\text{C}$	-11.4
Power Dissipation $R_{\theta JA}$ (Notes 1 & 2)	P_D	$T_C = 25^\circ\text{C}$	3.5
		$T_C = 100^\circ\text{C}$	1.7
Pulsed Drain Current	I_{DM}	-669	A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	-80	A
Single Pulse Drain-to-Source Avalanche Energy ($I_L(pk) = -64$)	E_{AS}	82	mJ
Lead Temperature for Soldering Purposes (1/83 from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case - Steady State	$R_{\theta JC}$	1.6	$^\circ\text{C}/\text{W}$
Junction-to-Ambient - Steady State (Note 2)	$R_{\theta JA}$	43	$^\circ\text{C}/\text{W}$

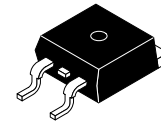
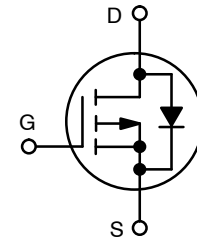
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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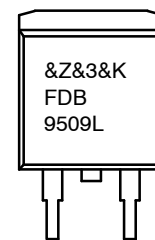
www.onsemi.com

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-40 V	8.0 mΩ @ -10 V	-83 A
	12.5 mΩ @ -4.5 V	



D²PAK-3 (TO-163AB)
CASE 418AJ

MARKING DIAGRAM



&Z = Assembly Plant Code
 &3 = Numeric Date Code
 &K = Lot Code
 FDB9509L = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

FDB9509L-F085

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Off Characteristics

Drain to Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-40			V	
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			20		$\text{mV}/^\circ\text{C}$	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = -40\text{ V}$	$T_J = 25^\circ\text{C}$			-1	μA
			$T_J = 175^\circ\text{C}$			-1	mA
Zero Gate Voltage Drain Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 16\text{ V}$				± 100	nA

On Characteristics (Note 4)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = -250\ \mu\text{A}$	-1	-1.7	-3	V
Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			-5		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = -10\text{ V}$	$I_D = -80\text{ A}$	6.4	8.0	$\text{m}\Omega$
		$V_{GS} = -4.5\text{ V}$	$I_D = -40\text{ A}$	9.6	12.5	

Charges, Capacitances & Gate Resistance

Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = -20\text{ V}$		3400		μF
Output Capacitance	C_{oss}			1250		μF
Reverse Transfer Capacitance	C_{rss}			39		μF
Gate Resistance	R_g	$V_{GS} = 0.5\text{ V}, f = 100\text{ kHz}$		21		Ω
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = -10\text{ V}, V_{DS} = -32\text{ V}; I_D = -80\text{ A}$		48		nC
		$V_{GS} = -4.5\text{ V}, V_{DS} = -32\text{ V}; I_D = -80\text{ A}$		22		
Threshold Gate Charge	$Q_{g(th)}$	$V_{GS} = 0\text{ to }-1\text{ V}$		6		
Gate to Source Gate Charge	Q_{gs}	$V_{DD} = -32\text{ V}, I_D = -80\text{ A}$		12		
Gate to Drain "Miller" Charge	Q_{gd}			5		
Plateau Voltage	V_{GP}			-3.5		V

Switching Characteristics

Turn-On Delay Time	$t_{d(ON)}$	$V_{DD} = -20\text{ V}, I_D = -80\text{ A}, V_{GS} = -10\text{ V}, R_{GEN} = 6\ \Omega$		9		ns
Turn-On Rise Time	t_r			4		ns
Turn-Off Delay Time	$t_{d(OFF)}$			200		ns
Turn-Off Fall Time	t_f			57		ns

Drain-Source Diode Characteristics

Source to Drain Diode Voltage	V_{SD}	$I_{SD} = -80\text{ A}, V_{GS} = 0\text{ V}$		-0.98	-1.25	V
		$I_{SD} = -40\text{ A}, V_{GS} = 0\text{ V}$		-0.9	-1.2	V
Reverse Recovery Time	T_{RR}	$V_{GS} = 0\text{ V}, dI_{SD}/dt = 100\text{ A}/\mu\text{s}, I_S = -80\text{ A}$		78		ns
Charge Time	t_a			33		
Discharge Time	t_b			46		
Reverse Recovery Charge	Q_{RR}			95		

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

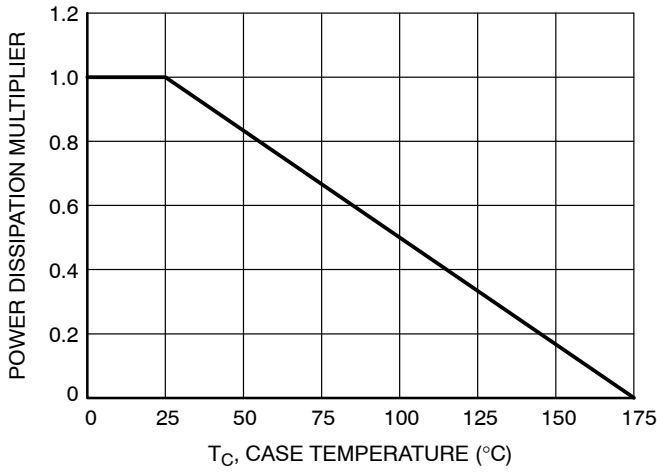


Figure 1. Normalized Power Dissipation vs. Case Temperature

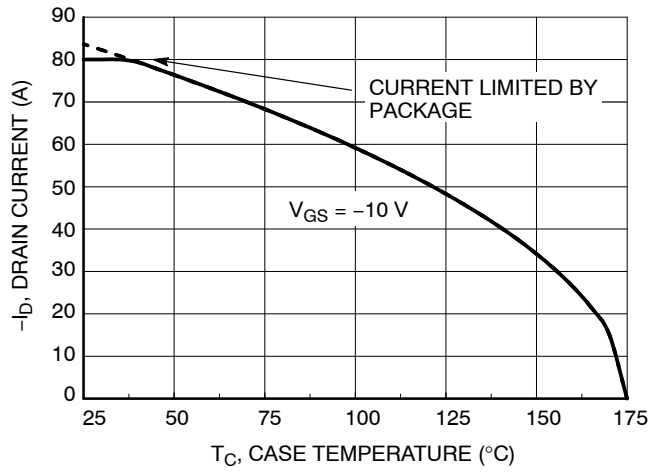


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

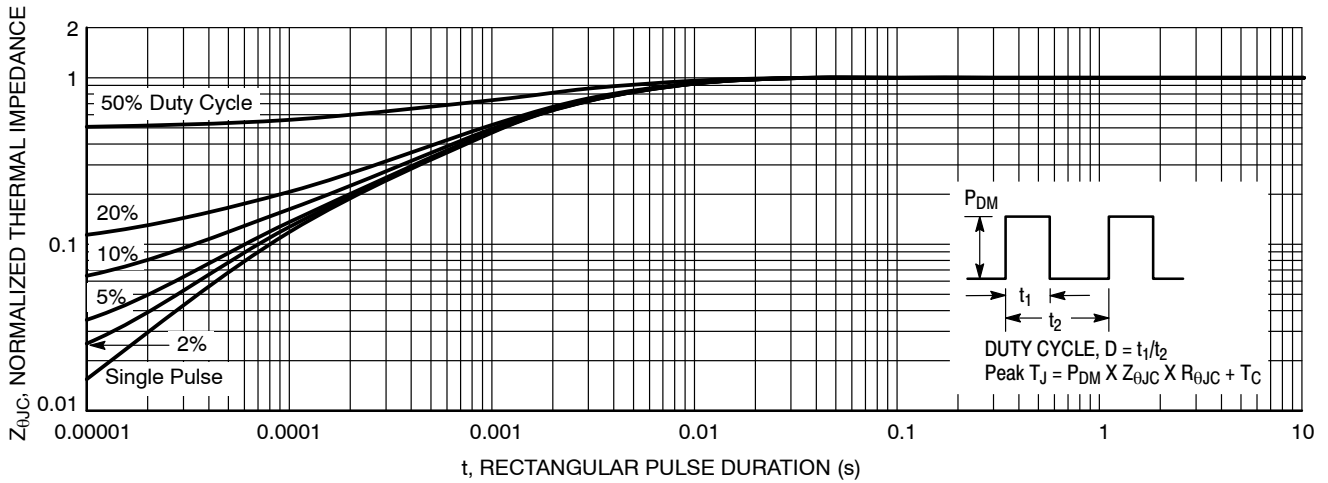


Figure 3. Normalized Maximum Transient Thermal Impedance

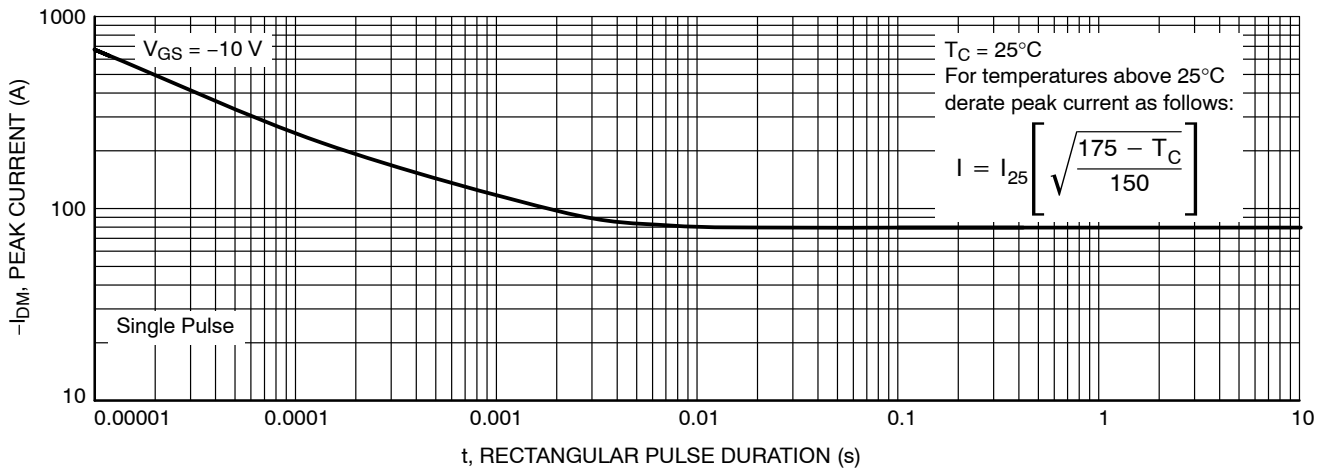


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

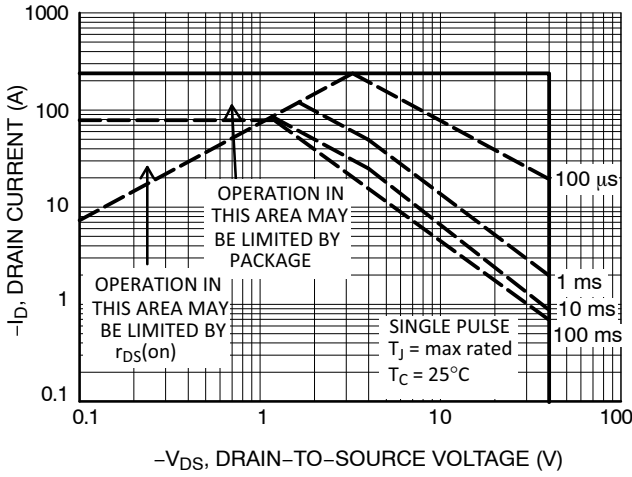
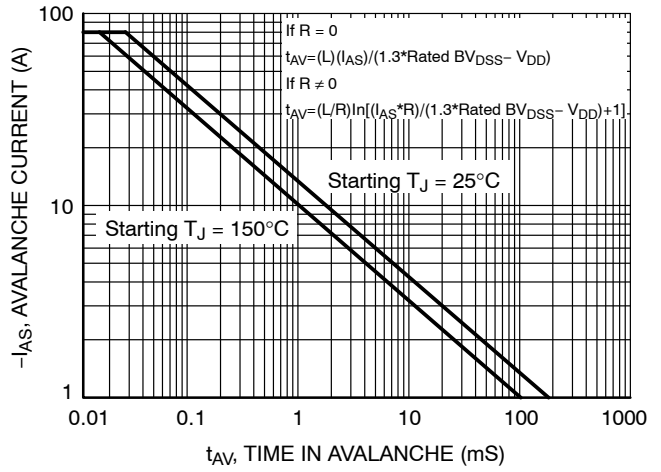


Figure 5. Forward Bias Safe Operating Area



Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

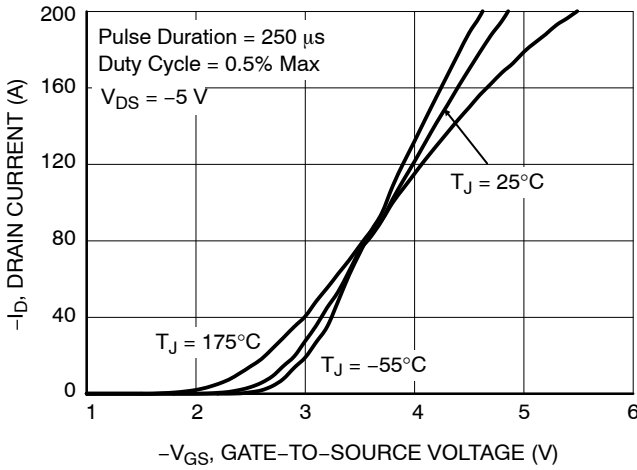


Figure 7. Transfer Characteristics

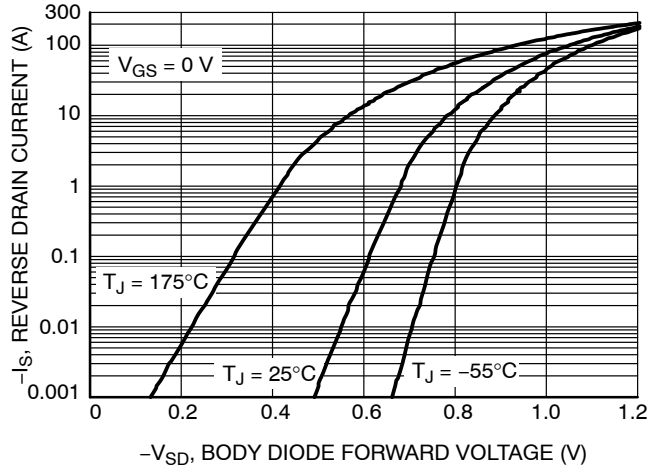


Figure 8. Forward Diode Characteristics

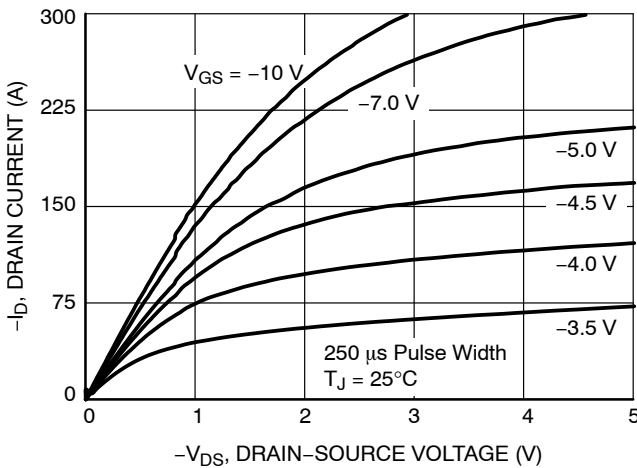


Figure 9. Saturation Characteristics

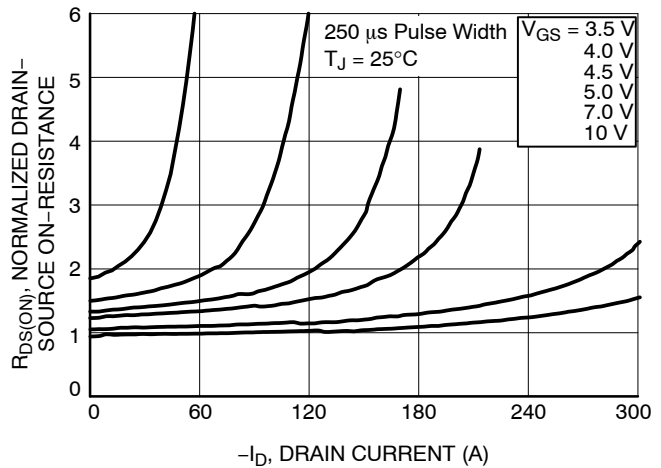


Figure 10. Normalized $R_{DS(ON)}$ vs. Drain Current

TYPICAL CHARACTERISTICS

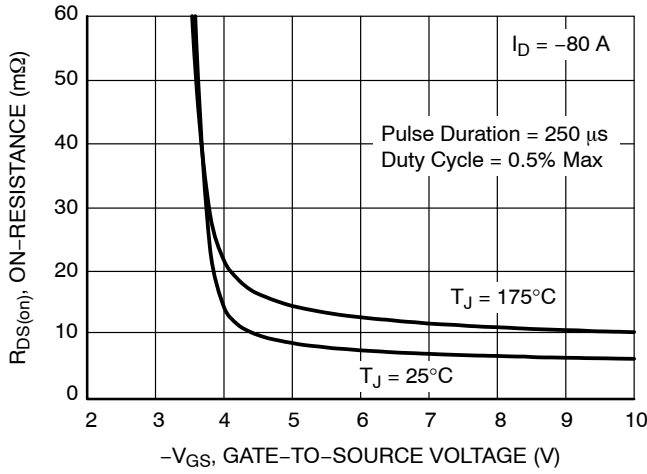


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

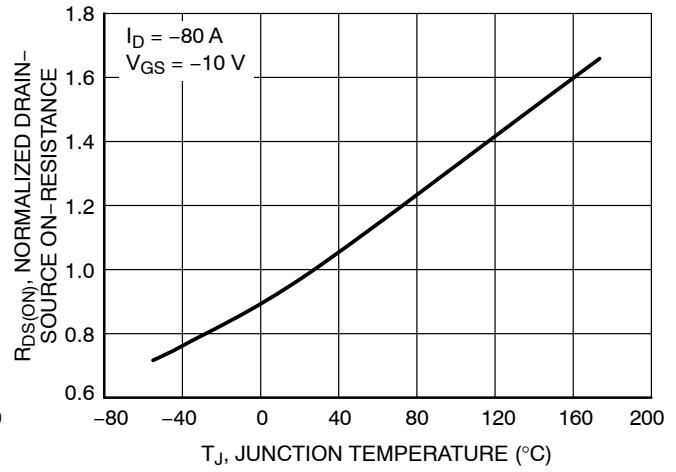


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

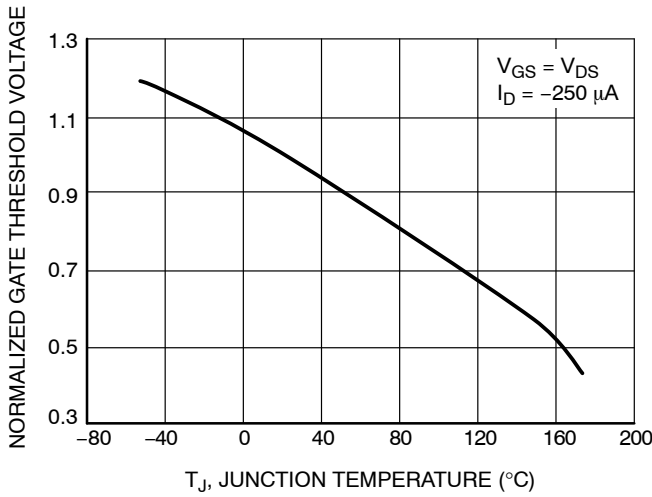


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

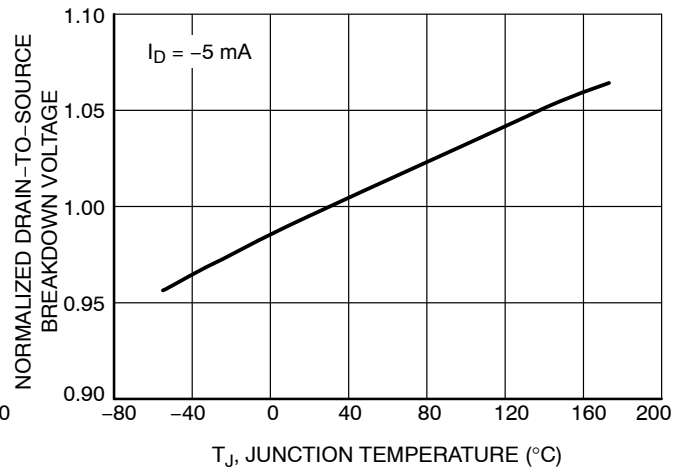


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

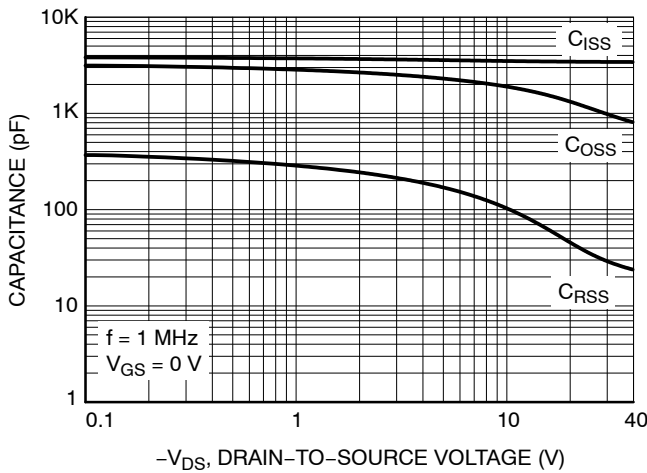


Figure 15. Capacitance vs. Drain-to-Source Voltage

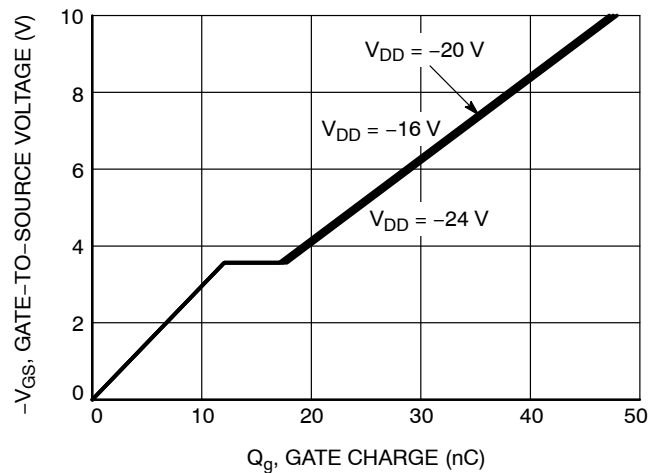


Figure 16. Gate Charge vs. Gate-to-Source Voltage

FDB9509L-F085

ORDERING INFORMATION

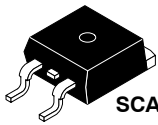
Device	Device Marking	Package	Shipping†
FDB9509L-F085	FDB9509L	D ² PAK-3 (Pb-Free, Halogen Free)	3,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

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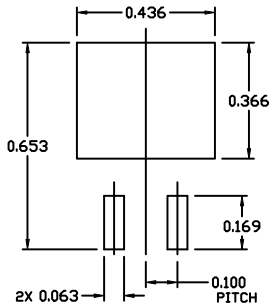
SCALE 1:1

D²PAK-3 (TO-263, 3-LEAD)

CASE 418AJ

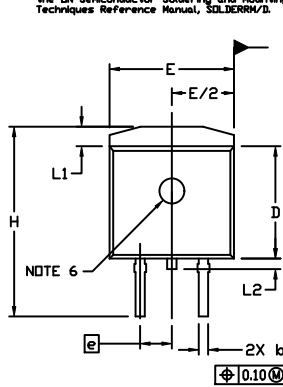
ISSUE F

DATE 11 MAR 2021



RECOMMENDED MOUNTING FOOTPRINT

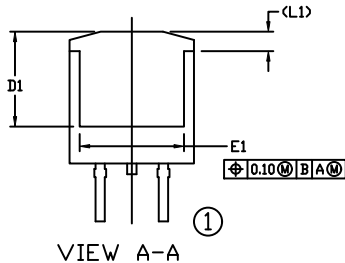
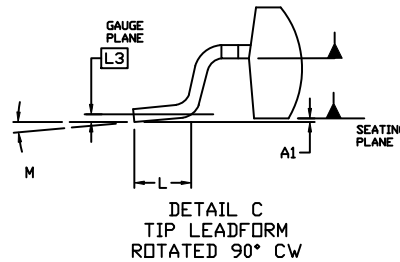
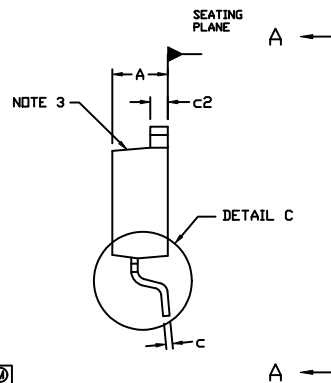
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



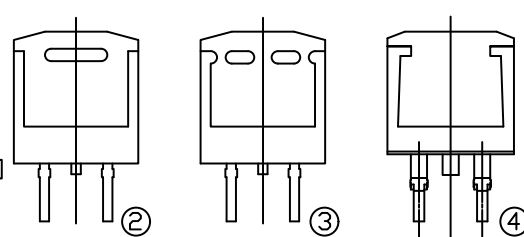
NOTES:

- DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
- CONTROLLING DIMENSION: INCHES
- CHAMFER OPTIONAL.
- DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
- THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
- OPTIONAL MOLD FEATURE.
- ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0*	8*	0*	8*

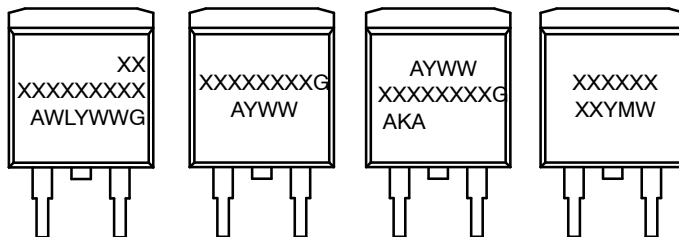


VIEW A-A



VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



IC

Standard

Rectifier

SSG

- XXXXXX = Specific Device Code
- A = Assembly Location
- WL = Wafer Lot
- Y = Year
- WW = Work Week
- W = Week Code (SSG)
- M = Month Code (SSG)
- G = Pb-Free Package
- AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	D ² PAK-3 (TO-263, 3-LEAD)	PAGE 1 OF 1

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