

FDB9509L-F085

Power MOSFET, Single P-Channel

-40 V, -83 A, 8.0 mΩ

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low QG and Capacitance to Minimize Driver Losses
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Parameter			Symbol	Value	Unit
Drain-to-Source Voltage			V _{DSS}	−40	V
Gate-to-Source Voltage			V _{GS}	±16	V
Continuous Drain Current R _{θJC} (Notes 1, 3)	Steady State	T _C = 25 °C	I _D	−83	A
		T _C = 100 °C		−59	
Power Dissipation R _{θJC} (Note 1)		T _C = 25 °C	P _D	93.8	W
		T _C = 100 °C		46.9	
Continuous Drain Current R _{θJA} (Notes 1, 2, 3)	Steady State	T _C = 25 °C	I _D	−16.1	A
		T _C = 100 °C		−11.4	
Power Dissipation R _{θJA} (Notes 1 & 2)		T _C = 25 °C	P _D	3.5	W
		T _C = 100 °C		1.7	
Pulsed Drain Current	T _C = 25 °C, t _p = 10 μs		I _{DM}	−669	A
Operating Junction and Storage Temperature			T _J , T _{stg}	−55 to +175	°C
Source Current (Body Diode)			I _S	−80	A
Single Pulse Drain-to-Source Avalanche Energy (I _L (pk) = −64)			E _{AS}	82	mJ
Lead Temperature for Soldering Purposes (1/83 from case for 10 s)			T _L	260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State	$R_{\theta JC}$	1.6	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Note 2)	$R_{\theta JA}$	43	$^\circ\text{C}/\text{W}$

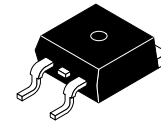
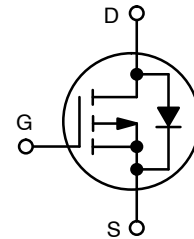
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm², 2 oz. Cu pad.
3. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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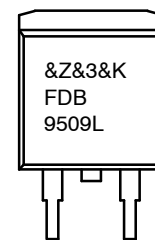
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$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
-40 V	8.0 mΩ @ -10 V	-83 A
	12.5 mΩ @ -4.5 V	



D²PAK-3 (TO-163AB)
CASE 418AJ

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = Lot Code
FDB9509L = Specific Device Code

ORDERING INFORMATION

See detailed ordering, marking and shipping information on page 6 of this data sheet.

FDB9509L–F085

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
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Off Characteristics

Drain to Source Breakdown Voltage	V _{(BR)DSS}	V _{GS} = 0 V, I _D = -250 μA	-40			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	V _{(BR)DSS} /T _J			20		mV/°C
Zero Gate Voltage Drain Current	I _{DSS}	V _{GS} = 0 V, V _{DS} = -40 V	T _J = 25°C		-1	μA
			T _J = 175°C		-1	mA
Zero Gate Voltage Drain Current	I _{GSS}	V _{DS} = 0 V, V _{GS} = ±16 V			±100	nA

On Characteristics (Note 4)

Gate Threshold Voltage	V _{GS(TH)}	V _{GS} = V _{DS} , I _D = -250 μA	-1	-1.7	-3	V
Threshold Temperature Coefficient	V _{GS(TH)} /T _J			-5		mV/°C
Drain-to-Source On Resistance	R _{DS(on)}	V _{GS} = -10 V, I _D = -80 A		6.4	8.0	mΩ
		V _{GS} = -4.5 V, I _D = -40 A		9.6	12.5	mΩ

Charges, Capacitances & Gate Resistance

Input Capacitance	C _{iss}	V _{GS} = 0 V, f = 1 MHz, V _{DS} = -20 V		3400		pF
Output Capacitance	C _{oss}			1250		pF
Reverse Transfer Capacitance	C _{rss}			39		pF
Gate Resistance	R _g	V _{GS} = 0.5 V, f = 100 kHz		21		Ω
Total Gate Charge	Q _{G(TOT)}	V _{GS} = -10 V, V _{DS} = -32 V, I _D = -80 A		48		nC
		V _{GS} = -4.5V, V _{DS} = -32 V, I _D = -80 A		22		
Threshold Gate Charge	Q _{g(th)}	V _{GS} = 0 to -1 V		6		
Gate to Source Gate Charge	Q _{gs}	V _{DD} = -32 V, I _D = -80 A		12		
Gate to Drain “Miller” Charge	Q _{gd}			5		
Plateau Voltage	V _{GP}			-3.5		V

Switching Characteristics

Turn-On Delay Time	t _{d(ON)}	V _{DD} = -20 V, I _D = -80 A, V _{GS} = -10 V, R _{GEN} = 6 Ω		9		ns
Turn-On Rise Time	t _r			4		ns
Turn-Off Delay Time	t _{d(OFF)}			200		ns
Turn-Off Fall Time	t _f			57		ns

Drain-Source Diode Characteristics

Source to Drain Diode Voltage	V _{SD}	I _{SD} = -80 A, V _{GS} = 0 V		-0.98	-1.25	V
		I _{SD} = -40 A, V _{GS} = 0 V		-0.9	-1.2	V
Reverse Recovery Time	T _{RR}	V _{GS} = 0 V, dI _{SD} /dt = 100 A/us, I _S = -80 A		78		ns
Charge Time	t _a			33		
Discharge Time	t _b			46		
Reverse Recovery Charge	Q _{RR}			95		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Pulse Test: pulse width ≤ 300 μs, duty cycle ≤ 2%

5. Switching characteristics are independent of operating junction temperatures.

TYPICAL CHARACTERISTICS

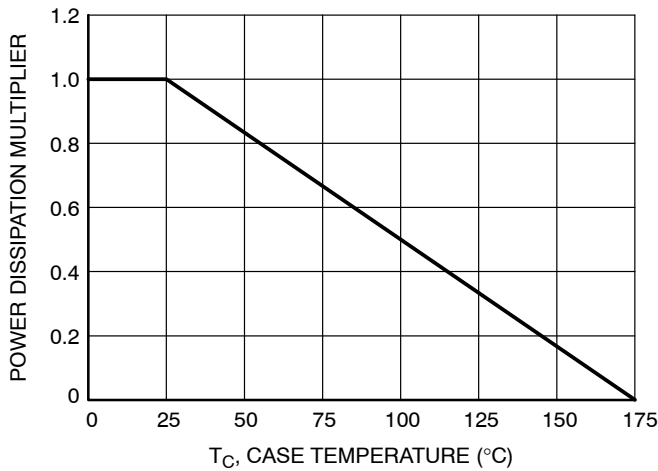


Figure 1. Normalized Power Dissipation vs. Case Temperature

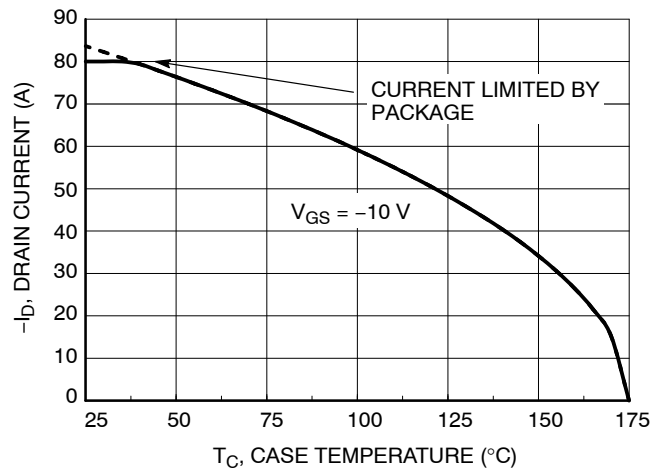


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

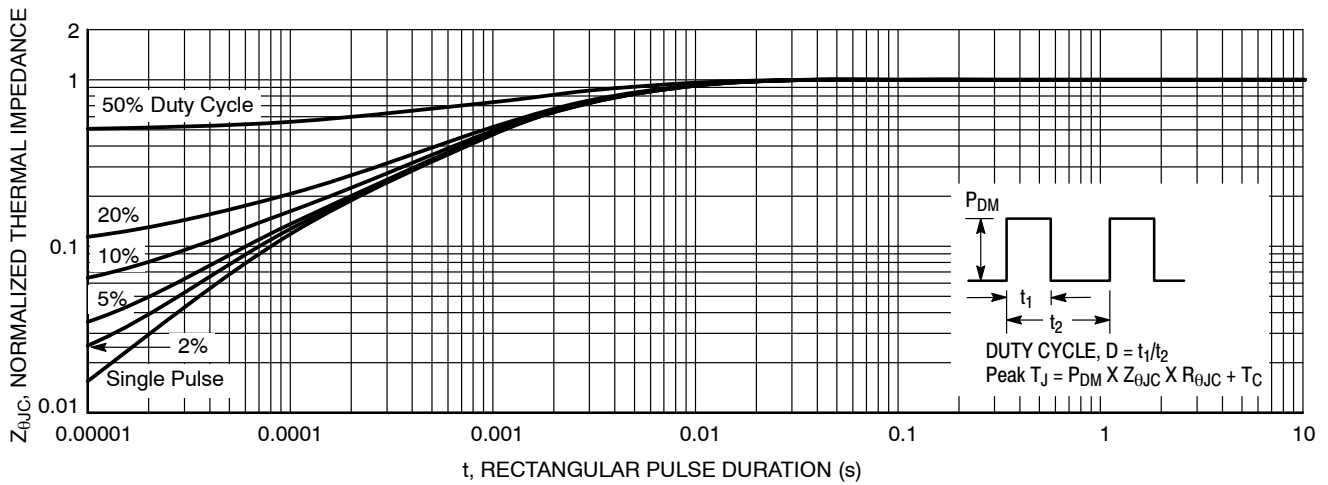


Figure 3. Normalized Maximum Transient Thermal Impedance

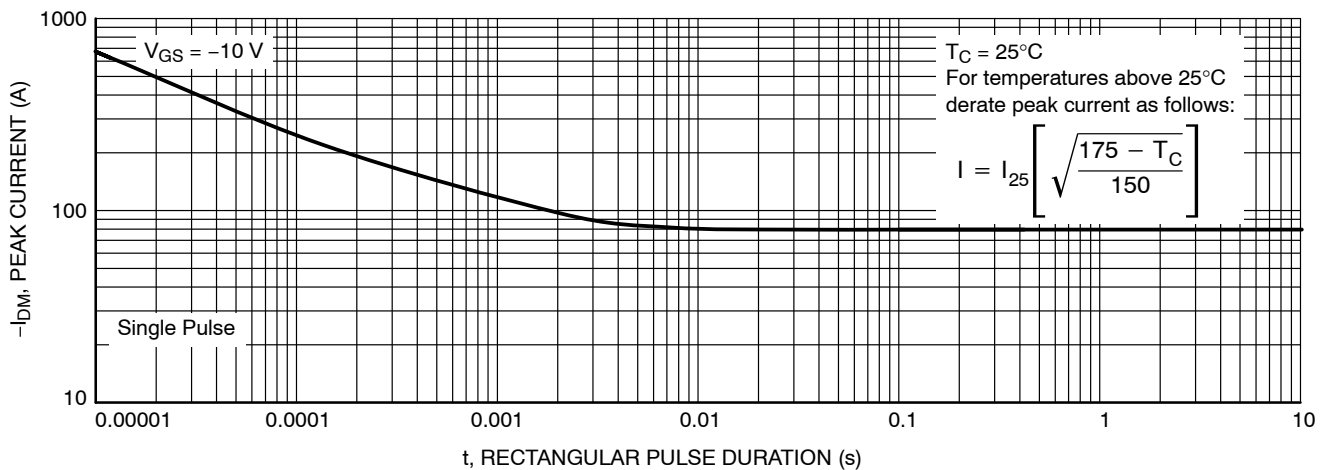


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS

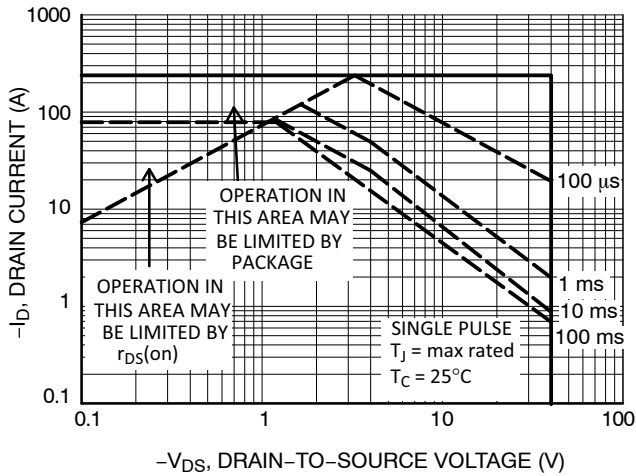
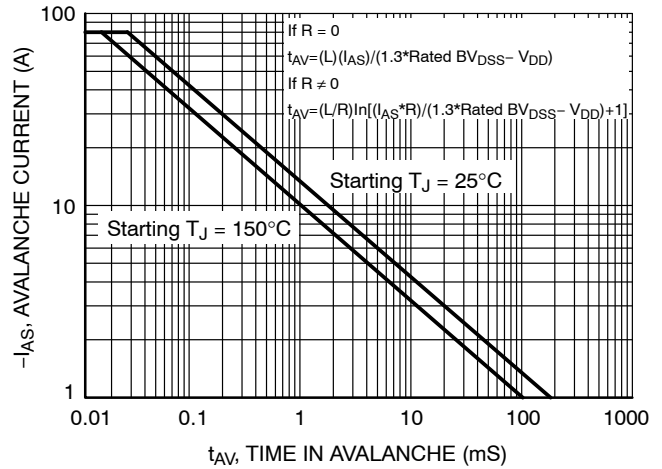


Figure 5. Forward Bias Safe Operating Area



Note: Refer to ON Semiconductor Application Notes AN7514 and AN7515

Figure 6. Unclamped Inductive Switching Capability

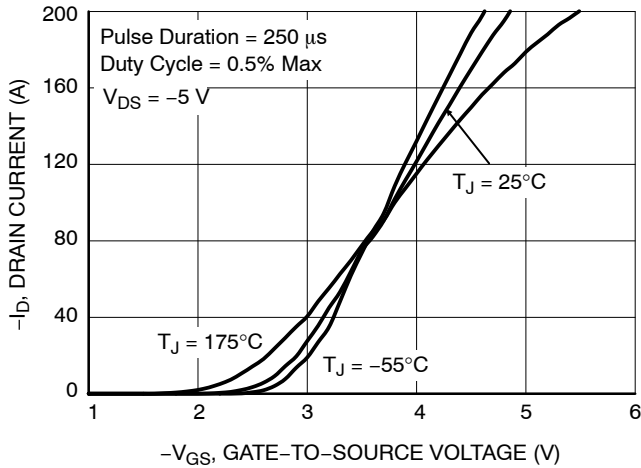


Figure 7. Transfer Characteristics

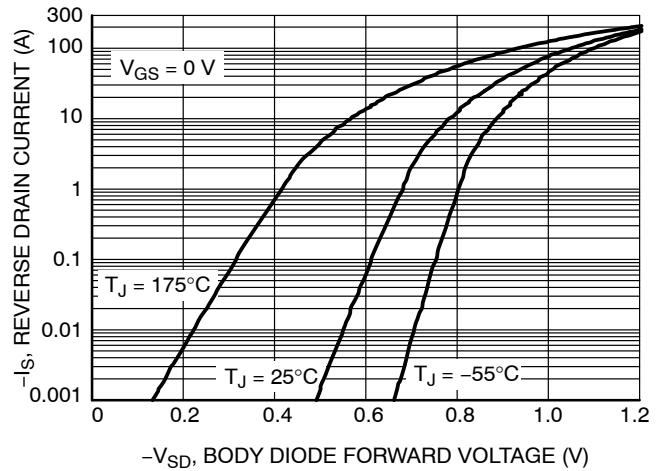


Figure 8. Forward Diode Characteristics

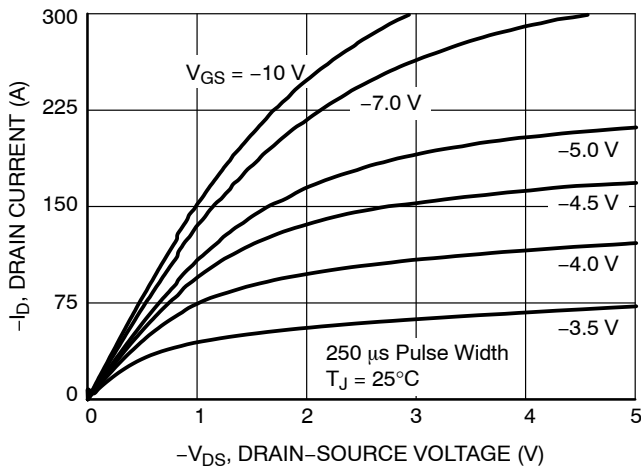
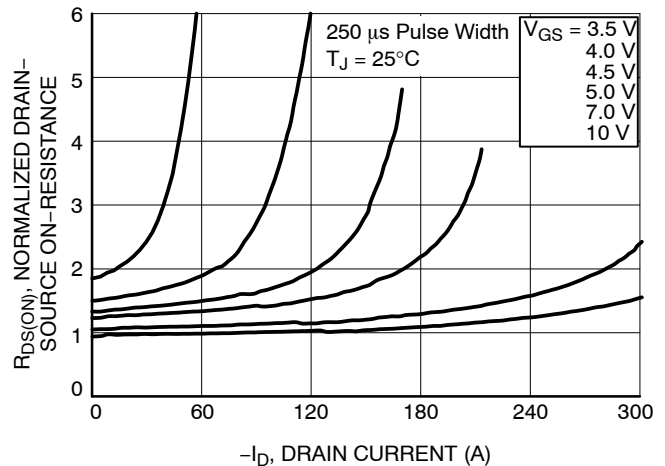


Figure 9. Saturation Characteristics

Figure 10. Normalized $R_{DS(ON)}$ vs. Drain Current

TYPICAL CHARACTERISTICS

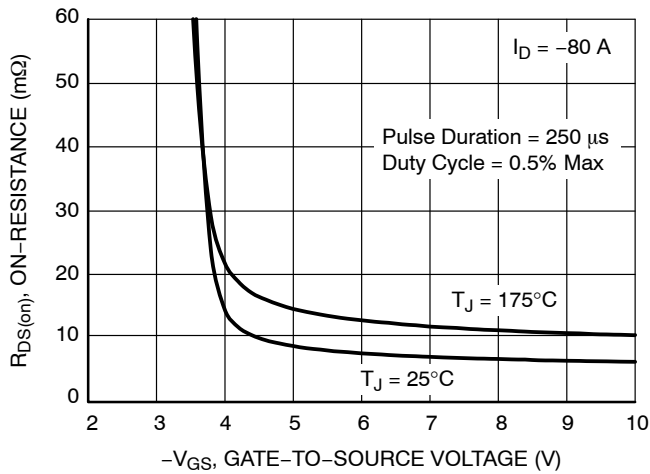


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

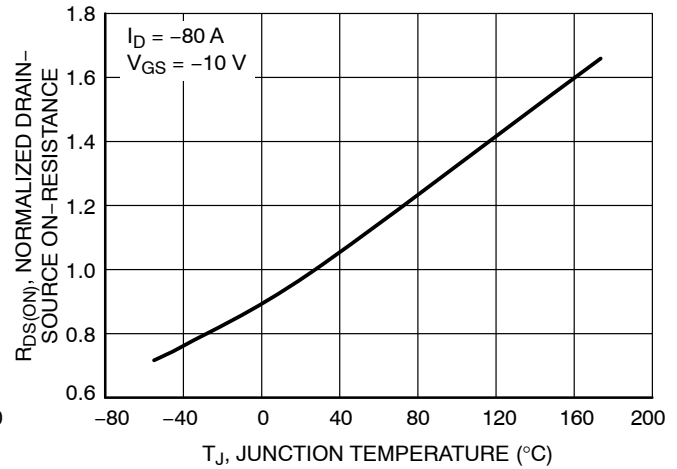


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

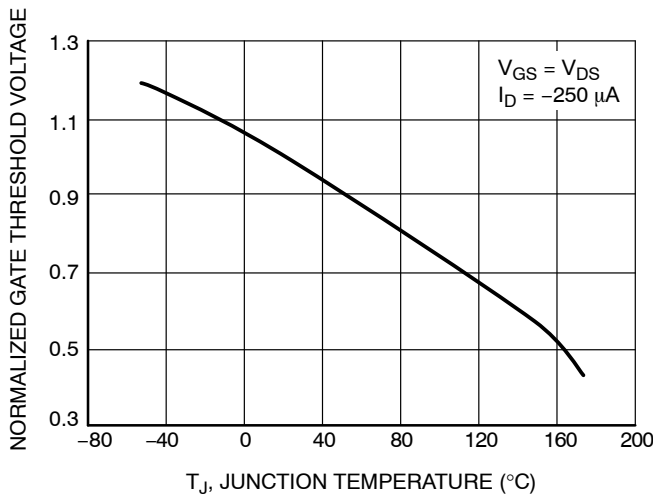


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

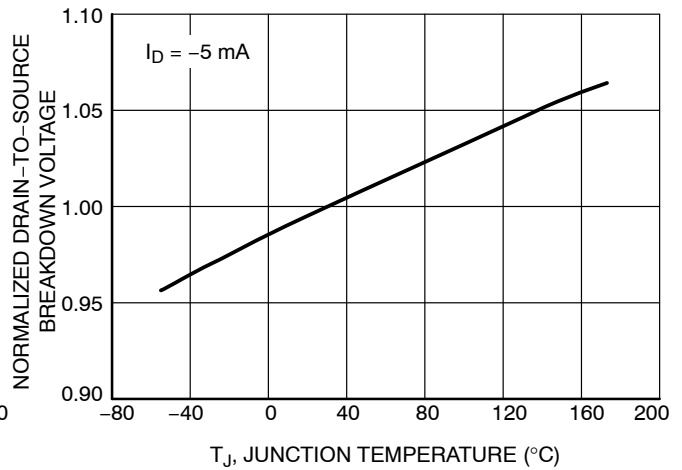


Figure 14. Normalized Drain-to-Source Breakdown Voltage vs. Junction Temperature

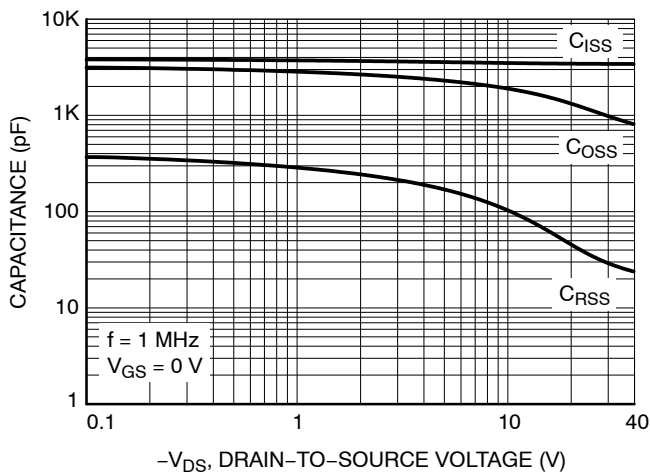


Figure 15. Capacitance vs. Drain-to-Source Voltage

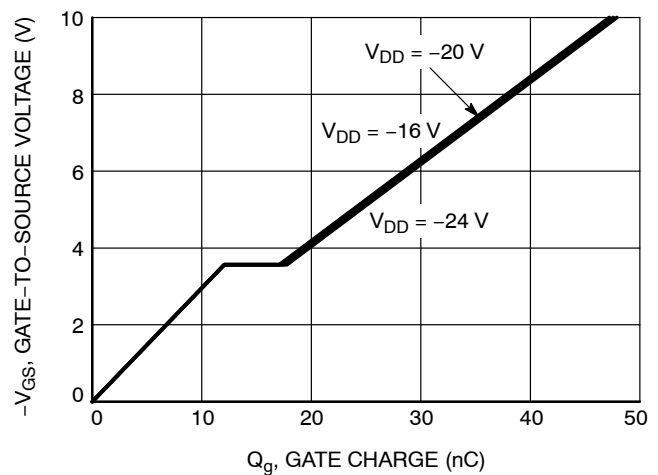


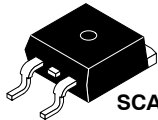
Figure 16. Gate Charge vs. Gate-to-Source Voltage

FDB9509L–F085

ORDERING INFORMATION

Device	Device Marking	Package	Shipping†
FDB9509L–F085	FDB9509L	D ² PAK–3 (Pb–Free, Halogen Free)	3,000 / Tape & Reel

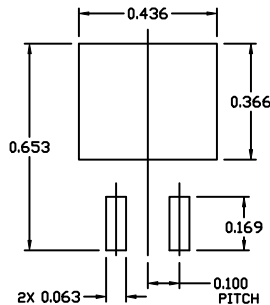
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D



SCALE 1:1

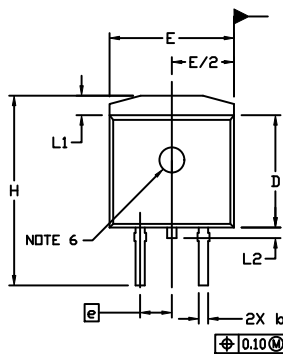
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ISSUE F

DATE 11 MAR 2021



**RECOMMENDED
MOUNTING FOOTPRINT**

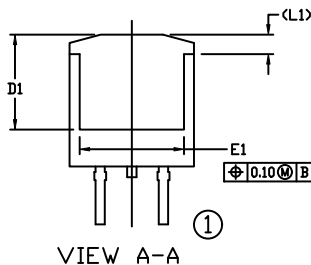
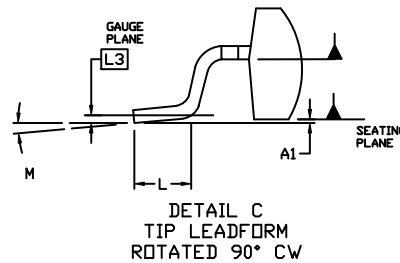
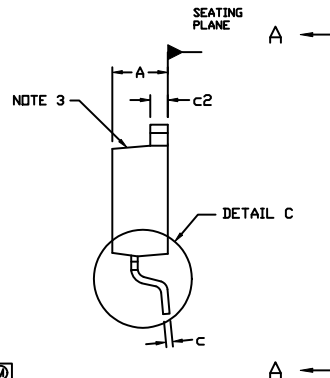
For additional information on our Pb-free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



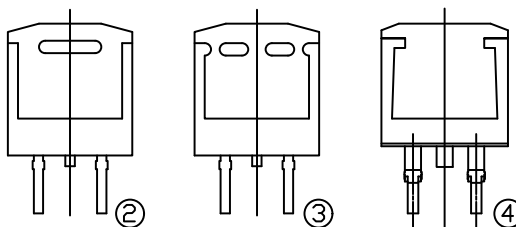
NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: INCHES
3. CHAMFER OPTIONAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005 PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY AT DATUM H.
5. THERMAL PAD CONTOUR IS OPTIONAL WITHIN DIMENSIONS E, L1, D1, AND E1.
6. OPTIONAL MOLD FEATURE.
7. ①, ② ... OPTIONAL CONSTRUCTION FEATURE CALL OUTS.

DIM	INCHES		MILLIMETERS	
	MIN.	MAX.	MIN.	MAX.
A	0.160	0.190	4.06	4.83
A1	0.000	0.010	0.00	0.25
b	0.020	0.039	0.51	0.99
c	0.012	0.029	0.30	0.74
c2	0.045	0.065	1.14	1.65
D	0.330	0.380	8.38	9.65
D1	0.260	---	6.60	---
E	0.380	0.420	9.65	10.67
E1	0.245	---	6.22	---
e	0.100	BSC	2.54	BSC
H	0.575	0.625	14.60	15.88
L	0.070	0.110	1.78	2.79
L1	---	0.066	---	1.68
L2	---	0.070	---	1.78
L3	0.010	BSC	0.25	BSC
M	0°	8°	0°	8°

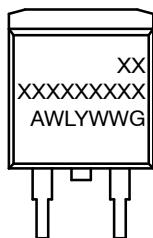


VIEW A-A

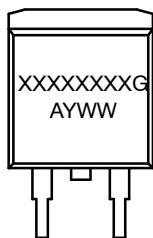


VIEW A-A
OPTIONAL CONSTRUCTIONS

GENERIC MARKING DIAGRAMS*



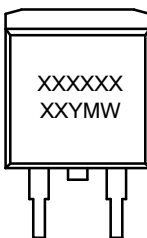
IC



Standard



Rectifier



SSG

XXXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
Y = Year
WW = Work Week
W = Week Code (SSG)
M = Month Code (SSG)
G = Pb-Free Package
AKA = Polarity Indicator

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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