

MOSFET – N-Channel, POWERTRENCH[®]

100 V, 300 A, 2.0 mΩ

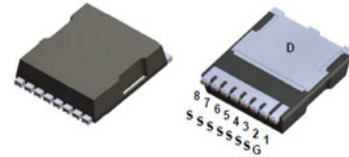
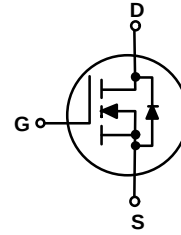
FDBL86062-F085

Features

- Typical $R_{DS(on)} = 1.5 \text{ m}\Omega$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- Typical $Q_{g(tot)} = 95 \text{ nC}$ at $V_{GS} = 10 \text{ V}$, $I_D = 80 \text{ A}$
- UIS Capability
- Qualified to AEC Q101
- This Device is Pb-Free and is RoHS Compliant

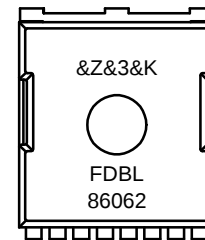
Applications

- Automotive Engine Control
- PowerTrain Management
- Solenoid and Motor Drivers
- Integrated Starter/Alternator
- Primary Switch for 12 V Systems



**H-PSOF8L 11.68x9.80
CASE 100CU**

MARKING DIAGRAM



&Z	= Assembly Plant Code
&3	= Data Code (Year & Week)
&K	= Lot Code
FDBL86062	= Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDBL86062-F085

MOSFET MAXIMUM RATINGS $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Rating	Units
V_{DS}	Drain-to-Source Voltage	100	V
V_{GS}	Gate-to-Source Voltage	± 20	V
I_D	Drain Current - Continuous ($V_{GS} = 10$) (Note 1)	$T_C = 25^\circ\text{C}$	A
	Pulsed Drain Current	$T_C = 25^\circ\text{C}$	
E_{AS}	Single Pulse Avalanche Energy (Note 2)	352	mJ
P_D	Power Dissipation	429	W
	Derate Above 25°C	2.9	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature	-55 to $+175$	$^\circ\text{C}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.35	$^\circ\text{C/W}$
$R_{\theta JA}$	Maximum Thermal Resistance, Junction to Ambient (Note 3)	43	$^\circ\text{C/W}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- Current is limited by silicon.
- Starting $T_J = 25^\circ\text{C}$, $L = 0.1$ mH, $I_{AS} = 84$ A, $V_{DD} = 100$ V during inductor charging and $V_{DD} = 0$ V during time in avalanche.
- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design, while $R_{\theta JA}$ is determined by the board design. The maximum rating presented here is based on mounting on a 1 in² pad of 2oz copper.

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDBL86062	FDBL86062-F085	H-PSOF8L	13"	24 mm	2000 Units

ELECTRICAL CHARACTERISTICS $T_J = 25^\circ\text{C}$, unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	-------

OFF CHARACTERISTICS

B_{VDS}	Drain-to-Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0$ V	100	–	–	V
I_{DSS}	Drain-to-Source Leakage Current	$V_{DS} = 100$ V, $V_{GS} = 0$ V	$T_J = 25^\circ\text{C}$	–	–	5 μA
			$T_J = 175^\circ\text{C}$ (Note 4)	–	–	2 mA
I_{GSS}	Gate-to-Source Leakage Current	$V_{GS} = \pm 20$ V	–	–	± 100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	3.1	4.5	V
$R_{DS(on)}$	Drain to Source On Resistance	$I_D = 80$ A, $V_{GS} = 10$ V	$T_J = 25^\circ\text{C}$	–	1.5	2.0 m Ω
			$T_J = 175^\circ\text{C}$ (Note 4)	–	3.3	4.3

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50$ V, $V_{GS} = 0$ V, $f = 1$ MHz	–	6970	–	pF
C_{oss}	Output Capacitance		–	3950	–	
C_{rss}	Reverse Transfer Capacitance		–	29	–	
R_g	Gate Resistance	$f = 1$ MHz	–	0.4	–	Ω
$Q_{g(TOT)}$	Total Gate Charge at 10 V	$V_{GS} = 0$ to 10 V	$V_{DD} = 80$ V $I_D = 80$ A	–	95	nC
$Q_{g(th)}$	Threshold Gate Charge	$V_{GS} = 0$ to 2 V		–	13	
Q_{gs}	Gate-to-Source Gate Charge			–	31	
Q_{gd}	Gate-to-Drain "Miller" Charge			–	20	

FDBL86062-F085

ELECTRICAL CHARACTERISTICS (continued) $T_J = 25^\circ\text{C}$, unless otherwise noted

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
--------	-----------	-----------------	------	------	------	-------

SWITCHING CHARACTERISTICS

t_{on}	Turn-On Time	$V_{DD} = 50\text{ V}$, $I_D = 80\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\ \Omega$	–	–	73	ns
$t_{d(on)}$	Turn-On Delay		–	31	–	
t_r	Rise Time		–	25	–	
$t_{d(off)}$	Turn-Off Delay		–	36	–	
t_f	Fall Time		–	9	–	
t_{off}	Turn-Off Time		–	–	59	

DRAIN-SOURCE DIODE CHARACTERISTICS

V_{SD}	Source-to-Drain Diode Voltage	$I_{SD} = 80\text{ A}$, $V_{GS} = 0\text{ V}$	–	–	1.25	V
		$I_{SD} = 40\text{ A}$, $V_{GS} = 0\text{ V}$	–	–	1.2	
t_{rr}	Reverse-Recovery Time	$I_F = 80\text{ A}$, $dI_{SD}/dt = 100\text{ A}/\mu\text{s}$, $V_{DD} = 80\text{ V}$	–	115	150	ns
Q_{rr}	Reverse-Recovery Charge		–	172	224	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. The maximum value is specified by design at $T_J = 175^\circ\text{C}$. Product is not tested to this condition in production.

TYPICAL CHARACTERISTICS

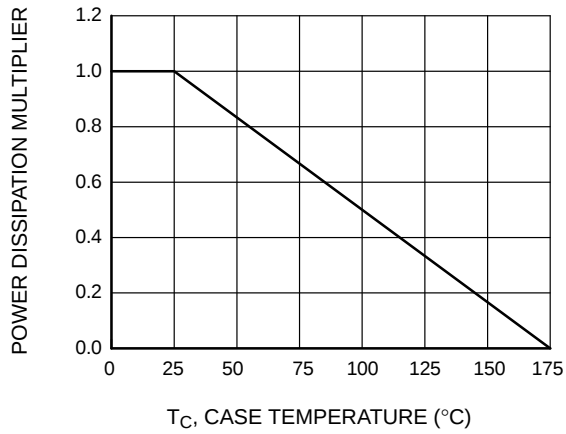


Figure 1. Normalized Power Dissipation vs. Case Temperature

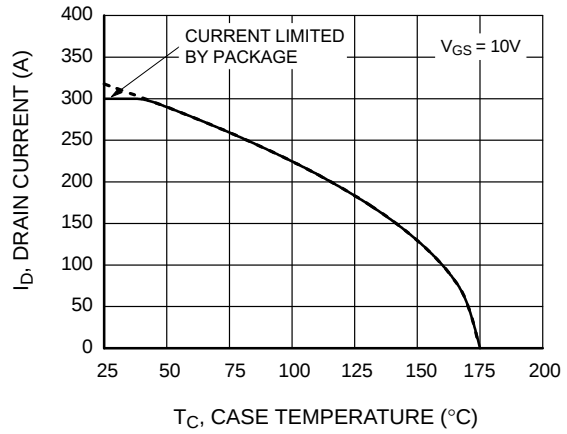


Figure 2. Maximum Continuous Drain Current vs. Case Temperature

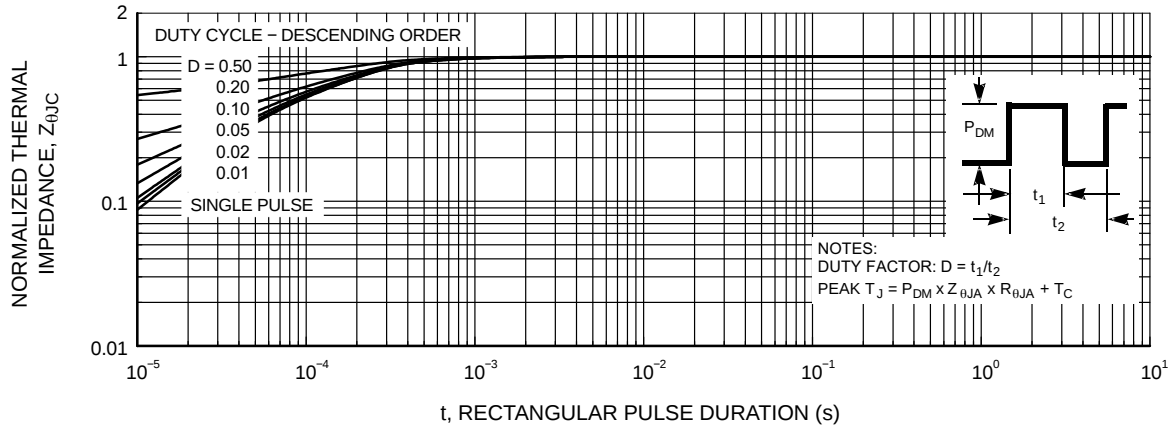


Figure 3. Normalized Maximum Transient Thermal Impedance

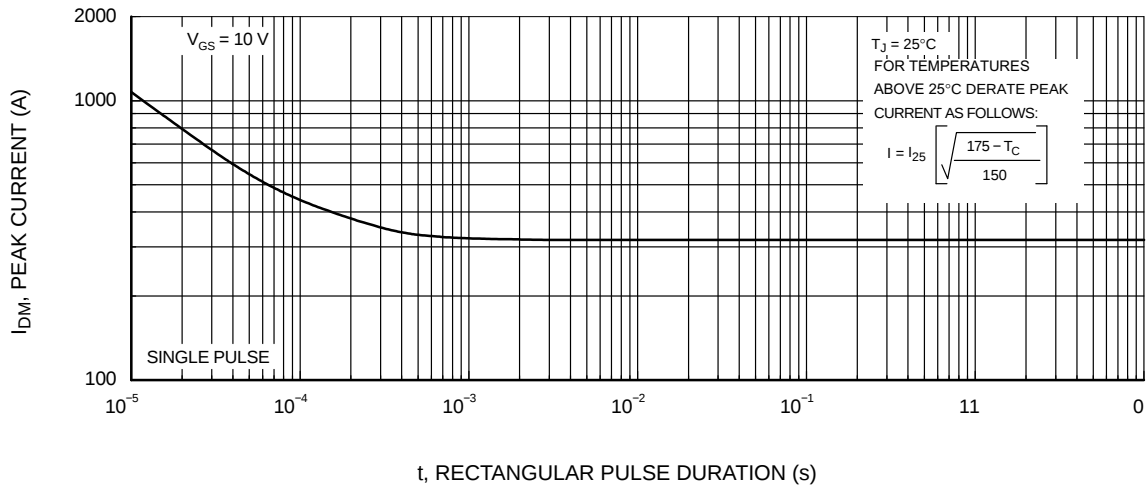


Figure 4. Peak Current Capability

TYPICAL CHARACTERISTICS (CONTINUED)

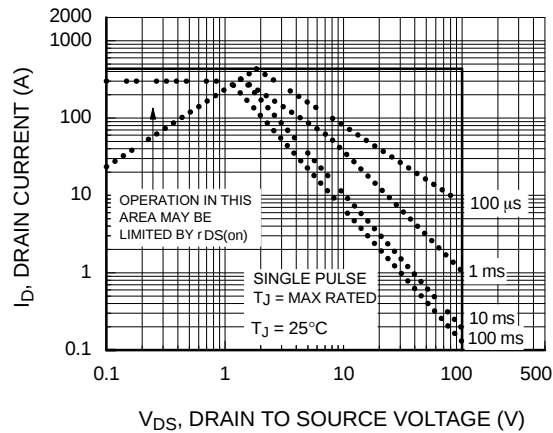


Figure 5. Forward Bias Safe Operating Area

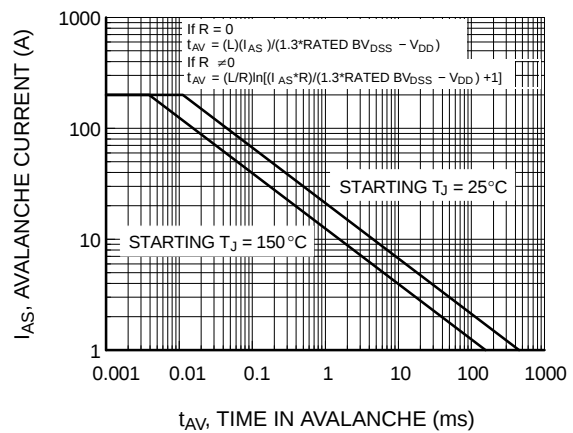


Figure 6. Unclamped Inductive Switching Capability

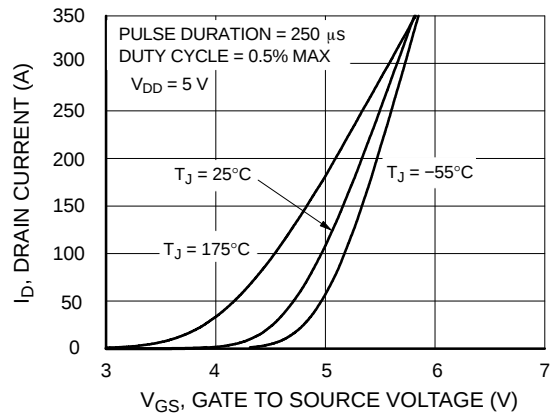


Figure 7. Transfer Characteristics

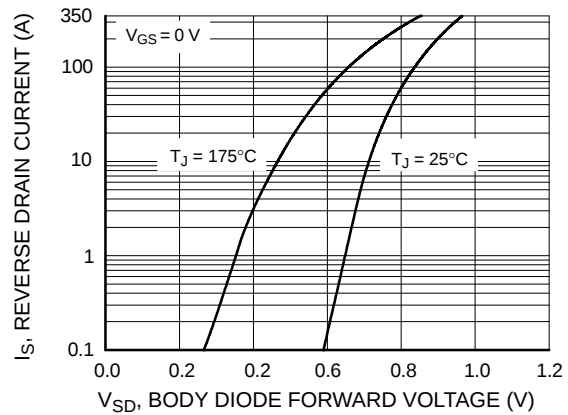


Figure 8. Forward Diode Characteristics

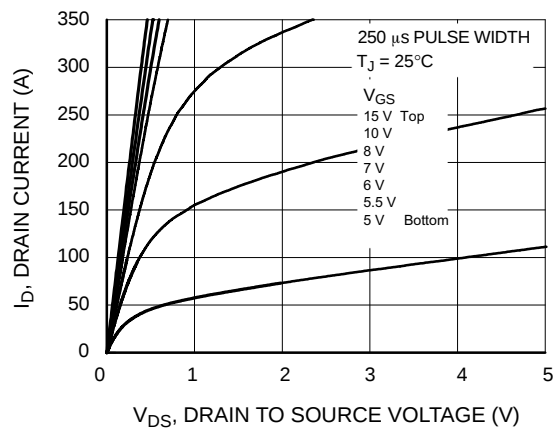


Figure 9. Saturation Characteristics

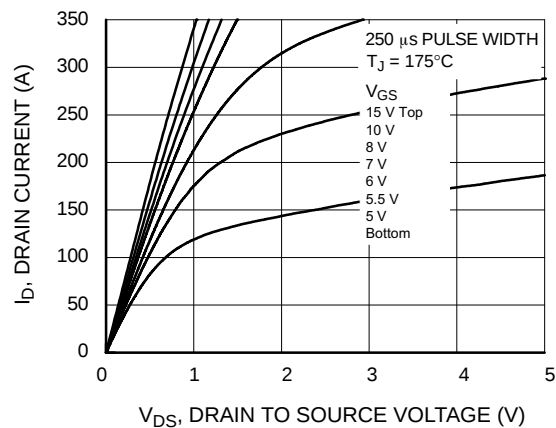


Figure 10. Saturation Characteristics

TYPICAL CHARACTERISTICS (CONTINUED)

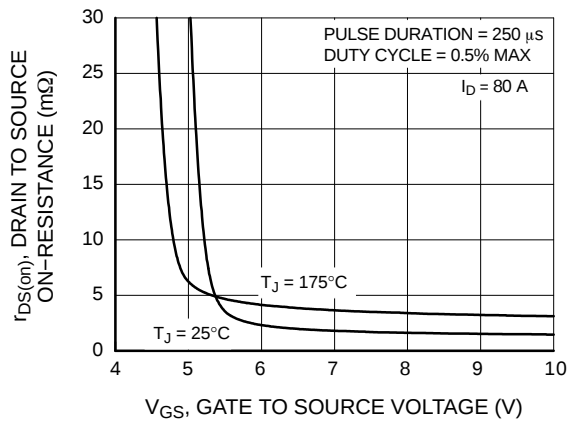


Figure 11. $R_{DS(on)}$ vs. Gate Voltage

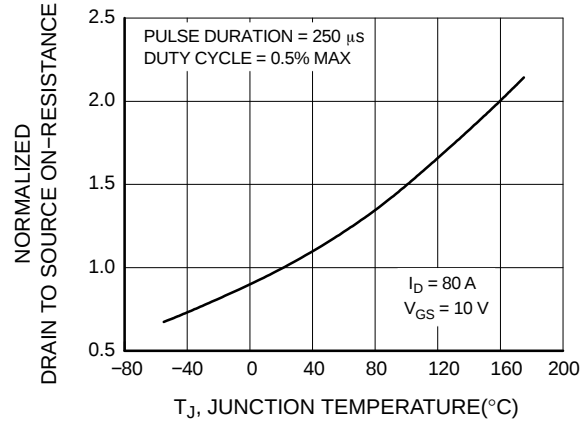


Figure 12. Normalized $R_{DS(on)}$ vs. Junction Temperature

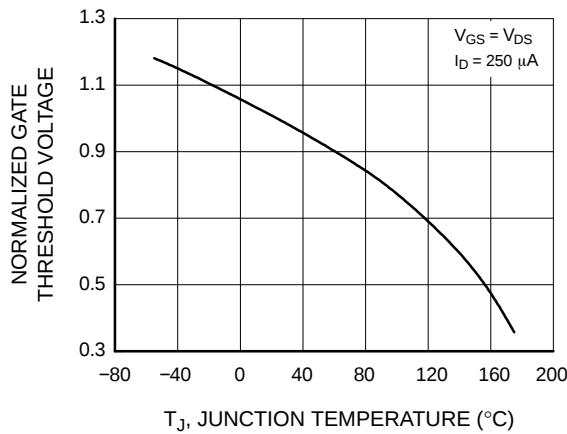


Figure 13. Normalized Gate Threshold Voltage vs. Temperature

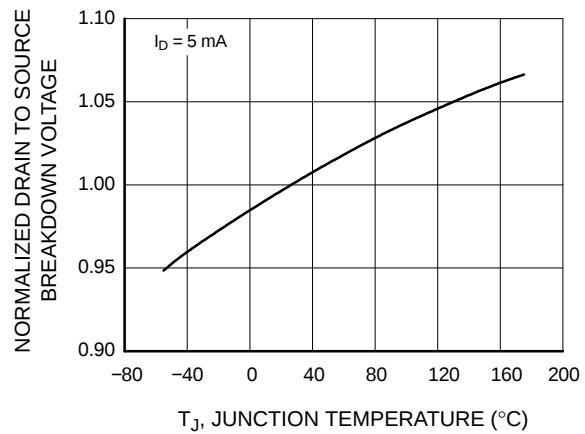


Figure 14. Normalized Drain to Source Breakdown Voltage vs. Junction Temperature

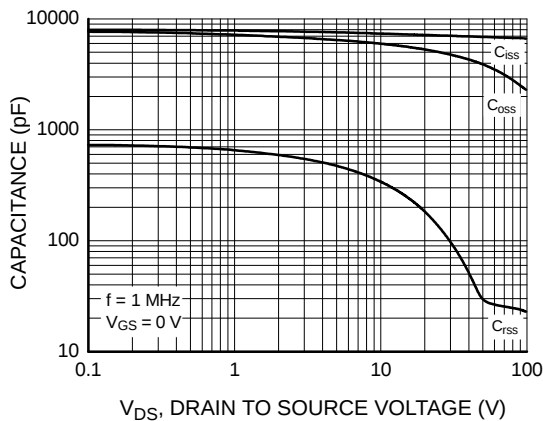


Figure 15. Capacitance vs. Drain to Source Voltage

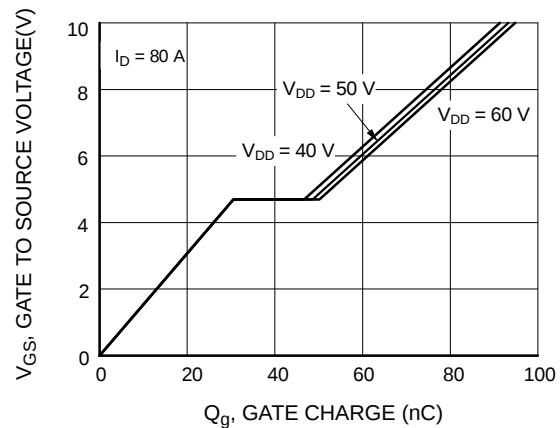
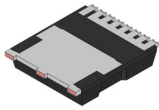
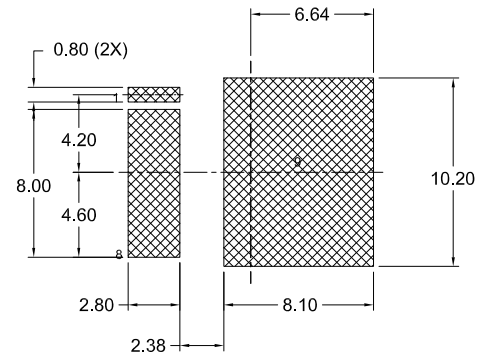
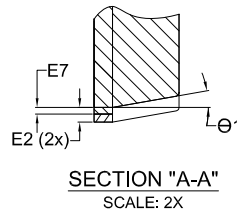
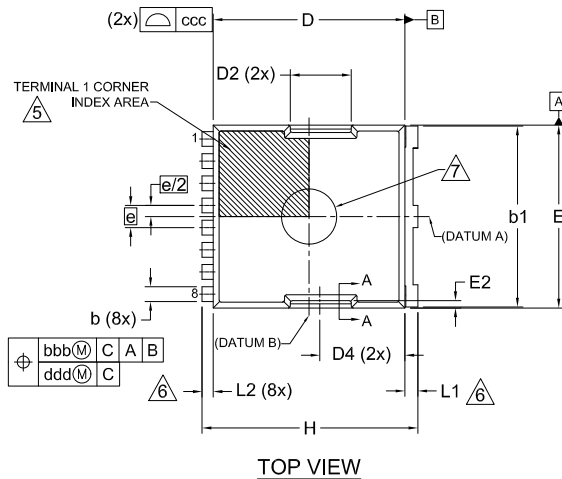


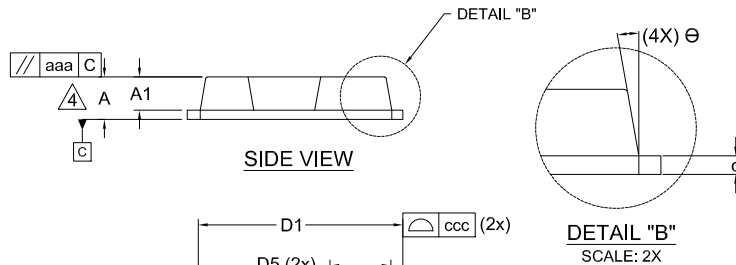
Figure 16. Gate Charge vs. Gate to Source Voltage


H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

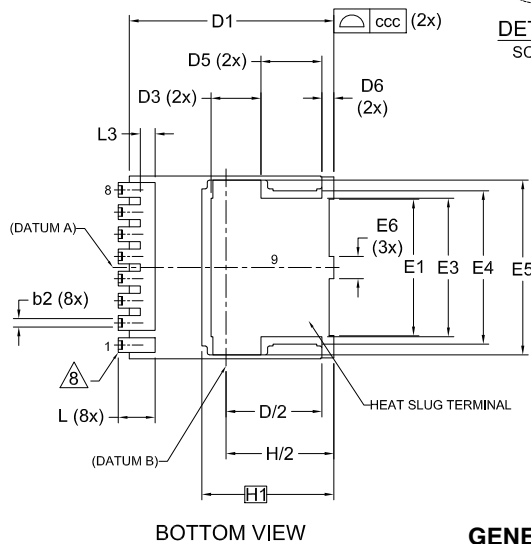
DATE 30 JUL 2024



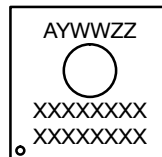
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.


NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.


GENERIC MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

DOCUMENT NUMBER: 98AON13813G

Electronic versions are uncontrolled except when accessed directly from the Document Repository.
Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.

DESCRIPTION: H-PSOF8L 11.68x9.80x2.30, 1.20P

PAGE 1 OF 1

onsemi and onsemi are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at
www.onsemi.com/support/sales