

MOSFET – Power, Single N-Channel, TOLL

40 V, 240 A, 1.21 mΩ

FDBL9406-F085T6

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Q_G and Capacitance to Minimize Driver Losses
- Lowers Switching Noise/EMI
- AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter			Value	Unit
V _{DSS}	Drain-to-Source Voltage			40	V
V _{GS}	Gate-to-Source Voltage			+20/-16	V
I _D	Continuous Drain Current R _{θJC} (Note 2)	Steady State	T _C = 25°C	240	A
			T _C = 100°C	179.4	
P _D	Power Dissipation R _{θJC} (Note 2)		T _C = 25°C	136.4	W
			T _C = 100°C	68.2	
I _D	Continuous Drain Current R _{θJA} (Notes 1, 2)	Steady State	T _A = 25°C	45	A
			T _A = 100°C	31.8	
P _D	Power Dissipation R _{θJA} (Notes 1, 2)		T _A = 25°C	4.3	W
			T _A = 100°C	2.1	
I _{DM}	Pulsed Drain Current	T _A = 25°C, t _p = 10 μs		2817	A
T _J , T _{stg}	Operating Junction and Storage Temperature Range			-55 to +175	°C
I _S	Source Current (Body Diode)			221	A
E _{AS}	Single Pulse Drain-to-Source Avalanche Energy (I _{L(pk)} = 42.5 A)			271	mJ
T _L	Lead Temperature Soldering Reflow for Soldering Purposes (1/8" from case for 10 s)			260	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

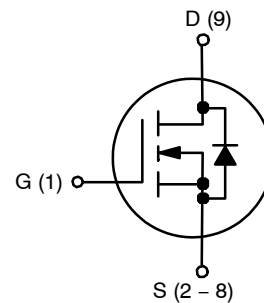
Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Junction-to-Case – Steady State (Note 2)	1.1	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Junction-to-Ambient – Steady State (Note 2)	35	

1. Surface-mounted on FR4 board using a 1 in² pad size, 1 oz. Cu pad.
2. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.

$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
40 V	1.21 mΩ @ 10 V	240 A



H-PSOF8L
CASE 100CU



ORDERING INFORMATION

Device	Package	Shipping†
FDBL9406-F085T6	H-PSOF8L (Pb-Free)	2,000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDBL9406–F085T6

Table 1. ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$	40			V
$V_{(BR)DSS}/T_J$	Drain-to-Source Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, $V_{GS} = 0\ \text{V}$		24.9		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 40\ \text{V}$, $V_{GS} = 0\ \text{V}$ $T_J = 25^\circ\text{C}$			10	μA
I_{GSS}	Gate-to-Source Leakage Current	$V_{DS} = 0\ \text{V}$, $V_{GS} = +20/-16\ \text{V}$			± 100	nA

ON CHARACTERISTICS (Note 3)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 190\ \mu\text{A}$	2	2.8	3.5	V
$V_{GS(th)}/T_J$	Negative Threshold Temperature Coefficient			-6.9		mV/ $^\circ\text{C}$
$R_{DS(on)}$	Drain-to-Source On Resistance	$V_{GS} = 10\ \text{V}$, $I_D = 50\ \text{A}$		1.1	1.21	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 15\ \text{V}$, $I_D = 50\ \text{A}$		143		S

CHARGES & CAPACITANCES

C_{iss}	Input Capacitance	$V_{GS} = 0\ \text{V}$, $V_{DS} = 25\ \text{V}$, $f = 1\ \text{MHz}$		4960		pF
C_{oss}	Output Capacitance			2800		pF
C_{rss}	Reverse Transfer Capacitance			62		pF
$Q_{G(tot)}$	Total Gate Charge	$V_{GS} = 10\ \text{V}$, $V_{DS} = 20\ \text{V}$, $I_D = 50\ \text{A}$		75		nC
$Q_{G(th)}$	Threshold Gate Charge			9		nC
Q_{gs}	Gate-to-Source Charge			22		nC
Q_{gd}	Gate-to-Drain Charge			16		nC

SWITCHING CHARACTERISTICS, $V_{GS} = 10\ \text{V}$ (Note 3)

$t_{d(on)}$	Turn-On Delay Time	$V_{GS} = 10\ \text{V}$, $V_{DS} = 20\ \text{V}$, $I_D = 50\ \text{A}$, $R_G = 6\ \Omega$		27		ns
t_r	Rise Time			44		ns
$t_{d(off)}$	Turn-Off Delay Time			61		ns
t_f	Fall Time			26		ns

DRAIN-SOURCE DIODE CHARACTERISTICS

V _{SD}	Forward Diode Voltage	I _S = 50 A, V _{GS} = 0 V	T _J = 25°C		0.8	1.2	V
		I _S = 50 A, V _{GS} = 0 V	T _J = 125°C		0.6		V
t _{rr}	Reverse Recovery Time	V _{GS} = 0 V, dI _S /dt = 100 A/μs, I _S = 50 A			78		ns
t _a	Charge Time				39		ns
t _b	Discharge Time				39		ns
Q _{rr}	Reverse Recovery Charge				101		nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Switching characteristics are independent of operating junction temperatures

TYPICAL CHARACTERISTICS

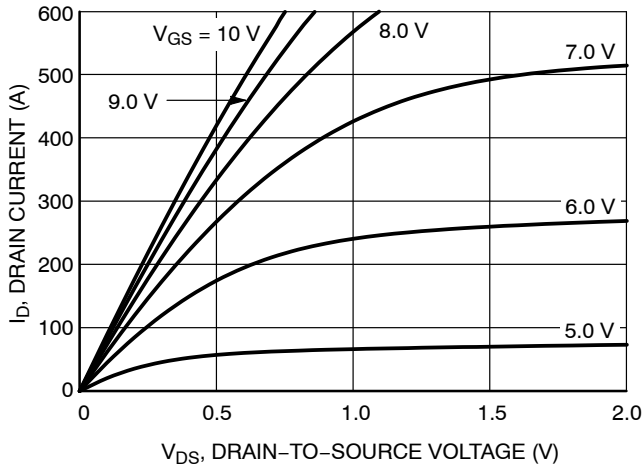


Figure 1. On-Region Characteristics

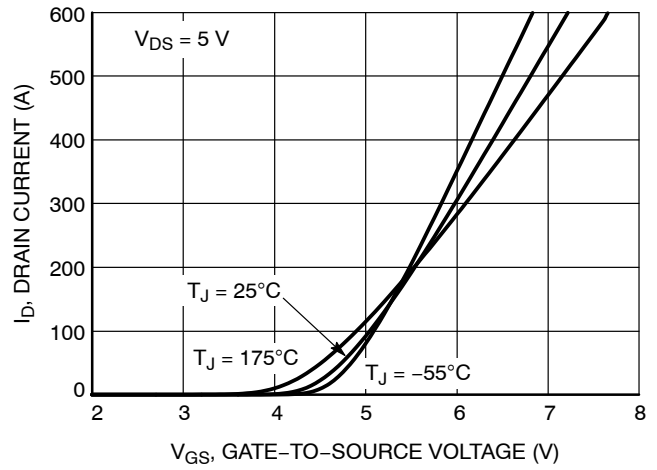


Figure 2. Transfer Characteristics

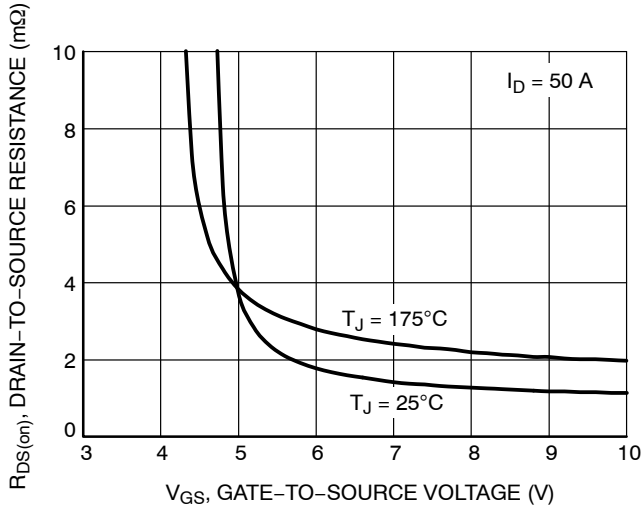


Figure 3. On-Resistance vs. Gate-to-Source Voltage

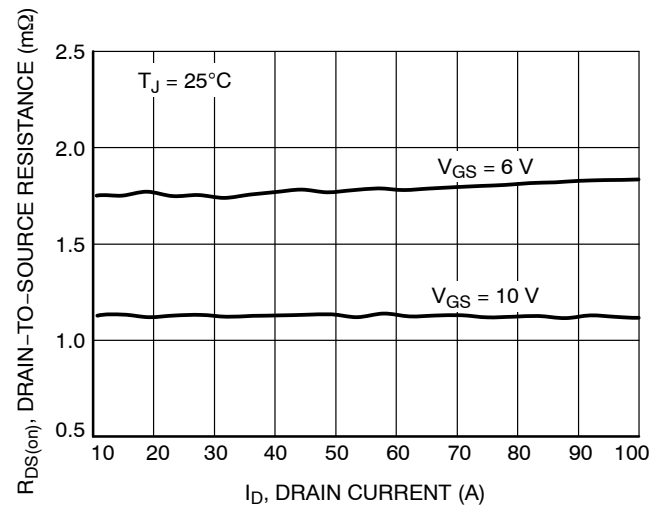


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

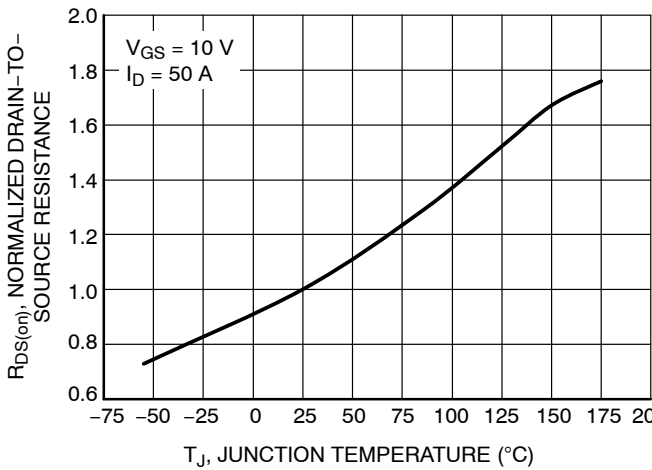


Figure 5. On-Resistance Variation with Temperature

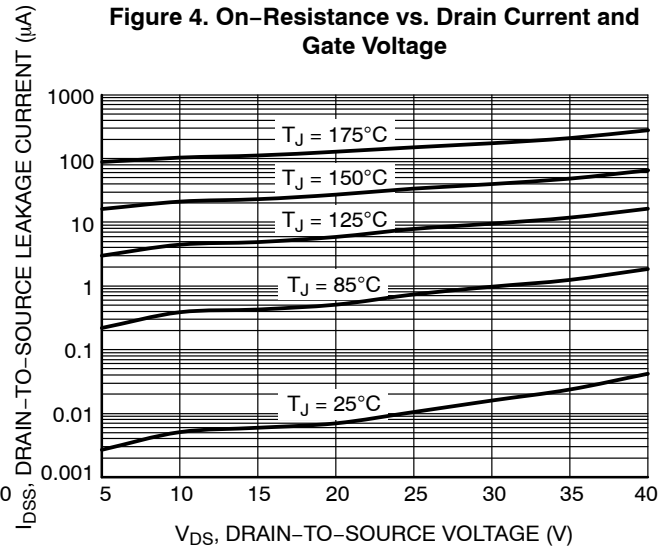


Figure 6. Drain-to-Source Leakage Current vs. Voltage

TYPICAL CHARACTERISTICS (continued)

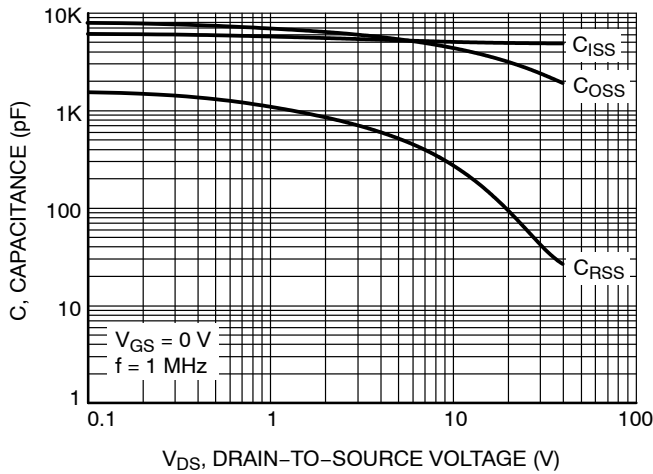


Figure 7. Capacitance Variation

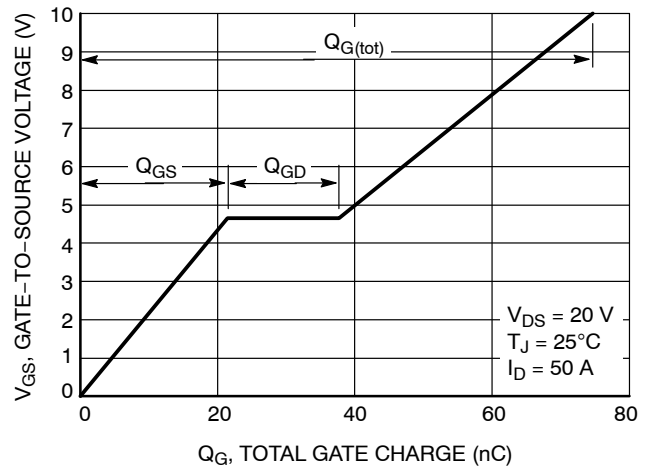


Figure 8. Gate-to-Source Voltage vs. Total Charge

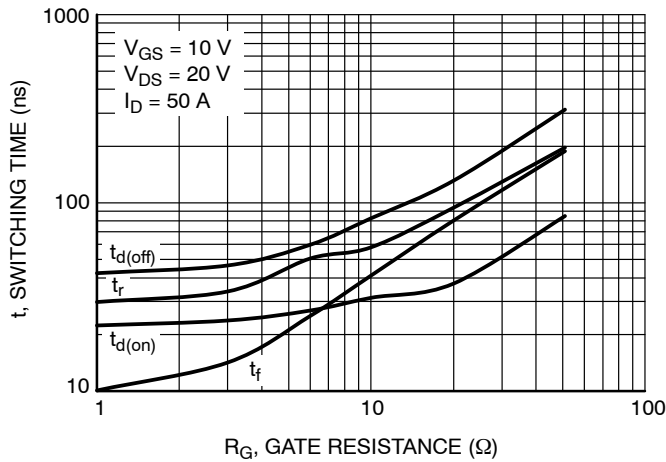


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

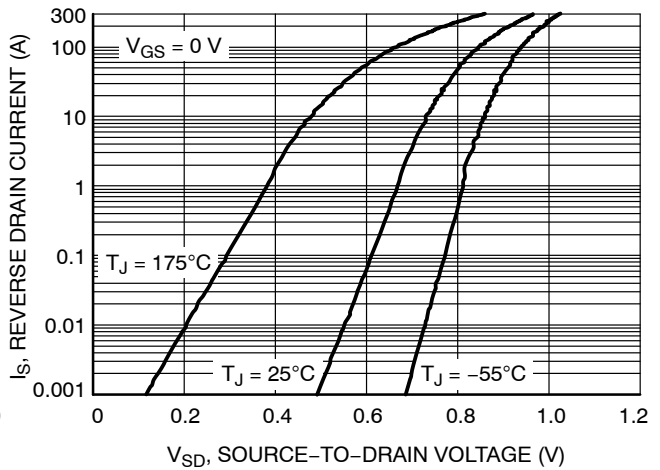


Figure 10. Diode Forward Voltage vs. Current

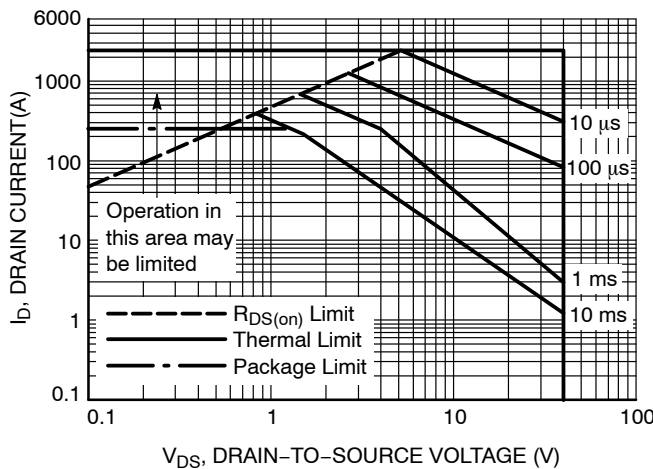


Figure 11. Maximum Rated Forward Biased Safe Operating Area

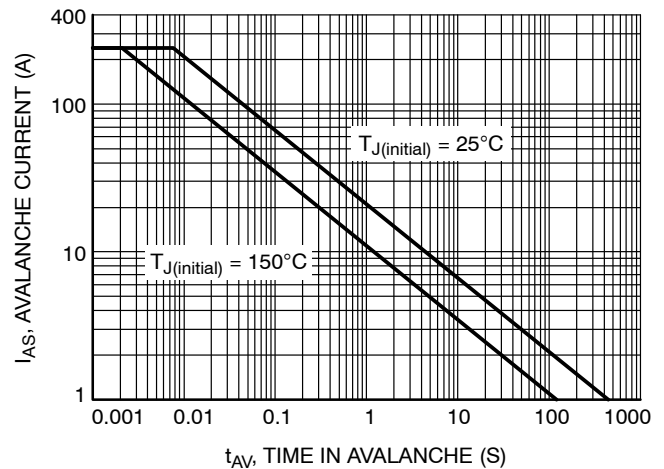


Figure 12. Maximum Drain Current vs. Time in Avalanche

TYPICAL CHARACTERISTICS (continued)

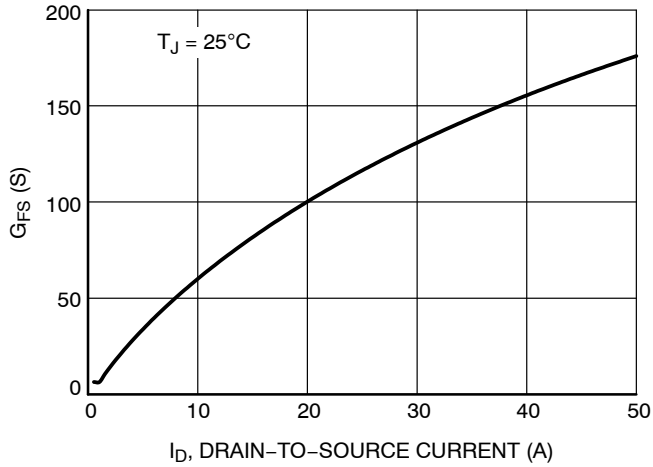


Figure 13. G_{FS} vs. I_D

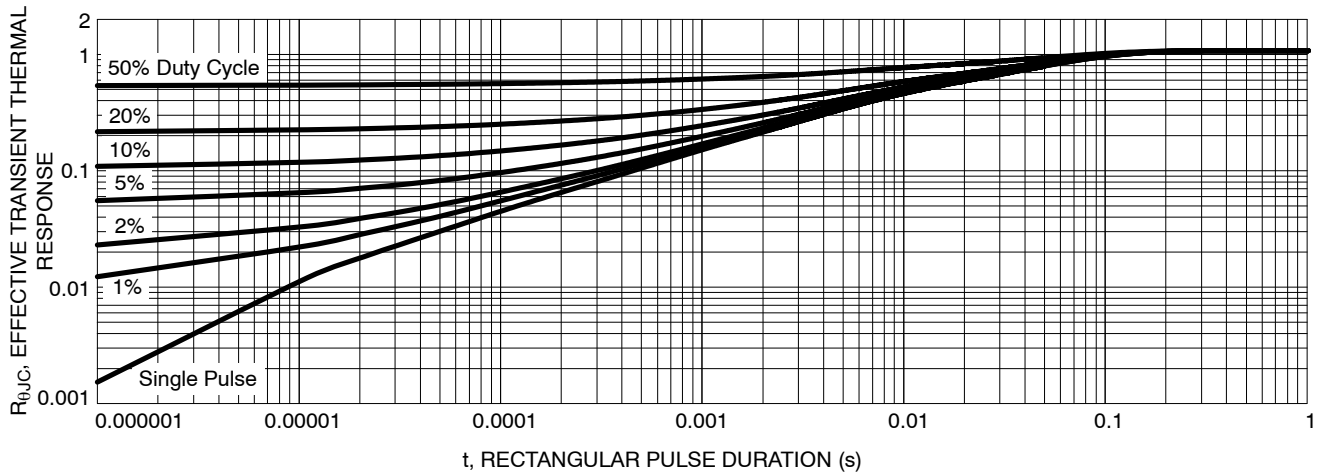
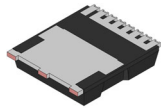


Figure 14. Thermal Response


H-PSOF8L 11.68x9.80x2.30, 1.20P
CASE 100CU
ISSUE F

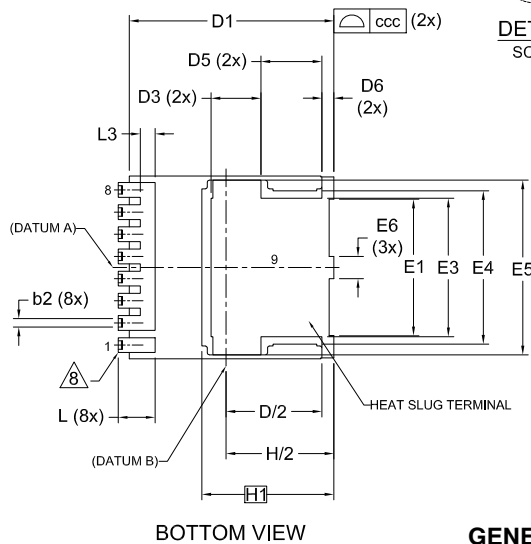
DATE 30 JUL 2024



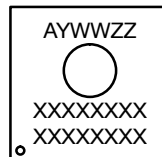
*FOR ADDITIONAL INFORMATION ON OUR Pb-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ONSEMI SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.


NOTES:

1. PACKAGE STANDARD REFERENCE: JEDEC MO-299, ISSUE B.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2018.
3. "e" REPRESENTS THE TERMINAL PITCH.
4. THIS DIMENSION INCLUDES ENCAPSULATION THICKNESS "A1", AND PACKAGE BODY THICKNESS, BUT DOES NOT INCLUDE ATTACHED FEATURES, e.g., EXTERNAL OR CHIP CAPACITORS. AN INTEGRAL HEATSLUG IS NOT CONSIDERED AS ATTACHED FEATURE.
5. A VISUAL INDEX FEATURE MUST BE LOCATED WITHIN THE HATCHED AREA.
6. DIMENSIONS b1, L1, L2 APPLY TO PLATED TERMINALS.
7. THE LOCATION AND SIZE OF EJECTOR MARKS ARE OPTIONAL.
8. THE LOCATION AND NUMBER OF FUSED LEADS ARE OPTIONAL.


GENERIC MARKING DIAGRAM*

A = Assembly Location
Y = Year
WW = Work Week
ZZ = Assembly Lot Code
XXXX = Specific Device Code



*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	2.20	2.30	2.40
A1	1.70	1.80	1.90
b	0.70	0.80	0.90
b1	9.70	9.80	9.90
b2	0.35	0.45	0.55
c	0.40	0.50	0.60
D	10.28	10.38	10.48
D/2	5.09	5.19	5.29
D1	10.98	11.08	11.18
D2	3.20	3.30	3.40
D3	2.60	2.70	2.80
D4	4.45	4.55	4.65
D5	3.20	3.30	3.40
D6	0.55	0.65	0.75
E	9.80	9.90	10.00
E1	7.30	7.40	7.50
E2	0.30	0.40	0.50
E3	7.40	7.50	7.60
E4	8.20	8.30	8.40

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
E5	9.36	9.46	9.56
E6	1.10	1.20	1.30
E7	0.15	0.18	0.21
e	1.20 BSC		
e/2	0.60 BSC		
H	11.58	11.68	11.78
H/2	5.74	5.84	5.94
H1	7.15 BSC		
L	1.90	2.00	2.10
L1	0.60	0.70	0.80
L2	0.50	0.60	0.70
L3	0.70	0.80	0.90
Θ	10° REF		
Θ1	10° REF		
aaa	0.20		
bbb	0.25		
ccc	0.20		
ddd	0.20		
eee	0.10		

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DESCRIPTION: H-PSOF8L 11.68x9.80x2.30, 1.20P

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