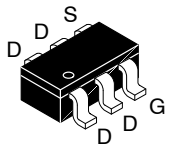
MOSFET – P-Channel, 2.5 V Specified, POWERTRENCH®

-20 V, -4.5 A, 43 mΩ

FDC638APZ

V_{DS}	$r_{DS(on)}$ MAX	I_D MAX
−20 V	43 mΩ @ −4.5 V	−4.5 A
	68 mΩ @ −2.5 V	



TSOT23 6−Lead
SUPERSOT™ −6
CASE 419BL

General Description

This P−Channel 2.5 V specified MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance and yet maintain low gate charge for superior switching performance.

These devices are well suited for battery power applications: load switching and power management, battery charging circuits, and DC/DC conversion.

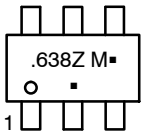
Features

- Max $r_{DS(on)}$ = 43 mΩ at V_{GS} = −4.5 V, I_D = −4.5 A
- Max $r_{DS(on)}$ = 68 mΩ at V_{GS} = −2.5 V, I_D = −3.8 A
- Low Gate Charge (8 nC typical)
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- SUPERSOT™ −6 Package: Small Footprint (72% smaller than Standard SO−8) Low Profile (1 mm thick)
- This Device is Pb−Free, Halide Free and is RoHS Compliant

Application

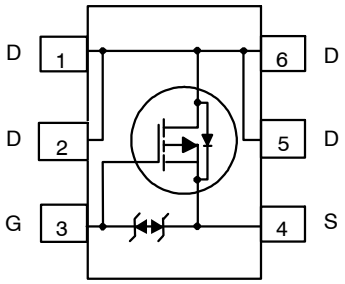
- DC−DC Conversion

MARKING DIAGRAM



.638Z = Specific Device Code
M = Date Code
▪ = Pb−Free Package
(Note: Microdot may be in either location)

PINOUT



ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter		Ratings	Units
V_{DS}	Drain to Source Voltage		−20	V
V_{GS}	Gate to Source Voltage		±12	V
I_D	Drain Current	Continuous (Note 1a)	−4.5	A
		Pulsed	−20	
P_D	Power Dissipation	(Note 1a)	1.6	W
		(Note 1b)	0.8	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Ratings	Units
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1b)	156	°C/W

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−20			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C		−9.4		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −16 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −16 V, V_{GS} = 0 V, T_J = 55°C			−10	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±12 V, V_{DS} = 0 V			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−0.4	−0.8	−1.5	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C		2.9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −4.5 V, I_D = −4.5 A		37	43	mΩ
		V_{GS} = −2.5 V, I_D = −3.8 A		52	68	
		V_{GS} = −4.5 V, I_D = −4.5 A, T_J = 125°C		50	72	
$I_{D(on)}$	On−State Drain Current	V_{GS} = −10 V, V_{DS} = −4.5 A	−20			A
g_{FS}	Forward Transconductance	V_{DS} = −10 V, I_D = −4.5 A		18		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −10 V, V_{GS} = 0 V, f = 1 MHz		750	1000	pF
C_{oss}	Output Capacitance			155	210	pF
C_{rss}	Reverse Transfer Capacitance			130	195	pF
SWITCHING CHARACTERISTICS (Note 2)						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −5 V, I_D = −4.5 A, V_{GS} = −4.5 V, R_{GEN} = 6 Ω		6	12	ns
t_r	Rise Time			20	31	ns
$t_{d(off)}$	Turn−Off Delay Time			48	77	ns
t_f	Fall Time			47	72	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to −4.5 V, V_{DD} = −5 V, I_D = −4.5 A		8	12	nC
Q_{gs}	Gate to Source Gate Charge	V_{DD} = −5 V, I_D = −4.5 A		2		nC
Q_{gd}	Gate to Drain “Miller” Charge			2		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
I_S	Maximum Continuous Drain−Source Diode Forward Current				−1.3	A
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −1.3 A (Note 2)		−0.8	−1.2	V
t_{rr}	Reverse Recovery Time	I_F = −4.5 A, di/dt = 100 A/μs		24	36	ns
Q_{rr}	Reverse Recovery Charge			13	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction−to−case and case−to−ambient resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by user’s board design.

a. 78°C/W when mounted on a 1 in^2 pad of 2 oz. copper on FR−4 board

b. 156°C/W when mounted on a minimum pad of 2 oz. copper

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.

TYPICAL CHARACTERISTICS

(T_J = 25°C unless otherwise noted)

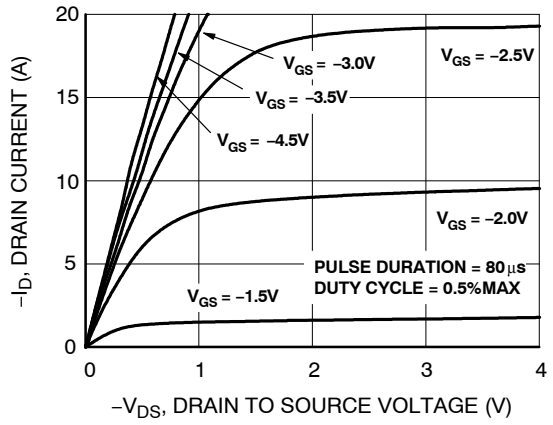

Figure 1. On−Region Characteristics

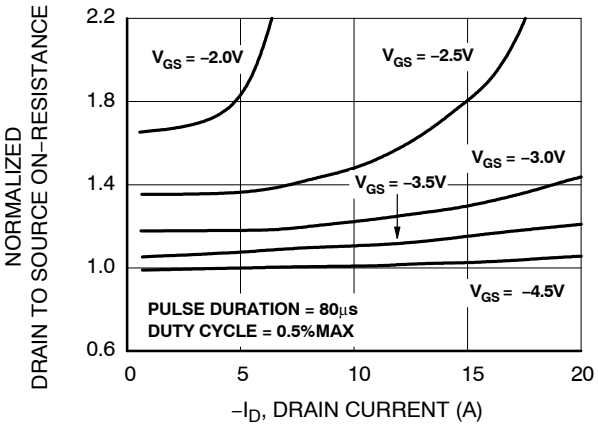

Figure 2. Normalized On−Resistance vs Drain Current and Gate Voltage

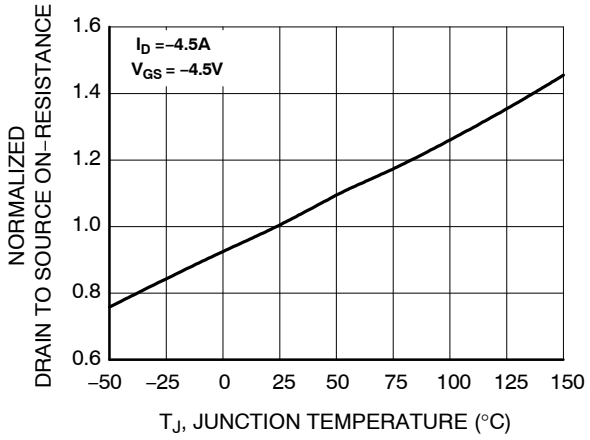

Figure 3. Normalized On−Resistance vs Junction Temperature

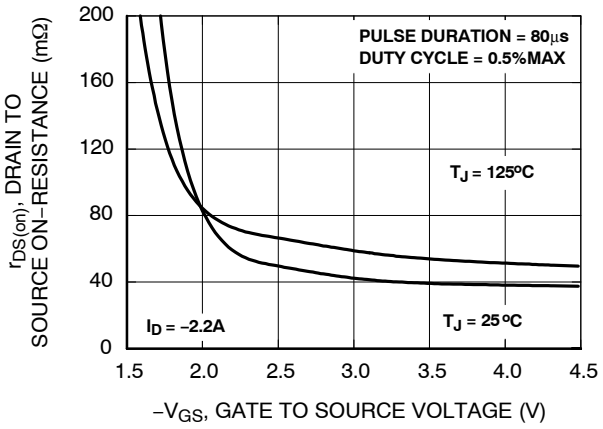

Figure 4. On−Resistance vs Gate to Source Voltage

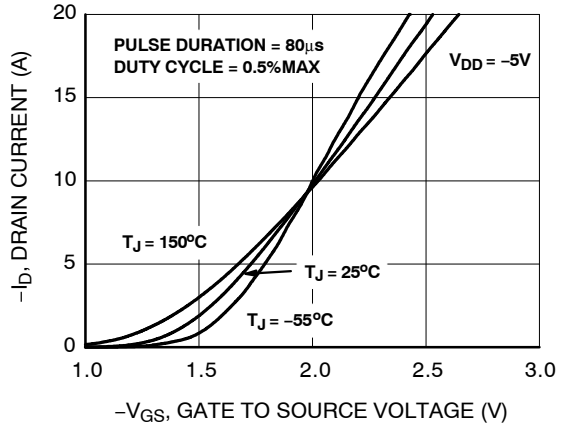

Figure 5. Transfer Characteristics

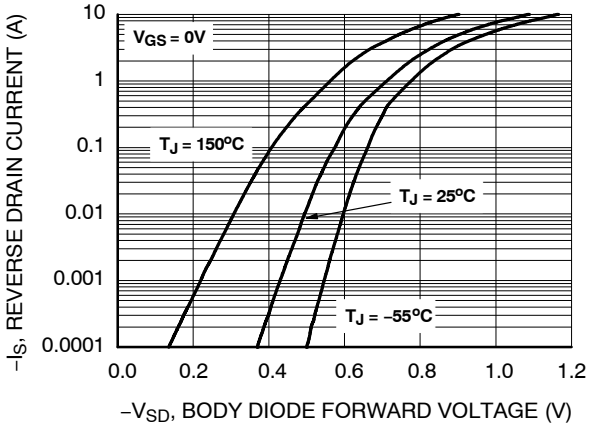

Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (continued)

(T_J = 25°C unless otherwise noted)

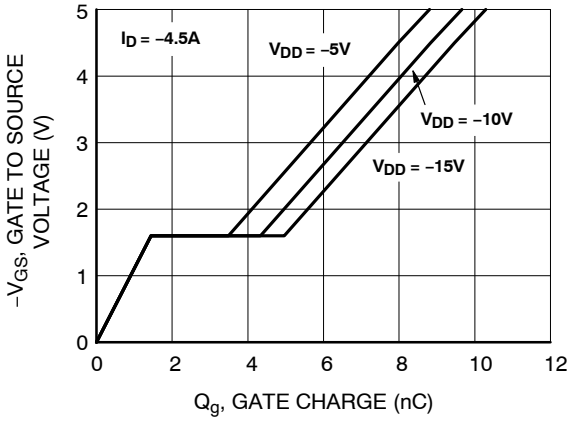

Figure 7. Gate Charge Characteristics

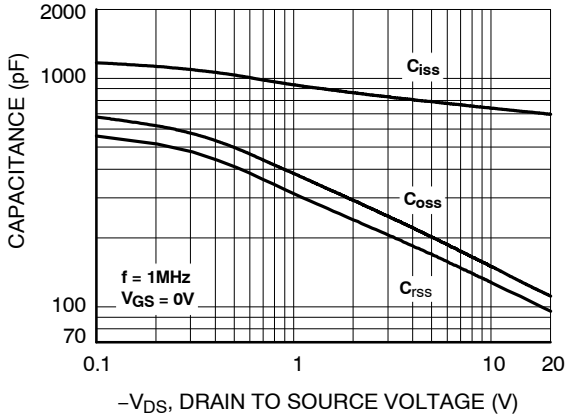

Figure 8. Capacitance vs Drain to Source Voltage

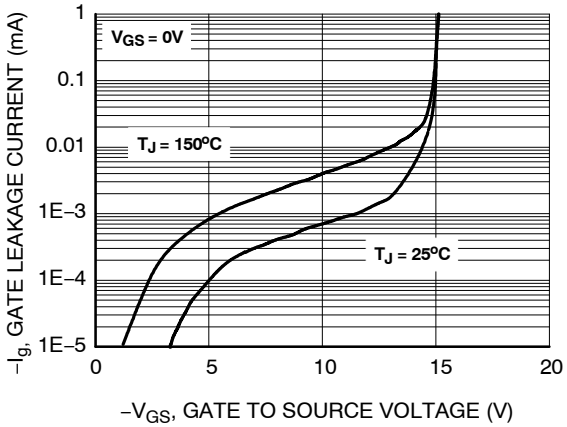

Figure 9. Gate Leakage Current vs. Gate to Source Voltage

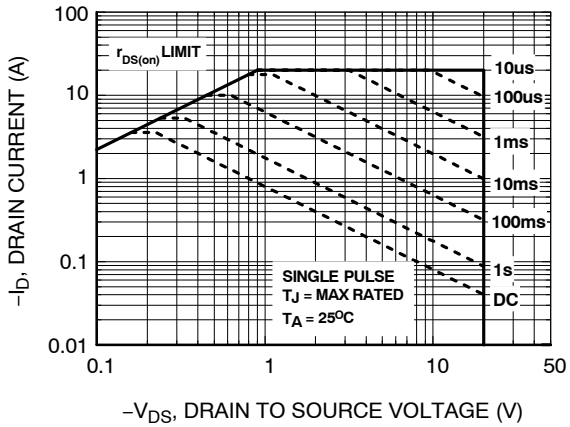

Figure 10. Forward Bias Safe Operating Area

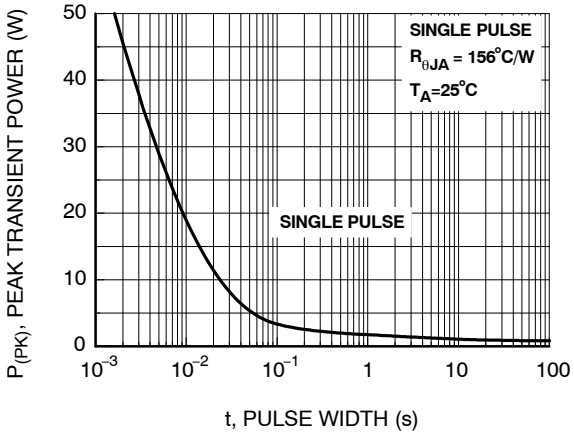

Figure 11. Single Pulse Maximum Power Dissipation

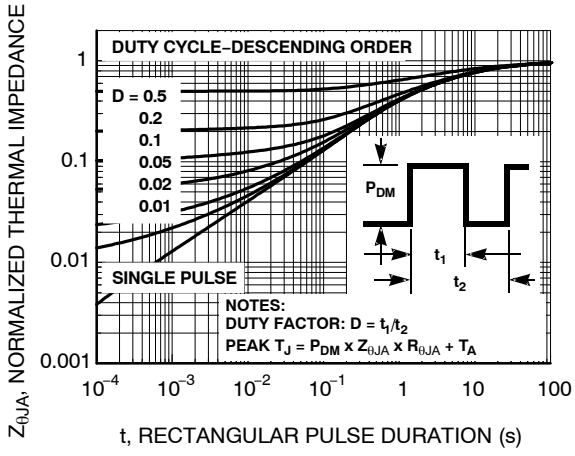

Figure 12. Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDC638APZ	.638Z	TSOT−23−6 (Pb−Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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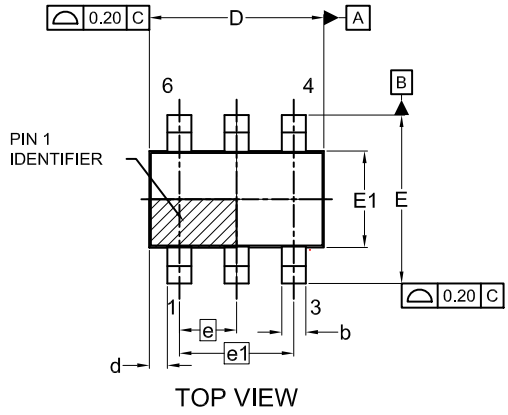
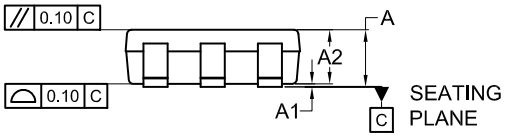
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

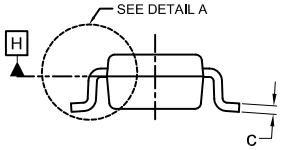


TOP VIEW

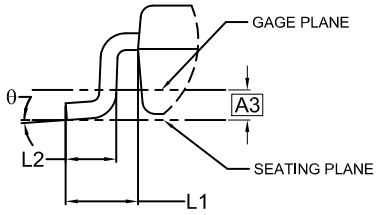


FRONT VIEW

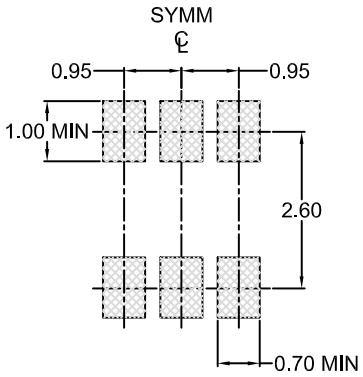
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

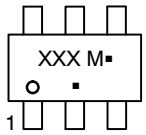
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

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