MOSFET – N-Channel, POWERTRENCH®
30 V, 8.0 A, 16 mΩ

FDC8878

1
TSOT 23 6−Lead
(SUPERSOT™−6)
CASE 419BL

Description

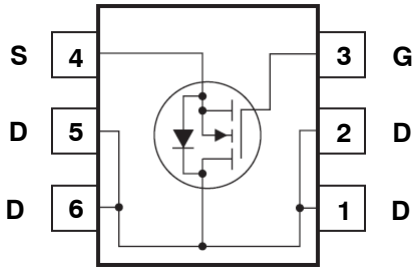
This N−Channel MOSFET is Produced Using **onsemi**'s Advanced POWERTRENCH Process that has been Optimized for $R_{DS(on)}$, switching performance.

Features

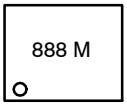
- Max $R_{DS(on)}$ = 16 mΩ at V_{GS} = 10 V, I_D = 8.0 A
- Max $R_{DS(on)}$ = 18 mΩ at V_{GS} = 4.5 V, I_D = 7.5 A
- High Performance trench technology for extremely low $R_{DS(on)}$
- Fast Switching Speed
- These Devices is Pb−Free, Halide Free and is RoHS Compliant

Applications

- Primary Switch



MARKING DIAGRAM



888 = Specific Device Code
M = Date Code

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage (Note 3)	±20	V
I_D	Drain Current – Continuous (Package Limited) T_C = 25°C – Continuous T_A = 25°C (Note 1a) – Pulsed	 8.0 8.0 32	A
P_D	Power Dissipation T_A = 25°C (Note 1a)	1.6	W
	Power Dissipation T_A = 25°C (Note 1b)	0.8	
T_J, T_{stg}	Operating and Storage Junction Temperature Range	−55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resitance, Juntion to Case	30	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	78	°C/W

ORDERING INFORMATION

Device	Package	Shipping†
FDC8878	TSOT−23−6 (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

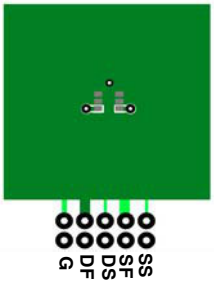
ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = 250 μA, V_{GS} = 0 V	30	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	13	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = 24 V, V_{GS} = 0 V	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current Forward	V_{GS} = 20 V, V_{DS} = 0 V	–	–	100	nA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = 250 μA	1.2	1.6	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = 250 μA, Referenced to 25°C	–	–5	–	mV/°C
$R_{DS(on)}$	Static Drain–Source On–Resistance	V_{GS} = 10 V, I_D = 8.0 A V_{GS} = 4.5 V, I_D = 7.5 A, V_{GS} = 10 V, I_D = 8.0 A, T_J = 125°C	– – –	12 14 16	16 18 21	mΩ
g_{FS}	Forward Transconductance	V_{DD} = 5 V, I_D = 8.0 A		43	–	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = 15 V, V_{GS} = 0 V, f = 1 MHz	–	782	1040	pF
C_{oss}	Output Capacitance		–	318	425	pF
C_{rss}	Reverse Transfer Capacitance		–	40	60	pF
R_g	Gate Resistance		–	1.2	–	Ω
Switching Characteristics						
$t_{d(on)}$	Turn–On Delay Time	V_{DD} = 15 V, I_D = 8 A, V_{GS} = 10 V, R_{GEN} = 6 Ω	–	6	12	ns
t_r	Rise Time		–	2	10	ns
$t_{d(off)}$	Turn–Off Delay Time		–	17	30	ns
t_f	Fall Time		–	2	10	ns
$Q_{g(TOT)}$	Total Gate Charge	V_{GS} = 0 V to 10 V V_{DD} = 15 V, I_D = 8 A	–	13	18	nC
		V_{GS} = 0 V to 4.5 V, V_{DD} = 15 V, I_D = 8 A	–	6	9	nC
Q_{gs}	Total Gate Charge	V_{DD} = 15 V, I_D = 8 A	–	1.7	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	2.0	–	nC
Drain–Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = 8.0 A (Note 2)	–	0.8	1.2	V
t_{rr}	Reverse Recovery Time	I_F = 8.0 A, di/dt = 100 A/μs	–	22	35	ns
Q_{rr}	Reverse Recovery Charge		–	7	14	nC

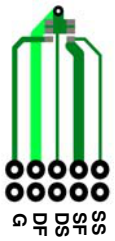
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user’s board design.



a. 78 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 175 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2.0%
3. As an N–ch device, the Negative Vgs Rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

TYPICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

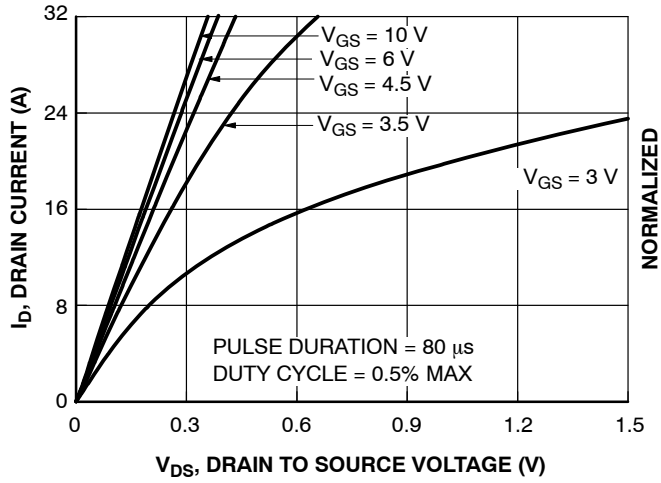


Figure 1. On−Region Characteristics

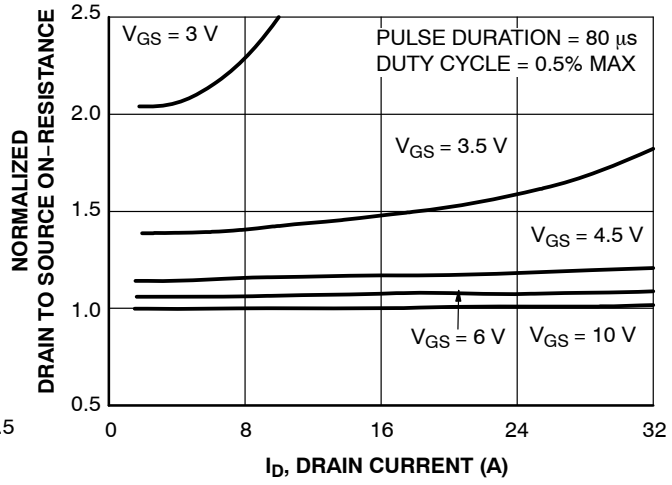


Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

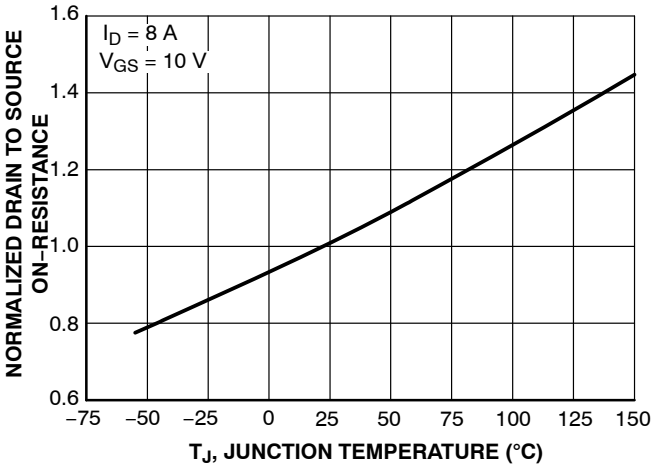


Figure 3. Normalized On−Resistance vs Junction Temperature

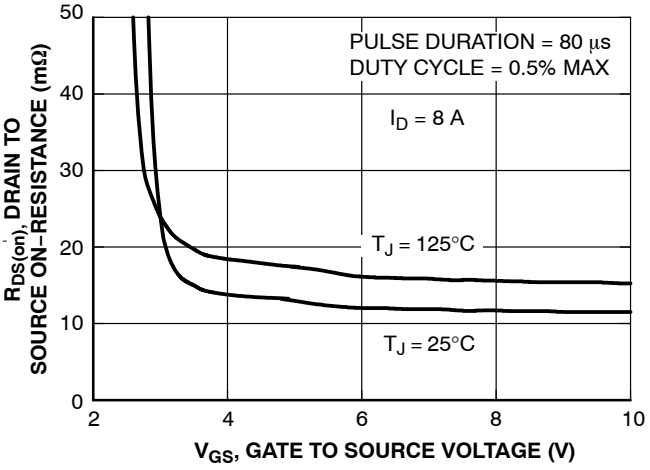


Figure 4. On−Resistance vs Gate to Source Voltage

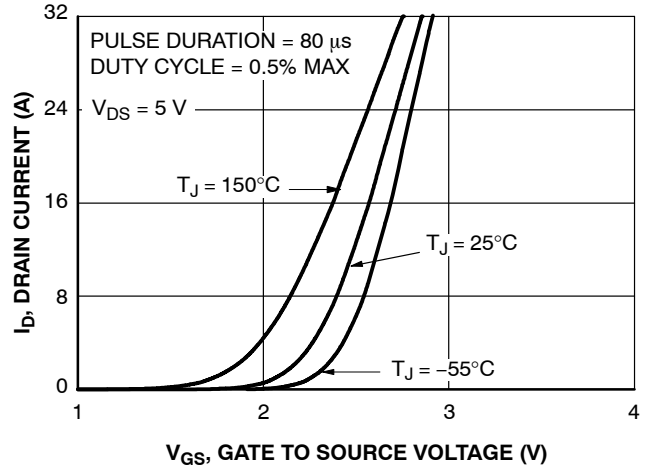


Figure 5. Transfer Characteristics

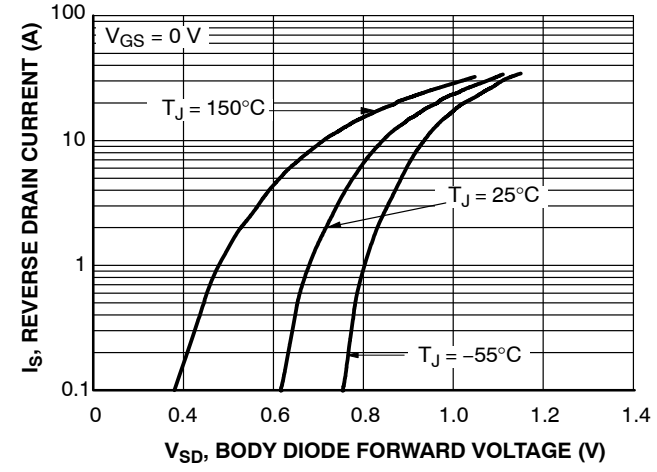


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (CONTINUED) (T_J = 25°C unless otherwise noted)

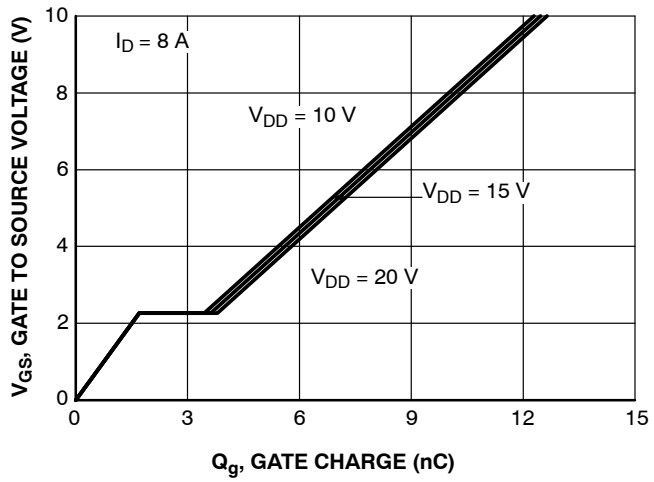


Figure 7. Gate Charge Characteristics

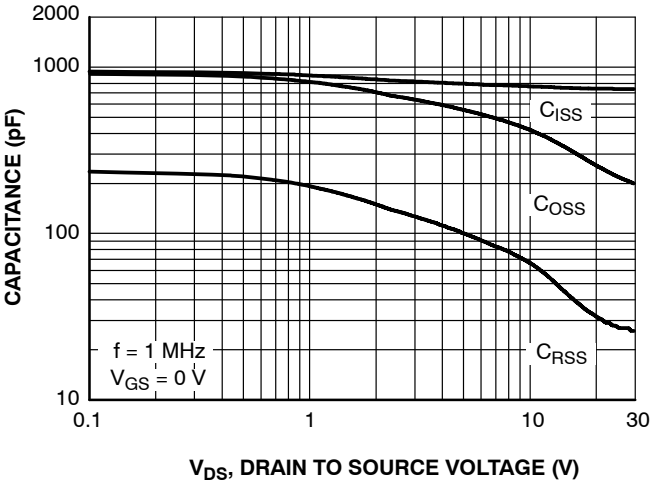


Figure 8. Capacitance vs Drain to Source Voltage

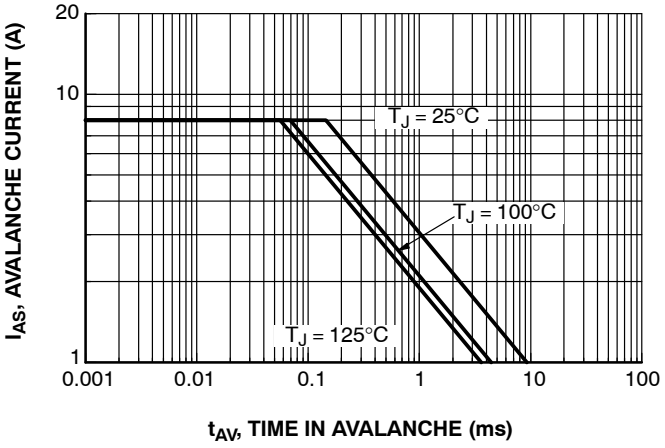


Figure 9. Unclamped Inductive Switching Capability

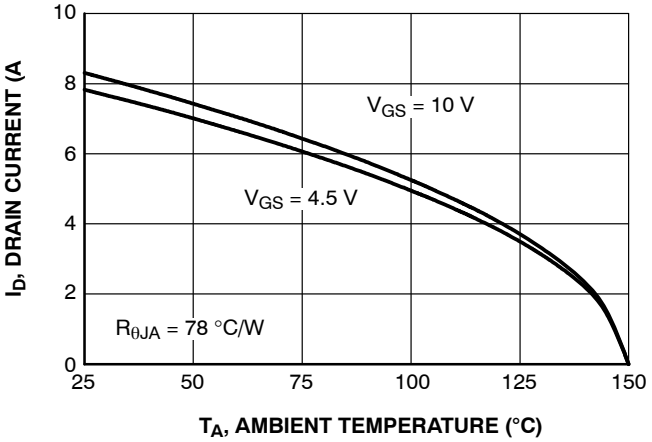


Figure 10. Maximum Continous Drain Current vs. Ambient Temperature

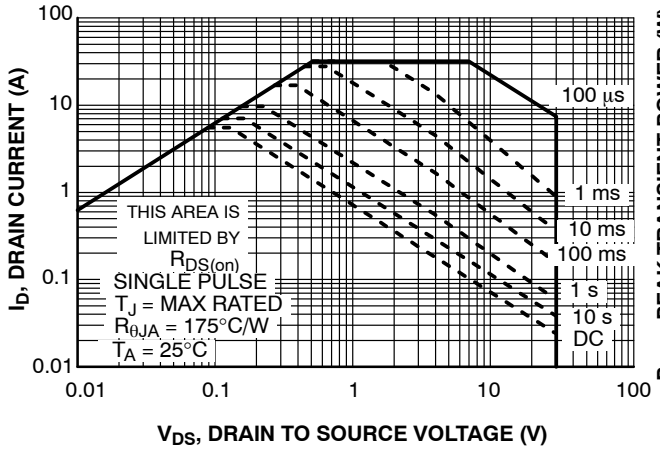


Figure 11. Forward Bias Safe Operating Area

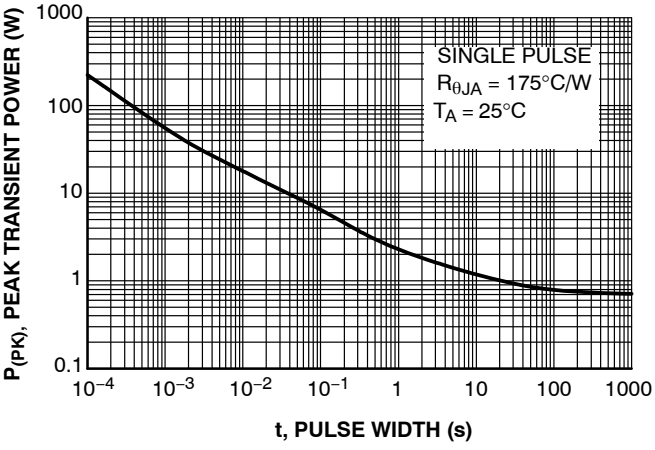


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (CONTINUED) (T_J = 25°C unless otherwise noted)

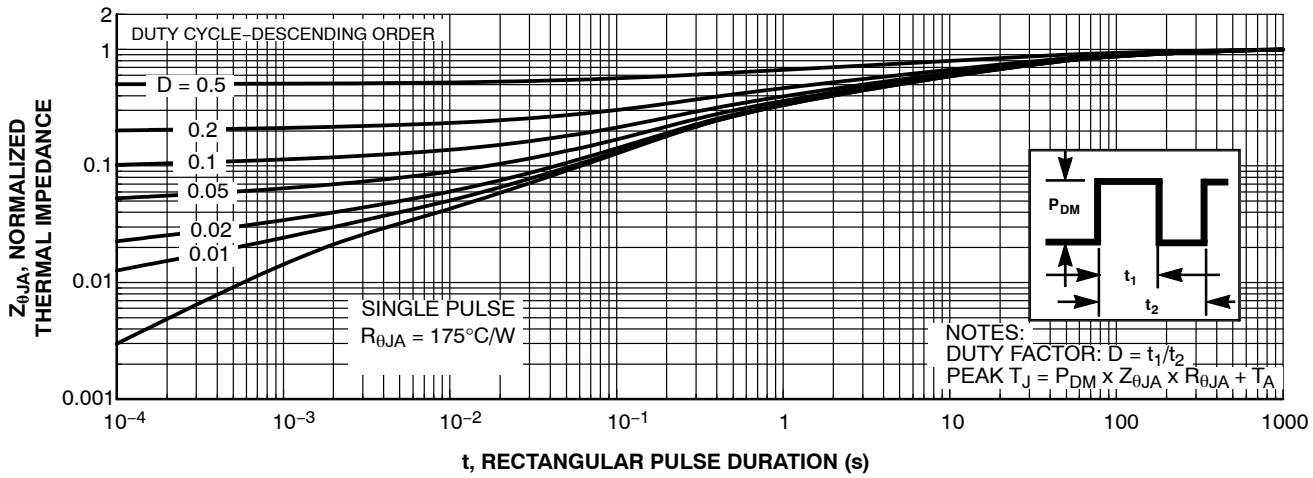
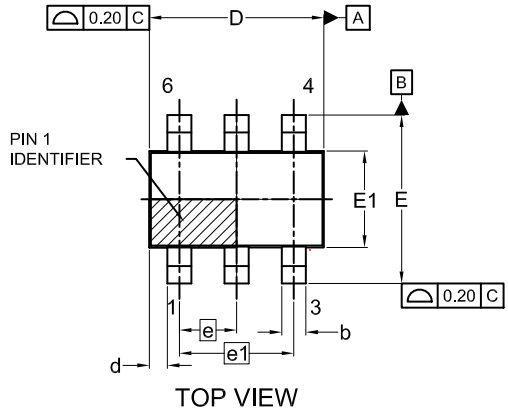


Figure 13. Junction−to−Ambient Transient Thermal Response Curve

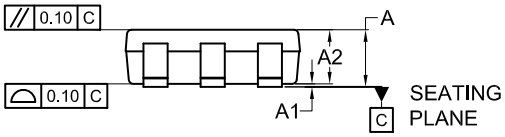
1
SCALE 2:1

TSOT23 6−Lead
CASE 419BL
ISSUE A

DATE 31 AUG 2020

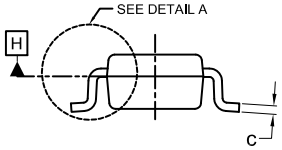


TOP VIEW

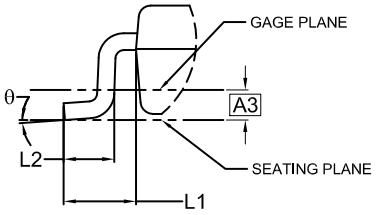


FRONT VIEW

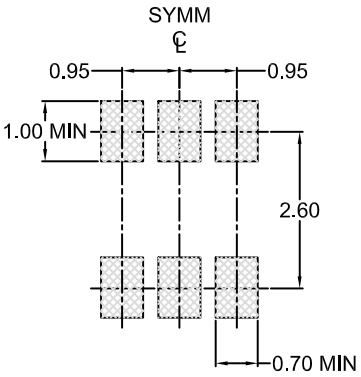
NOTE 4



SIDE VIEW



DETAIL A



LAND PATTERN
RECOMMENDATION

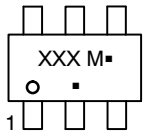
*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS OR GATE BURRS SHALL NOT EXCEED 0.25MM PER END. DIMENSIONS D AND E1 ARE DETERMINED AT DATUM H.
4. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	0.05	0.10
A2	0.70	0.85	1.00
A3		0.25 BSC	
b	0.25	0.38	0.50
c	0.10	0.18	0.26
D	2.80	2.95	3.10
d		0.30 REF	
E	2.50	2.75	3.00
E1	1.30	1.50	1.70
e		0.95 BSC	
e1		1.90 BSC	
L1		0.60 REF	
L2	0.20	0.40	0.60
θ	0°	---	10°

GENERIC MARKING DIAGRAM*



XXX = Specific Device Code
M = Date Code
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, "G" or microdot " ▪", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**TSOT23 6−Lead**	**PAGE 1 OF 1**

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