



Is Now Part of



ON Semiconductor®

To learn more about ON Semiconductor, please visit our website at
www.onsemi.com

Please note: As part of the Fairchild Semiconductor integration, some of the Fairchild orderable part numbers will need to change in order to meet ON Semiconductor's system requirements. Since the ON Semiconductor product management systems do not have the ability to manage part nomenclature that utilizes an underscore (_), the underscore (_) in the Fairchild part numbers will be changed to a dash (-). This document may contain device numbers with an underscore (_). Please check the ON Semiconductor website to verify the updated device numbers. The most current and up-to-date ordering information can be found at www.onsemi.com. Please email any questions regarding the system integration to Fairchild_questions@onsemi.com.

ON Semiconductor and the ON Semiconductor logo are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.



FDD8424H

Dual N & P-Channel PowerTrench[®] MOSFET N-Channel: 40V, 20A, 24mΩ P-Channel: -40V, -20A, 54mΩ

Features

Q1: N-Channel

- Max $r_{DS(on)}$ = 24mΩ at $V_{GS} = 10V$, $I_D = 9.0A$
- Max $r_{DS(on)}$ = 30mΩ at $V_{GS} = 4.5V$, $I_D = 7.0A$

Q2: P-Channel

- Max $r_{DS(on)}$ = 54mΩ at $V_{GS} = -10V$, $I_D = -6.5A$
- Max $r_{DS(on)}$ = 70mΩ at $V_{GS} = -4.5V$, $I_D = -5.6A$
- Fast switching speed
- RoHS Compliant

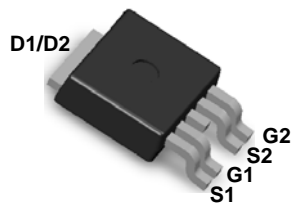


General Description

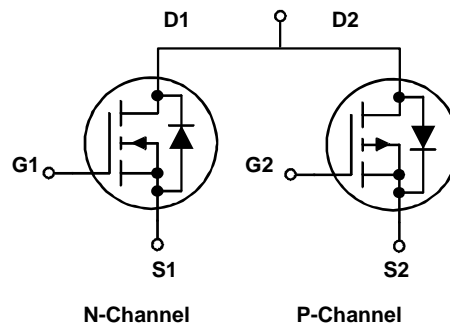
These dual N and P-Channel enhancement mode Power MOSFETs are produced using Fairchild Semiconductor's advanced PowerTrench- process that has been especially tailored to minimize on-state resistance and yet maintain superior switching performance.

Application

- Inverter
- H-Bridge



Dual DPAK 4L



MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Q1	Q2	Units
V_{DS}	Drain to Source Voltage	40	-40	V
V_{GS}	Gate to Source Voltage	± 20	± 20	V
I_D	Drain Current - Continuous (Package Limited)	20	-20	A
	- Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	26	-20	
	- Continuous $T_A = 25^\circ\text{C}$	9.0	-6.5	
	- Pulsed	55	-40	
P_D	Power Dissipation for Single Operation $T_C = 25^\circ\text{C}$ (Note 1)	30	35	W
	$T_A = 25^\circ\text{C}$ (Note 1a)	3.1		
	$T_A = 25^\circ\text{C}$ (Note 1b)	1.3		
E_{AS}	Single Pulse Avalanche Energy (Note 3)	29	33	mJ
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150		$^\circ\text{C}$

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q1 (Note 1)	4.1	$^\circ\text{C/W}$
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Single Operation for Q2 (Note 1)	3.5	

Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDD8424H	FDD8424H	TO-252-4L	13"	16mm	2500 units

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\mu\text{A}, V_{GS} = 0\text{V}$ $I_D = -250\mu\text{A}, V_{GS} = 0\text{V}$	Q1 Q2	40 -40			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		34 -32		mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 32\text{V}, V_{GS} = 0\text{V}$ $V_{DS} = -32\text{V}, V_{GS} = 0\text{V}$	Q1 Q2			1 -1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{V}, V_{DS} = 0\text{V}$	Q1 Q2			± 100 ± 100	nA nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\mu\text{A}$ $V_{GS} = V_{DS}, I_D = -250\mu\text{A}$	Q1 Q2	1 -1	1.7 -1.6	3 -3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\mu\text{A}$, referenced to 25°C $I_D = -250\mu\text{A}$, referenced to 25°C	Q1 Q2		-5.3 4.8		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{V}, I_D = 9.0\text{A}$ $V_{GS} = 4.5\text{V}, I_D = 7.0\text{A}$ $V_{GS} = 10\text{V}, I_D = 9.0\text{A}, T_J = 125^\circ\text{C}$	Q1		19 23 29	24 30 37	m Ω
		$V_{GS} = -10\text{V}, I_D = -6.5\text{A}$ $V_{GS} = -4.5\text{V}, I_D = -5.6\text{A}$ $V_{GS} = -10\text{V}, I_D = -6.5\text{A}, T_J = 125^\circ\text{C}$	Q2		42 58 62	54 70 80	
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{V}, I_D = 9.0\text{A}$ $V_{DS} = -5\text{V}, I_D = -6.5\text{A}$	Q1 Q2		29 13		S

Dynamic Characteristics

C_{iss}	Input Capacitance	Q1 $V_{DS} = 20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		750 1000	1000 1330	pF
C_{oss}	Output Capacitance	Q2	Q1 Q2		115 140	155 185	pF
C_{rss}	Reverse Transfer Capacitance	$V_{DS} = -20\text{V}, V_{GS} = 0\text{V}, f = 1\text{MHz}$	Q1 Q2		75 75	115 115	pF
R_g	Gate Resistance	$f = 1\text{MHz}$	Q1	0.1	1.1	3.3	Ω
			Q2	0.1	3.3	9.9	

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	Q1	Q1 Q2		7 7	14 14	ns
t_r	Rise Time	$V_{DD} = 20\text{V}, I_D = 9.0\text{A},$ $V_{GS} = 10\text{V}, R_{GEN} = 6\Omega$	Q1		13	24	ns
			Q2		3	10	
$t_{d(off)}$	Turn-Off Delay Time	Q2 $V_{DD} = -20\text{V}, I_D = -6.5\text{A},$ $V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	Q1		17	31	ns
			Q2		20	36	
t_f	Fall Time	$V_{GS} = -10\text{V}, R_{GEN} = 6\Omega$	Q1		6	12	ns
			Q2		3	10	
$Q_{g(TOT)}$	Total Gate Charge	Q1 $V_{GS} = 10\text{V}, V_{DD} = 20\text{V}, I_D = 9.0\text{A}$	Q1		14	20	nC
			Q2		17	24	
Q_{gs}	Gate to Source Charge	Q2	Q1		2.3		nC
			Q2		3.0		
Q_{gd}	Gate to Drain "Miller" Charge	$V_{GS} = -10\text{V}, V_{DD} = -20\text{V}, I_D = -6.5\text{A}$	Q1		3.2		nC
			Q2		3.6		

Electrical Characteristics $T_J = 25^\circ\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
--------	-----------	-----------------	------	-----	-----	-----	-------

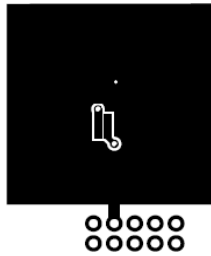
Drain-Source Diode Characteristics

I_S	Maximum Continuous Drain to Source Diode Forward Current		Q1 Q2			20 -20	A
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	(Note 2)	Q1 Q2			55 -40	A
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{V}, I_S = 9.0\text{A}$ (Note 2) $V_{GS} = 0\text{V}, I_S = -6.5\text{A}$ (Note 2)	Q1 Q2		0.87 0.88	1.2 -1.2	V
t_{rr}	Reverse Recovery Time	Q1 $I_F = 9.0\text{A}, di/dt = 100\text{A/s}$	Q1 Q2		25 29	38 44	ns
Q_{rr}	Reverse Recovery Charge	Q2 $I_F = -6.5\text{A}, di/dt = 100\text{A/s}$	Q1 Q2		19 29	29 44	nC

Notes:

1. $R_{\theta JA}$ is determined with the device mounted on a 1in^2 pad 2 oz copper pad on a $1.5 \times 1.5\text{in.}$ board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.

Q1



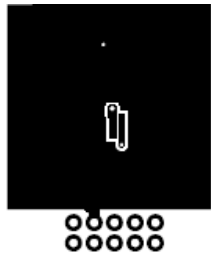
a. 40°C/W when mounted on a 1in^2 pad of 2 oz copper



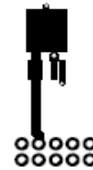
b. 96°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

Q2



a. 40°C/W when mounted on a 1in^2 pad of 2 oz copper



b. 96°C/W when mounted on a minimum pad of 2 oz copper

Scale 1 : 1 on letter size paper

2. Pulse Test: Pulse Width $< 300\mu\text{s}$, Duty cycle $< 2.0\%$.

3. Starting $T_J = 25^\circ\text{C}$, N-ch: $L = 0.3\text{mH}$, $I_{AS} = 14\text{A}$, $V_{DD} = 40\text{V}$, $V_{GS} = 10\text{V}$; P-ch: $L = 0.3\text{mH}$, $I_{AS} = -15\text{A}$, $V_{DD} = -40\text{V}$, $V_{GS} = -10\text{V}$.

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

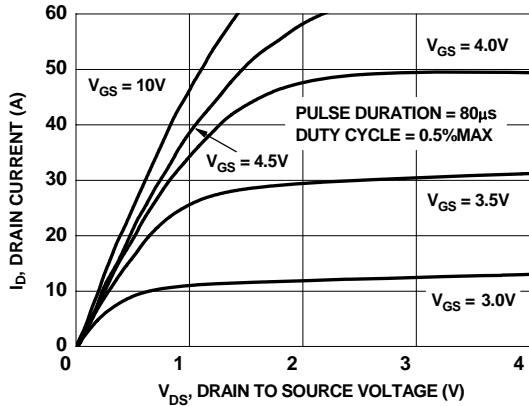


Figure 1. On-Region Characteristics

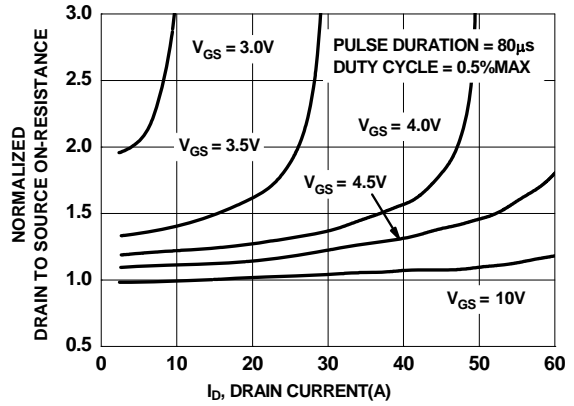


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

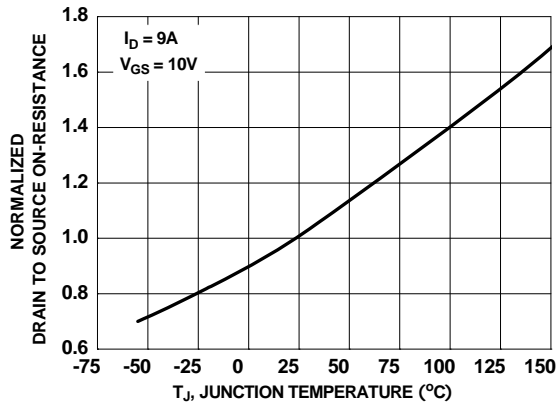


Figure 3. Normalized On-Resistance vs Junction Temperature

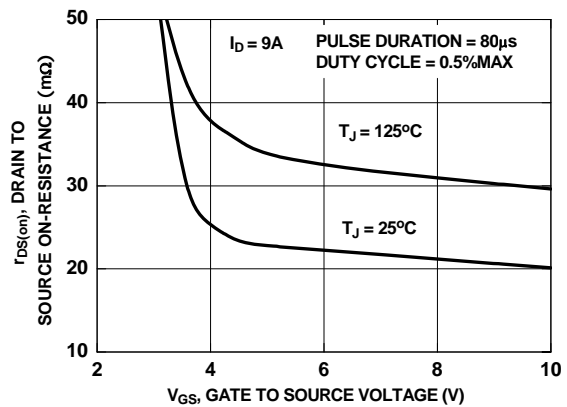


Figure 4. On-Resistance vs Gate to Source Voltage

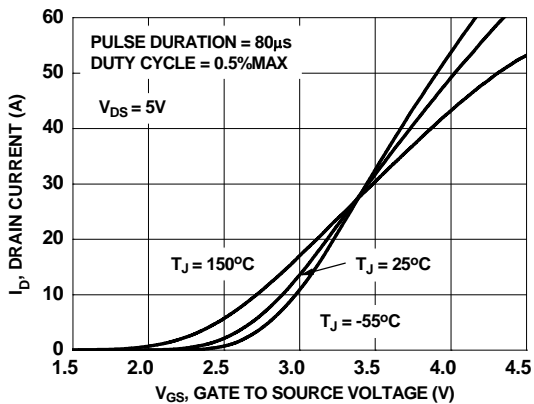


Figure 5. Transfer Characteristics

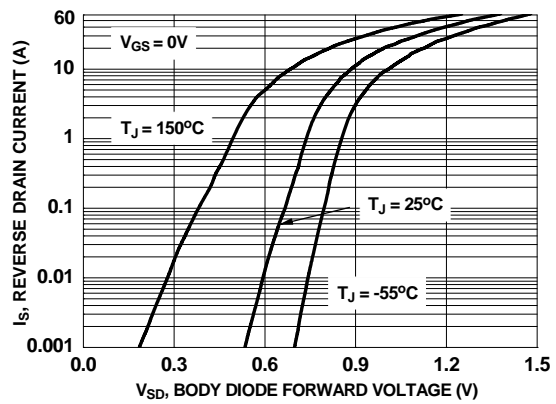


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

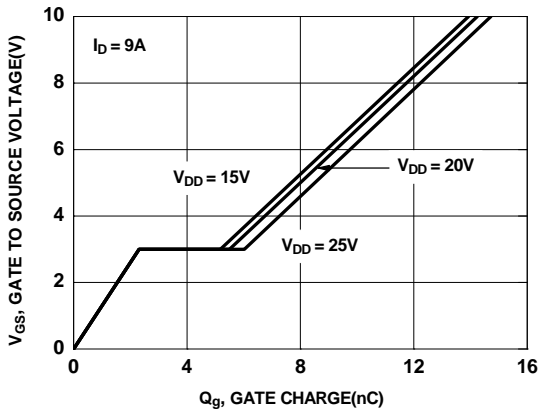


Figure 7. Gate Charge Characteristics

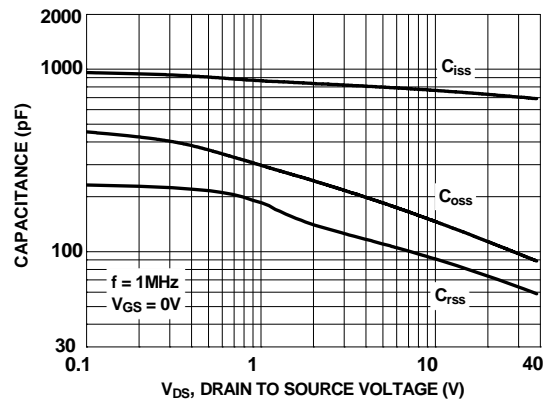


Figure 8. Capacitance vs Drain to Source Voltage

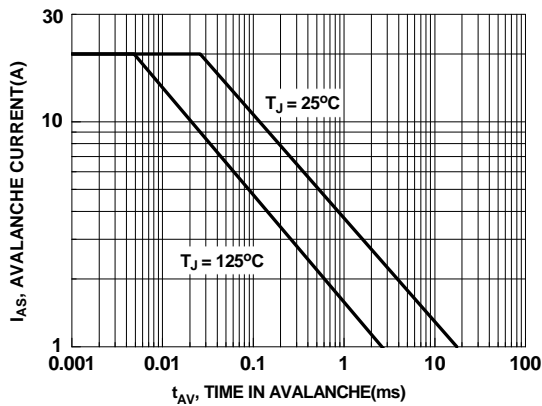


Figure 9. Unclamped Inductive Switching Capability

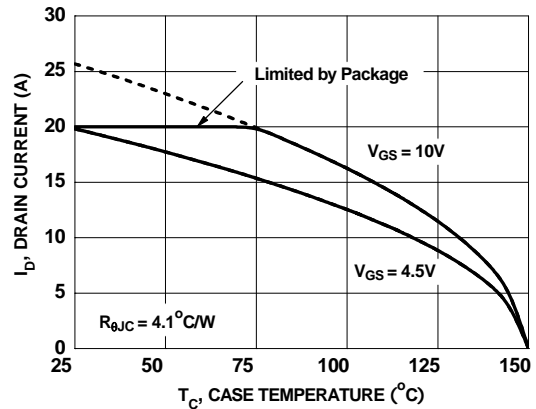


Figure 10. Maximum Continuous Drain Current vs Case Temperature

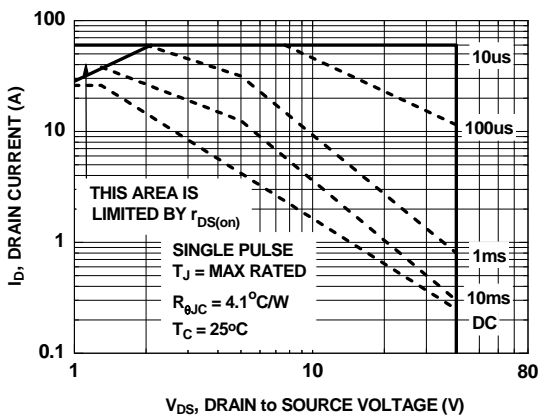


Figure 11. Forward Bias Safe Operating Area

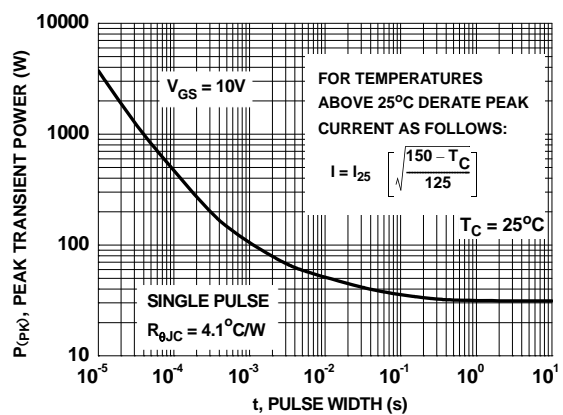


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q1 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

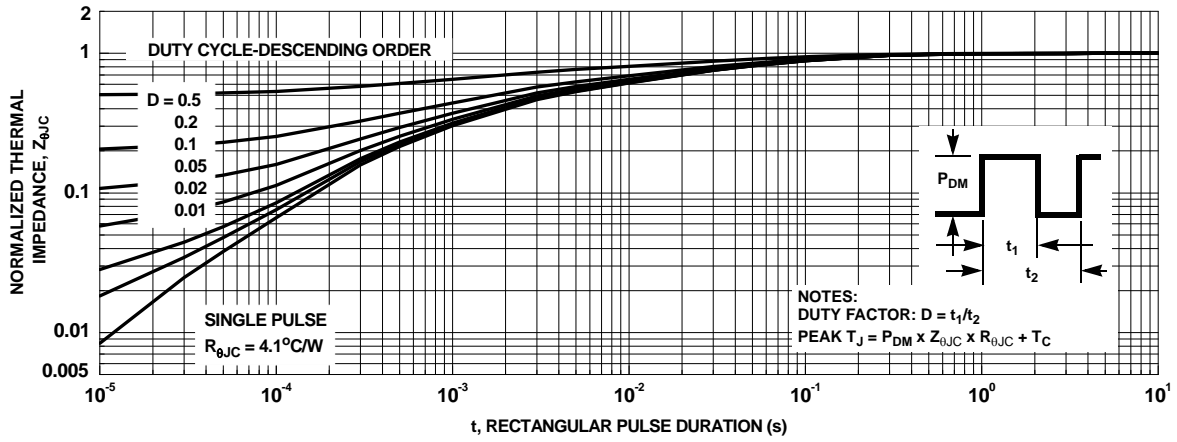


Figure 13. Transient Thermal Response Curve

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

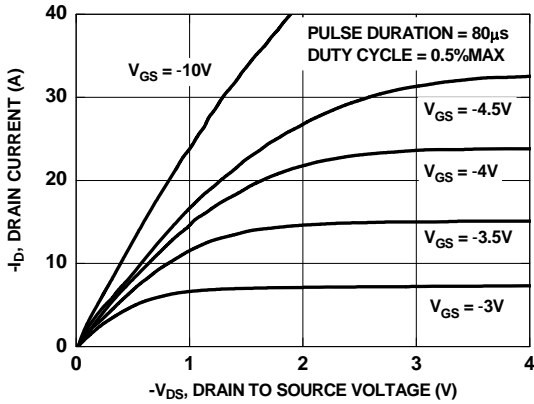


Figure 14. On-Region Characteristics

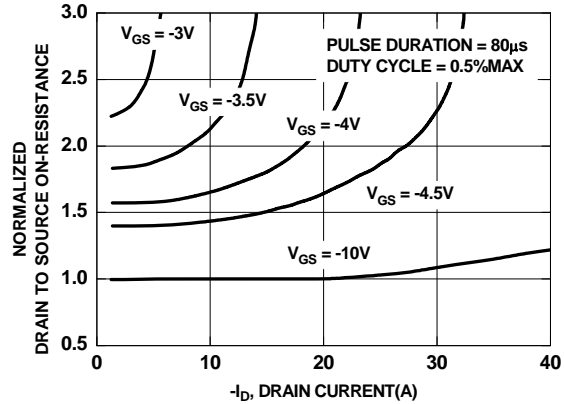


Figure 15. Normalized on-Resistance vs Drain Current and Gate Voltage

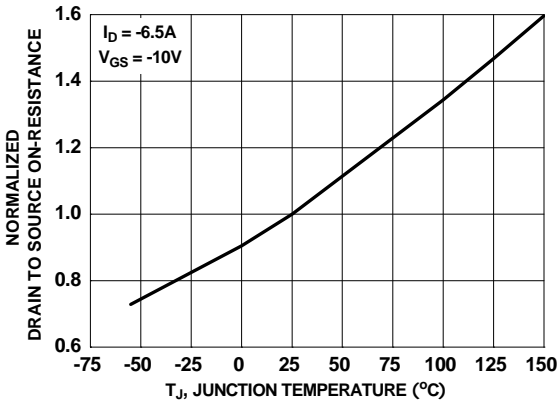


Figure 16. Normalized On-Resistance vs Junction Temperature

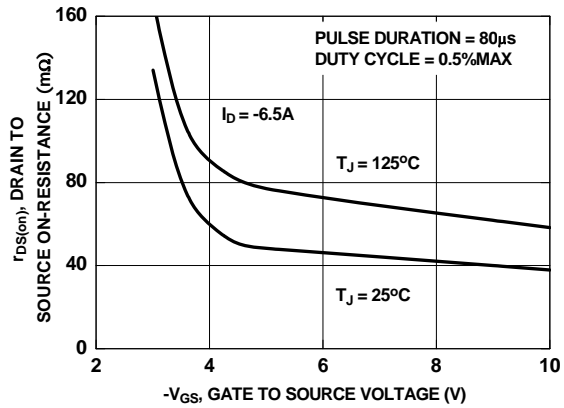


Figure 17. On-Resistance vs Gate to Source Voltage

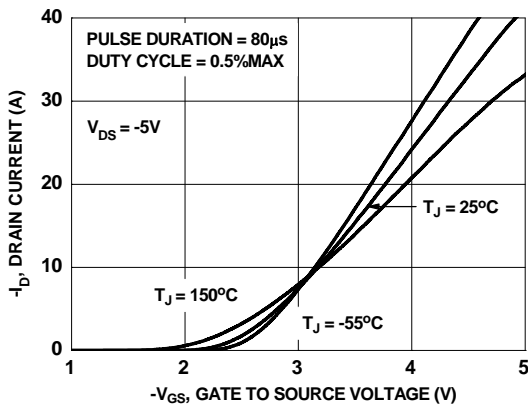


Figure 18. Transfer Characteristics

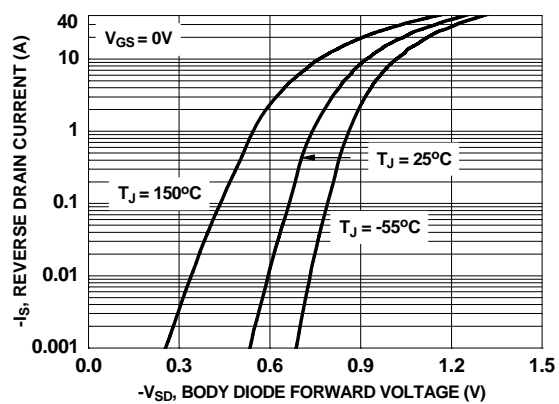


Figure 19. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

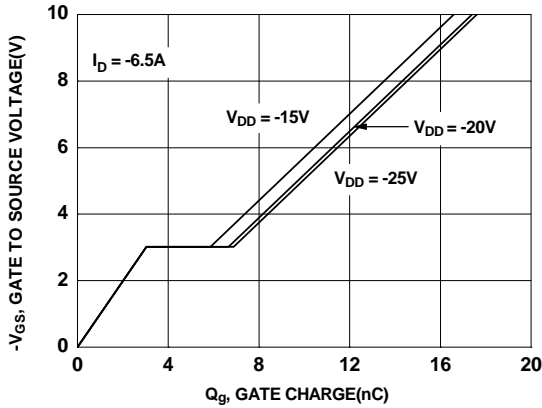


Figure 20. Gate Charge Characteristics

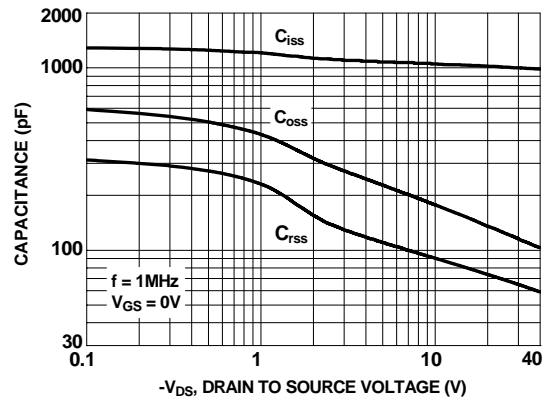


Figure 21. Capacitance vs Drain to Source Voltage

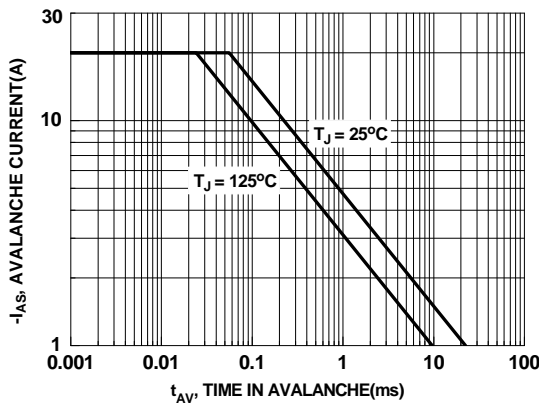


Figure 22. Unclamped Inductive Switching Capability

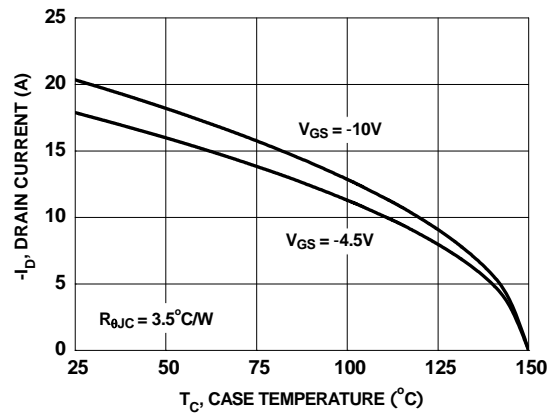


Figure 23. Maximum Continuous Drain Current vs Case Temperature

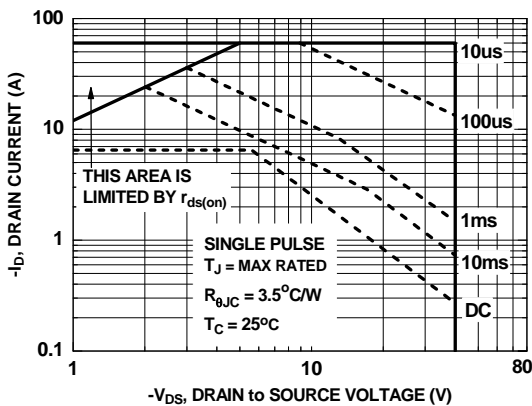


Figure 24. Forward Bias Safe Operating Area

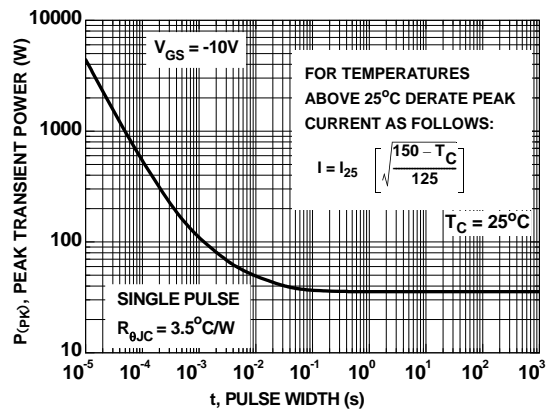
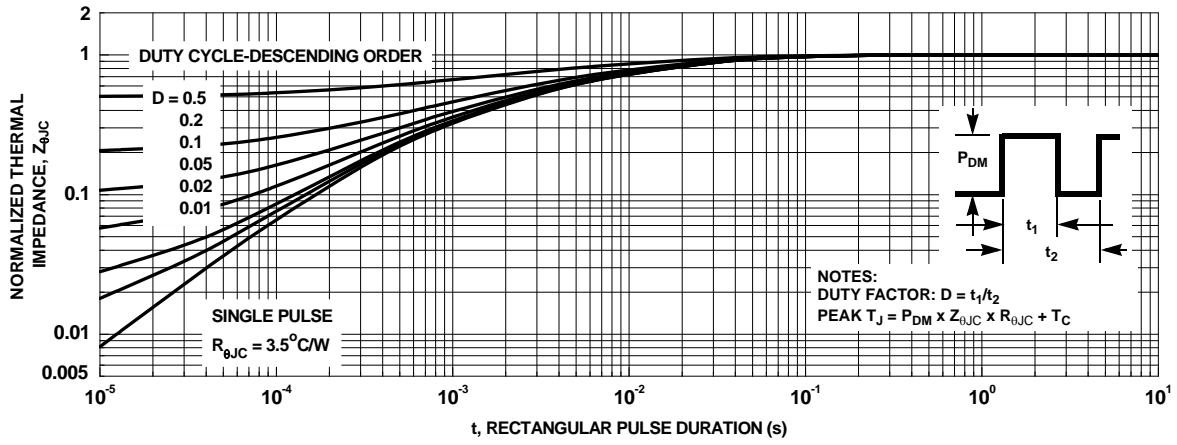
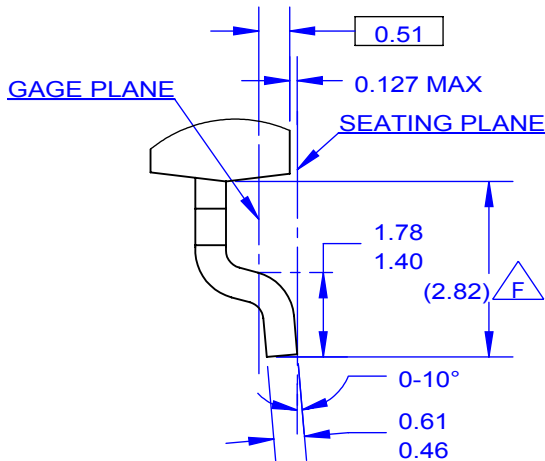
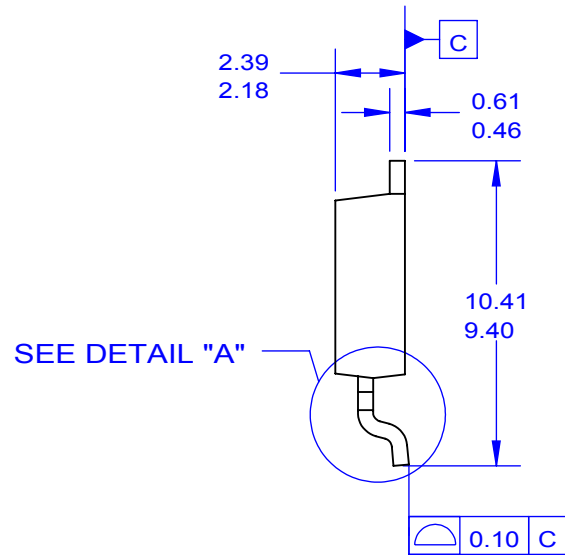
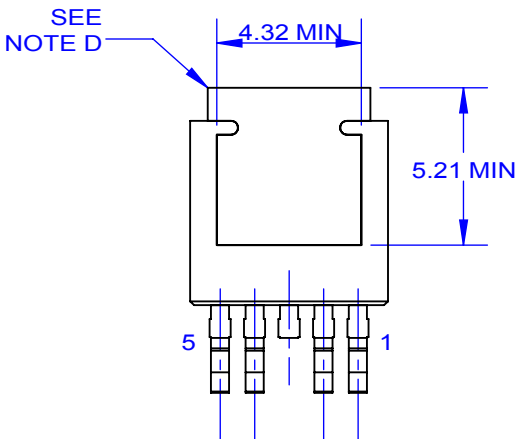
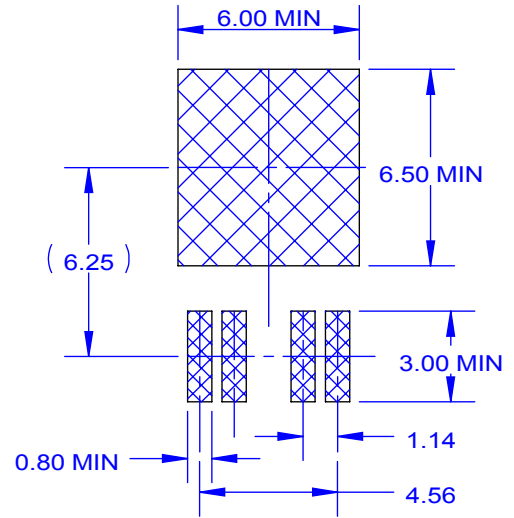
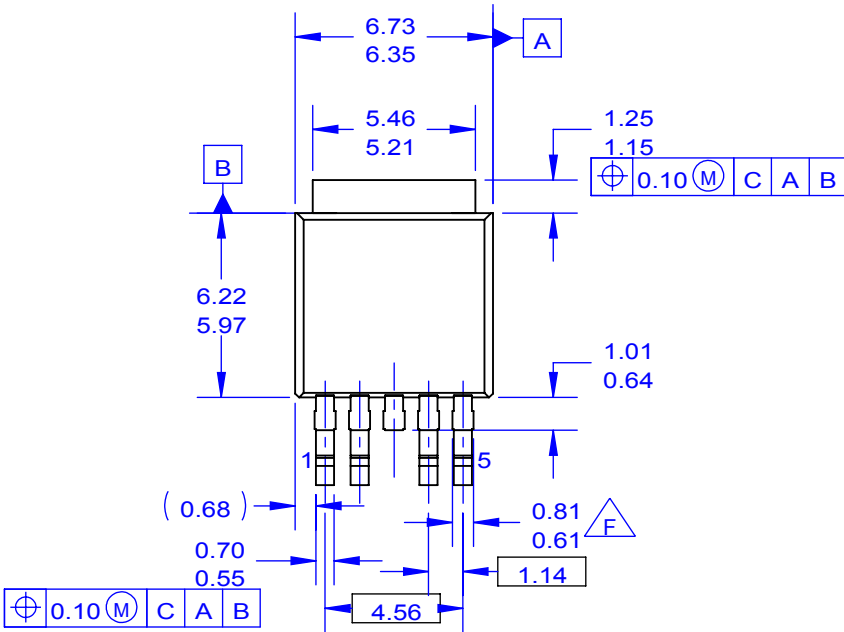


Figure 25. Single Pulse Maximum Power Dissipation

Typical Characteristics (Q2 P-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted





DETAIL A
SCALE 2:1

NOTES: UNLESS OTHERWISE SPECIFIED

- A. THIS PACKAGE CONFORMS TO JEDEC, TO252 VARIATION AD.
- B. ALL DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS
- D. HEATSINK TOP EDGE COULD BE IN CHAMFERED CORNERS OR EDGE PROTRUSION.
- E. DIMENSIONS AND TOLERANCES AS PER ASME Y14.5-2009.
- F. EXCEPTION TO TO-252 STANDARD.
- G. FILE NAME: TO252B05REV3
- H. FAIRCHILDSEMICONDUCTOR

ON Semiconductor and  are trademarks of Semiconductor Components Industries, LLC dba ON Semiconductor or its subsidiaries in the United States and/or other countries. ON Semiconductor owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of ON Semiconductor's product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. ON Semiconductor reserves the right to make changes without further notice to any products herein. ON Semiconductor makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does ON Semiconductor assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using ON Semiconductor products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by ON Semiconductor. "Typical" parameters which may be provided in ON Semiconductor data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. ON Semiconductor does not convey any license under its patent rights nor the rights of others. ON Semiconductor products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use ON Semiconductor products for any such unintended or unauthorized application, Buyer shall indemnify and hold ON Semiconductor and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that ON Semiconductor was negligent regarding the design or manufacture of the part. ON Semiconductor is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
19521 E. 32nd Pkwy, Aurora, Colorado 80011 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5817-1050

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>
For additional information, please contact your local
Sales Representative