

# MOSFET – N-Channel, POWERTRENCH®

100 V, 57 A, 16 mΩ

## FDI150N10

### Description

This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been tailored to minimize the on-state resistance while maintaining superior switching performance.

### Features

- $R_{DS(on)} = 12 \text{ m}\Omega$  (Typ.) @  $V_{GS} = 10 \text{ V}$ ,  $I_D = 49 \text{ A}$
- Fast Switching Speed
- Low Gate Charge
- High Performance Trench Technology for Extremely Low  $R_{DS(on)}$
- High Power and Current Handling Capability
- RoHS Compliant

### Applications

- Synchronous Rectification for ATX / Server / Telecom PSU
- Battery Protection Circuit
- Motor Drives and Uninterruptible Power Supplies
- Micor Solar Inverter

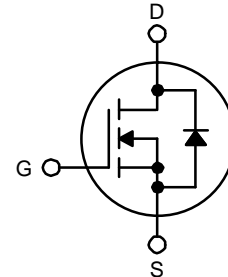
### MOSFET MAXIMUM RATINGS ( $T_C = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	FDI150N10	Unit
$V_{DSS}$	Drain to Source Voltage	100	V
$V_{GSS}$	Gate to Source Voltage	$\pm 20$	V
$I_D$	Drain Current	– Continuous ( $T_C = 25^\circ\text{C}$ )	57
		– Continuous ( $T_C = 100^\circ\text{C}$ )	40
$I_{DM}$	Drain Current	– Pulsed (Note 1)	228
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	132	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	7.5	V/ns
$P_D$	Power Dissipation	( $T_C = 25^\circ\text{C}$ )	110
		– Derate Above $25^\circ\text{C}$	0.88
$T_J, T_{STG}$	Operating and Storage Temperature Range	$-55$ to $+150$	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds	300	$^\circ\text{C}$

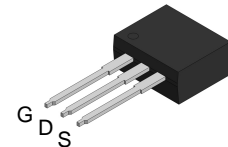
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Repetitive rating: pulse-width limited by maximum junction temperature.
2.  $L = 0.11 \text{ mH}$ ,  $I_{AS} = 49 \text{ A}$ ,  $V_{DD} = 50 \text{ V}$ ,  $R_G = 25 \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 49 \text{ A}$ ,  $di/dt \leq 200 \text{ A}/\mu\text{s}$ ,  $V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .

$V_{DSS}$	$R_{DS(on)} \text{ MAX}$	$I_D \text{ MAX}$
100 V	16 mΩ @ 10 V	57 A

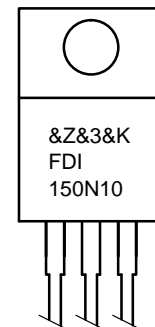


P-Channel MOSFET



I2PAK  
CASE 418AV

### MARKING DIAGRAM



- &Z = Assembly Plant Code
- &3 = 3-Digit Plant Code
- &K = 2-Digits Lot Run Traceability Code
- FDI150N10 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping
FDI150N10	I2PAK	800 Units / Tube

# FDI150N10

## THERMAL CHARACTERISTICS

Symbol	Parameter	FDI150N10	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	1.13	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient, Max.	62.5	

## ELECTRICAL CHARACTERISTICS ( $T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$ , $V_{GS} = 0 \text{ V}$ , $T_C = 25^\circ\text{C}$	100	–	–	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$ , Referenced to $25^\circ\text{C}$	–	0.1	–	V/°C
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$	–	–	1	$\mu\text{A}$
		$V_{DS} = 100 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $T_C = 150^\circ\text{C}$	–	–	500	
$I_{GSS}$	Gate to Body Leakage Current	$V_{GS} = \pm 20 \text{ V}$ , $V_{DS} = 0 \text{ V}$	–	–	$\pm 100$	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250 \mu\text{A}$	2.5	–	4.5	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$ , $I_D = 49 \text{ A}$	–	12	16	m $\Omega$
$g_{FS}$	Forward Transconductance	$V_{DS} = 20 \text{ V}$ , $I_D = 49 \text{ A}$	–	156	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 25 \text{ V}$ , $V_{GS} = 0 \text{ V}$ , $f = 1 \text{ MHz}$	–	3580	4760	pF
$C_{oss}$	Output Capacitance		–	340	450	pF
$C_{rss}$	Reverse Transfer Capacitance		–	140	210	pF

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}$ , $I_D = 49 \text{ A}$ , $V_{GS} = 10 \text{ V}$ , $R_G = 25 \Omega$ (Note 4)	–	47	104	ns
$t_r$	Turn-On Rise Time		–	164	338	ns
$t_{d(off)}$	Turn-Off Delay Time		–	86	182	ns
$t_f$	Turn-Off Fall Time		–	83	176	ns
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{DS} = 80 \text{ V}$ , $I_D = 49 \text{ A}$ , $V_{GS} = 10 \text{ V}$ (Note 4)	–	53	69	nC
$Q_{gs}$	Gate to Source Gate Charge		–	19	–	nC
$Q_{gd}$	Gate to Drain "Miller" Charge		–	15	–	nC

### DRAIN-SOURCE DIODE CHARACTERISTICS

$I_S$	Maximum Continuous Drain to Source Diode Forward Current		–	–	57	A
$I_{SM}$	Maximum Pulsed Drain to Source Diode Forward Current		–	–	228	A
$V_{SD}$	Drain to Source Diode Forward Voltage	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 49 \text{ A}$	–	–	1.3	V
$t_{rr}$	Reverse Recovery Time	$V_{GS} = 0 \text{ V}$ , $I_{SD} = 49 \text{ A}$ , $di_F/dt = 100 \text{ A}/\mu\text{s}$	–	41	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	70	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

4. Essentially independent of operating temperature typical characteristics.

## TYPICAL PERFORMANCE CHARACTERISTICS

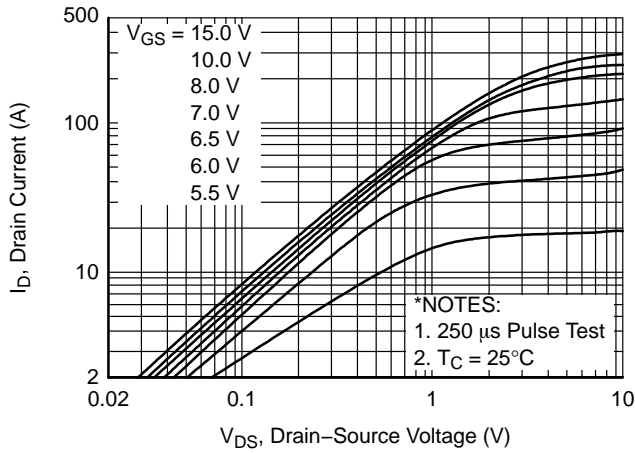


Figure 1. On-Region Characteristics

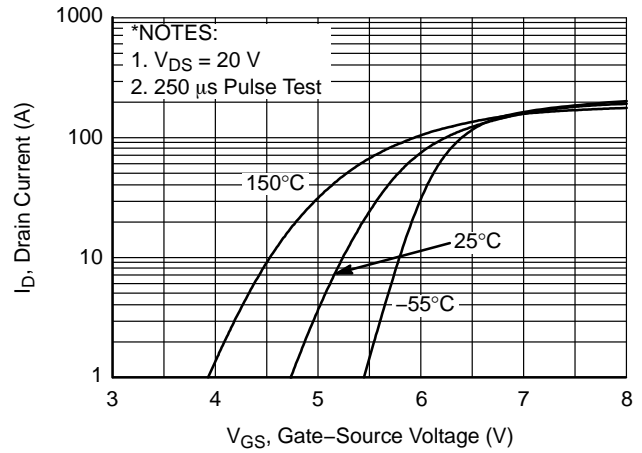


Figure 2. Transfer Characteristics

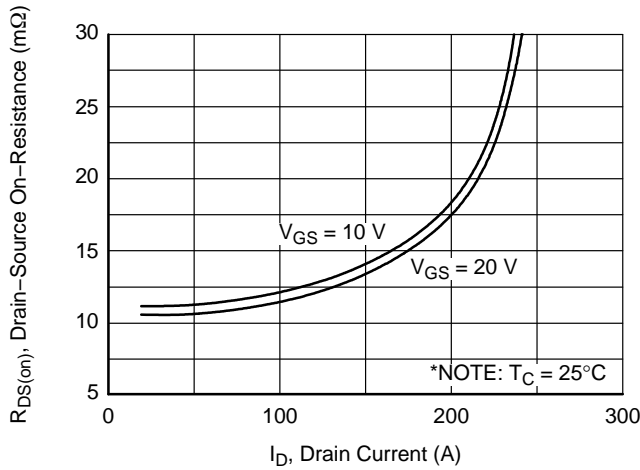


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

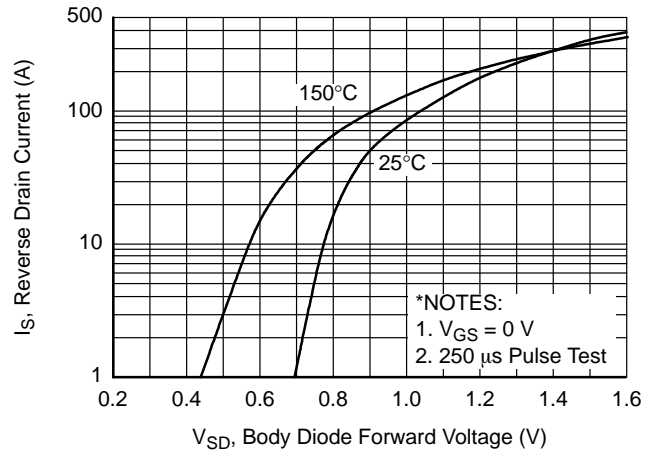


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

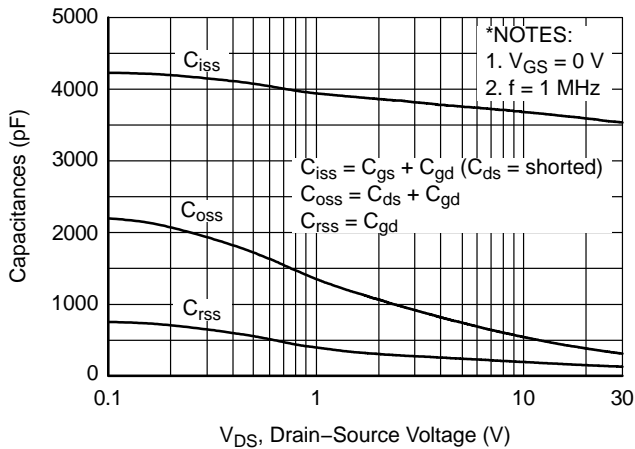


Figure 5. Capacitance Characteristics

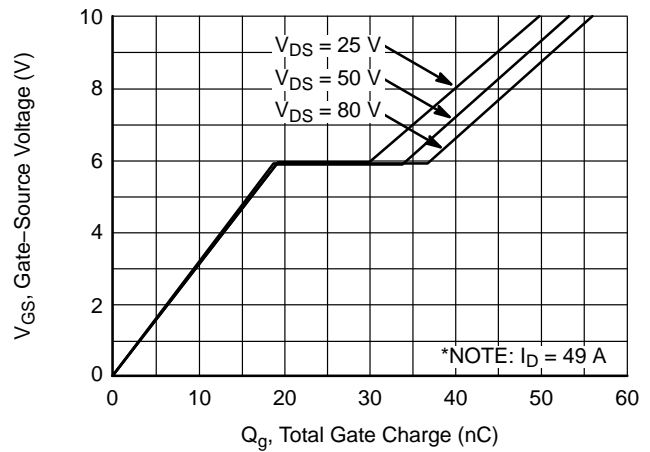


Figure 6. Gate Charge Characteristics

## TYPICAL PERFORMANCE CHARACTERISTICS (CONTINUED)

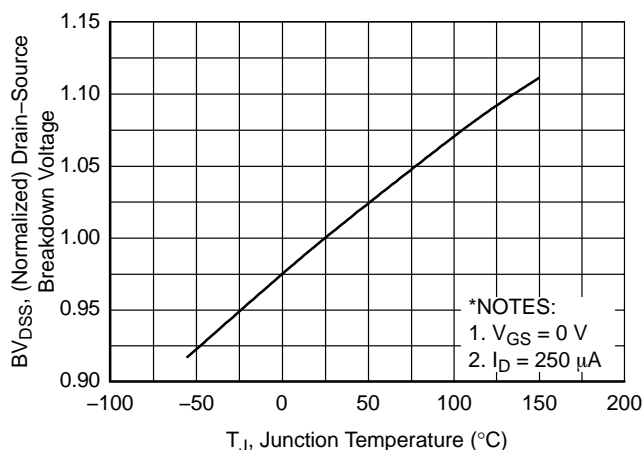


Figure 7. Breakdown Voltage Variation vs. Temperature

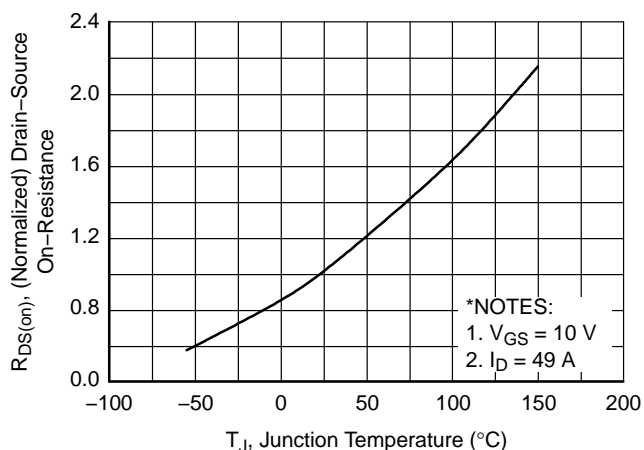


Figure 8. On-Resistance Variation vs. Temperature

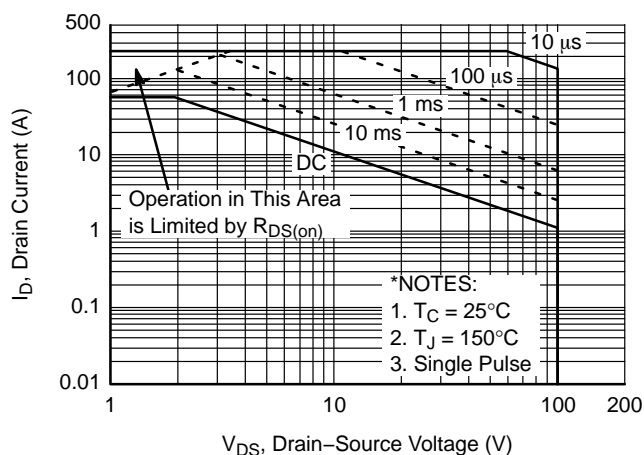


Figure 9. Maximum Safe Operating Area

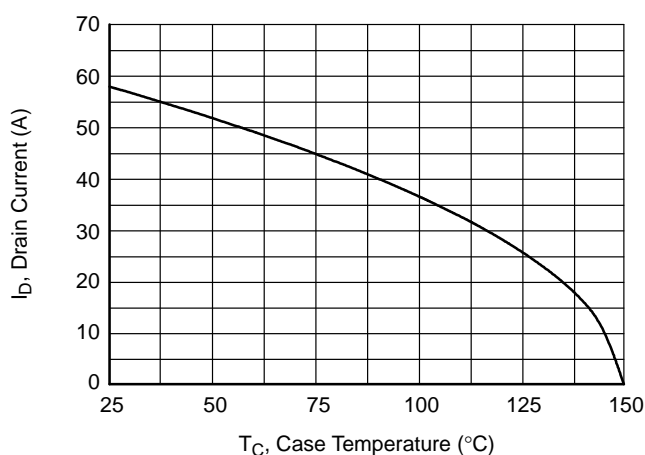


Figure 10. Maximum Drain Current vs. Case Temperature

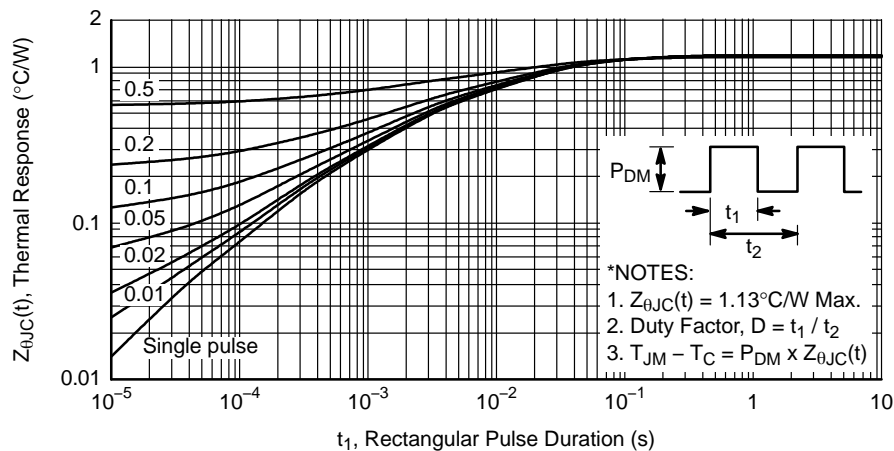


Figure 11. Transient Thermal Response Curve

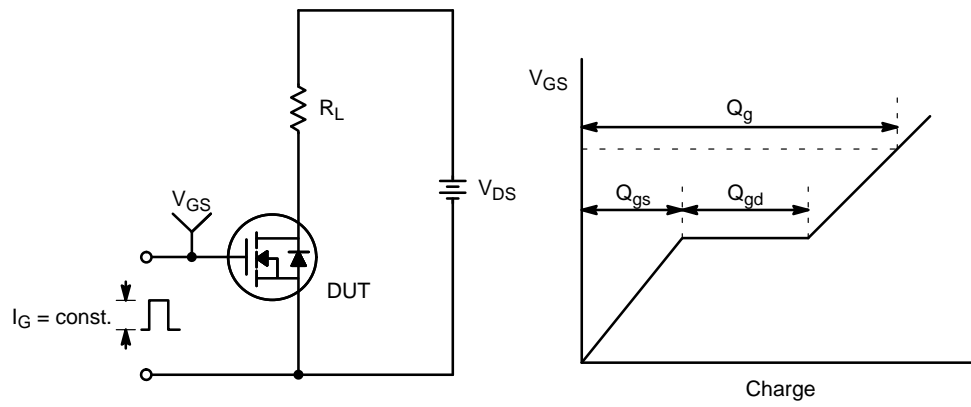


Figure 12. Gate Charge Test Circuit & Waveform

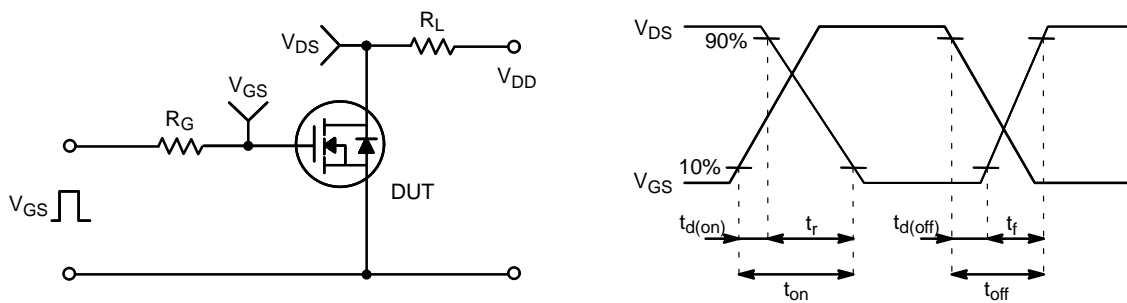


Figure 13. Resistive Switching Test Circuit & Waveforms

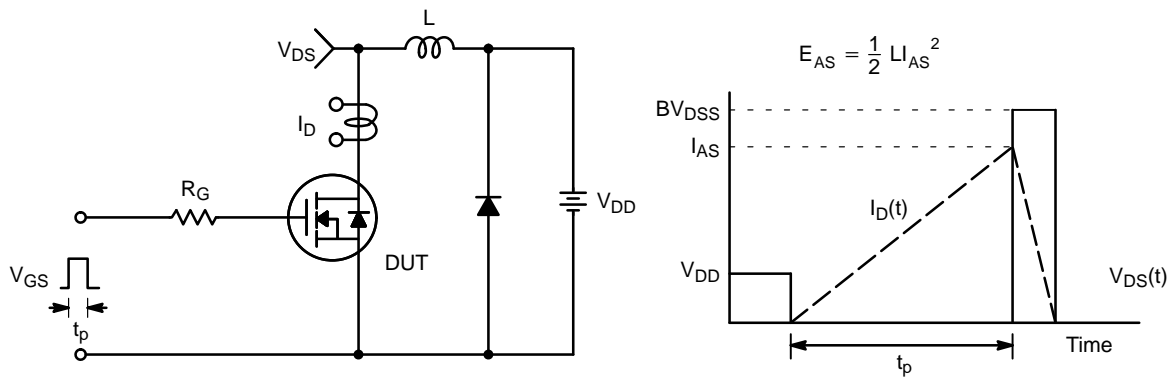
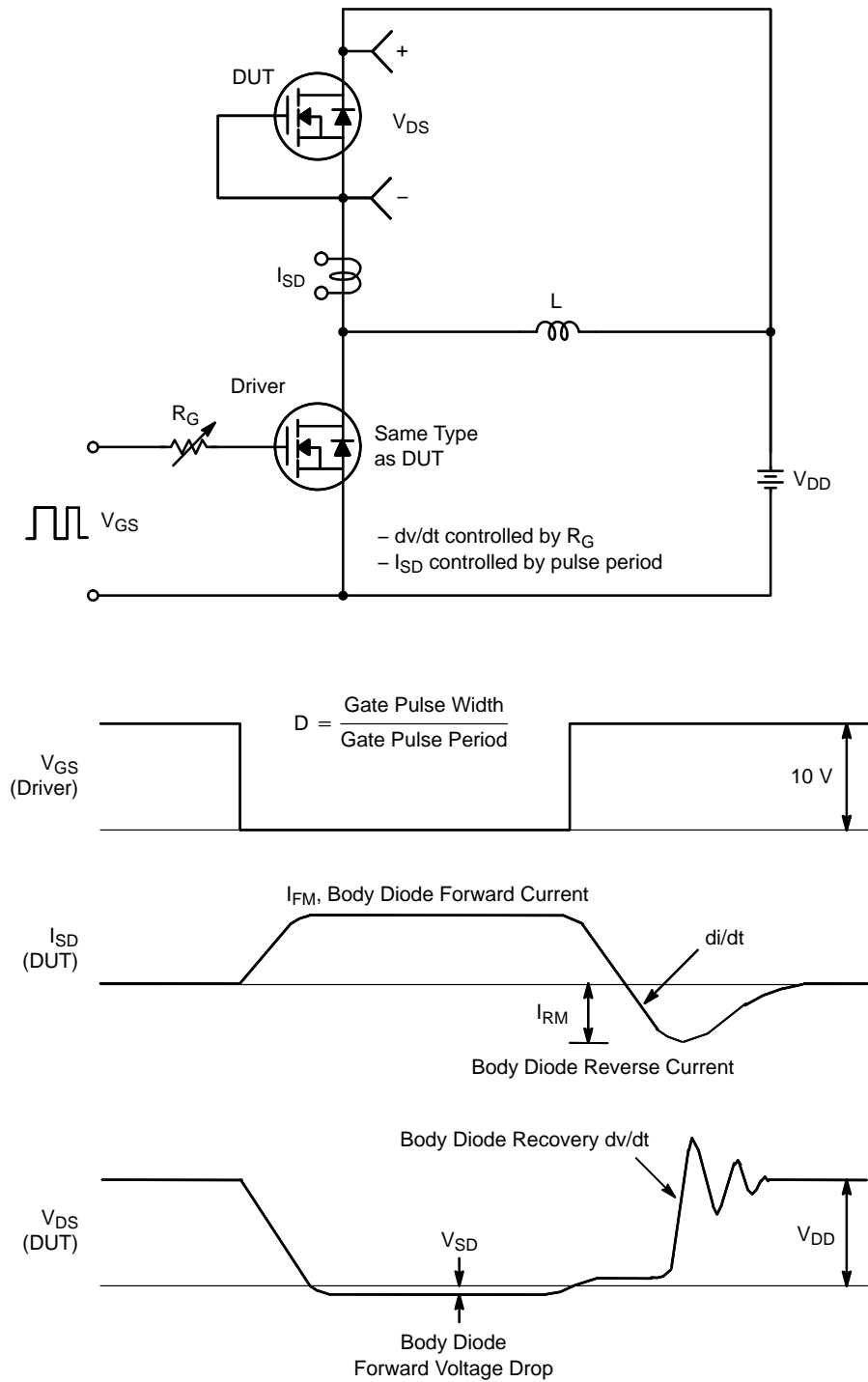
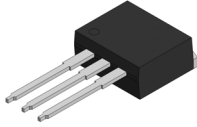


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

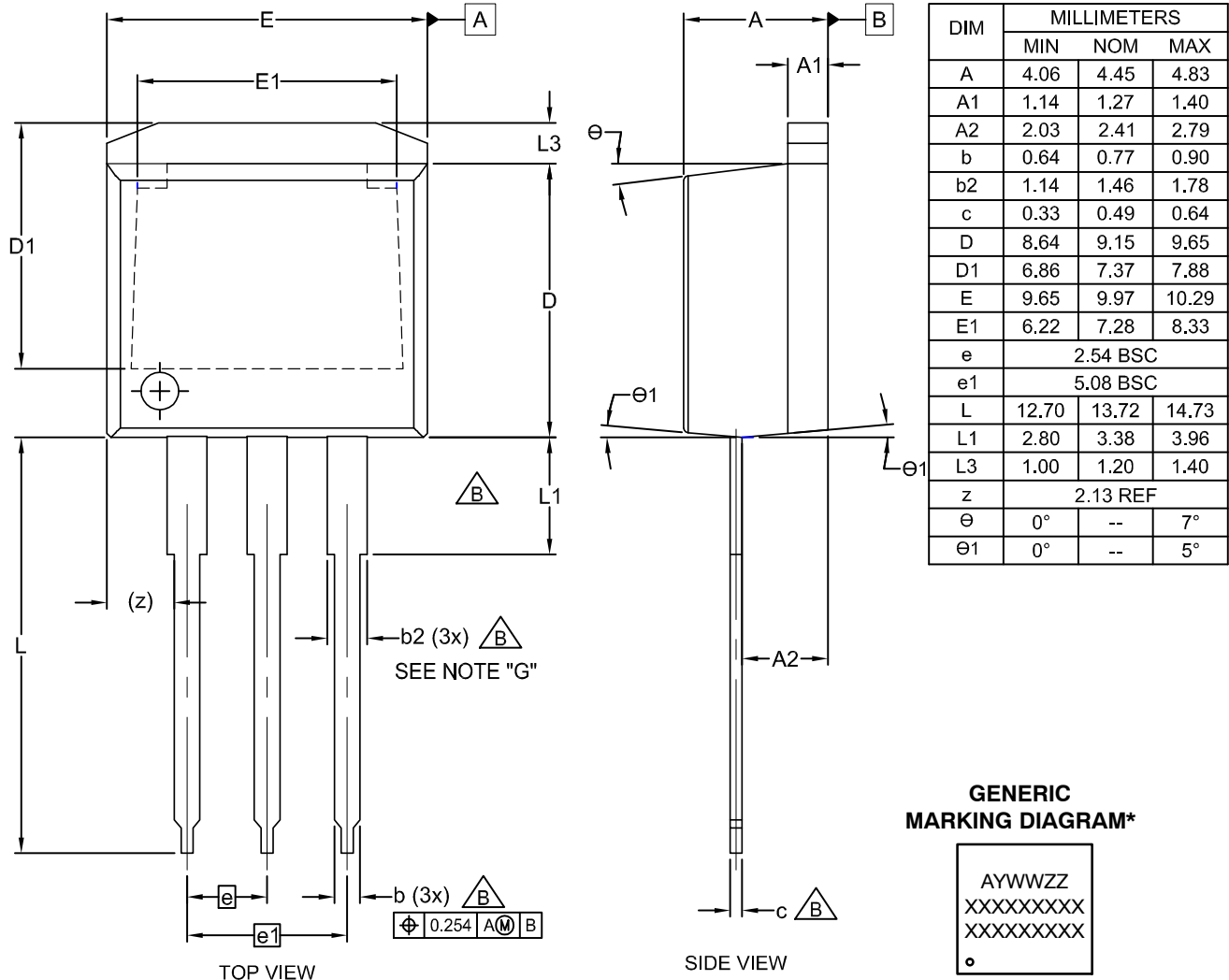
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**Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms**


**I2PAK (TO-262 3 LD)**  
CASE 418AV  
ISSUE A

DATE 30 AUG 2022



## NOTES:

- A. EXCEPT WHERE NOTED CONFORMS TO T262 JEDEC VARIATION AA.  
B. DOES NOT COMPLY JEDEC STD. VALUE.  
C. ALL DIMENSIONS ARE IN MILLIMETERS.  
D. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH AND TIE BAR PROTRUSIONS.  
E. DIMENSION AND TOLERANCE AS PER ANSI Y14.5-1994.  
F. LOCATION OF PIN HOLE MAY VARY (LOWER LEFT CORNER, LOWER CENTER AND CENTER OF PACKAGE)  
G. MAXIMUM WIDTH FOR F102 DEVICE = 1.35 MAX.

XXXX = Specific Device Code  
A = Assembly Location  
Y = Year  
WW = Work Week  
ZZ = Assembly Lot Code

\*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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