

MOSFET – Single P-Channel, POWERTRENCH[®], 1.8 V Specified

FDMA291P

General Description

This device is designed specifically for battery charge or load switching in cellular handset and other ultraportable applications. It features a MOSFET with low on-state resistance. The MicroFET™ 2x2 package offers exceptional thermal performance for its physical size and is well suited to linear mode applications.

Features

- -6.6 A, -20 V
 - ♦ $R_{DS(ON)} = 42\text{ m}\Omega @ V_{GS} = -4.5\text{ V}$
 - ♦ $R_{DS(ON)} = 58\text{ m}\Omega @ V_{GS} = -2.5\text{ V}$
 - ♦ $R_{DS(ON)} = 98\text{ m}\Omega @ V_{GS} = -1.8\text{ V}$
- Low Profile – 0.8 mm Maximum – in the New Package MicroFET 2x2 mm
- Free from Halogenated Compounds and Antimony Oxides
- This Device is Pb-Free, Halide Free and RoHS Compliant RoHS Compliant

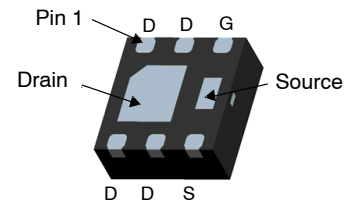
ABSOLUTE MAXIMUM RATINGS (T_A = 25°C unless otherwise noted.)

Symbol	Parameter	Value	Unit
V _{DS}	Drain-Source Voltage	-20	V
V _{GS}	Gate-Source Voltage	±8	V
I _D	Drain Current – Continuous (Note 1a) – Pulsed	-6.6 24	A
P _D	Power Dissipation for Single Operation (Note 1a) (Note 1b)	2.4 0.9	W
T _J , T _{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

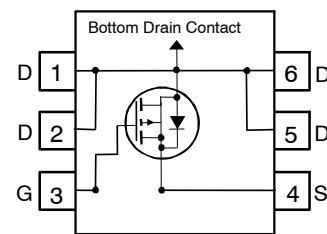
Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

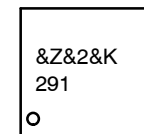
Symbol	Parameter	Value	Unit
R _{θJC}	Thermal Resistance, Junction-to-Case	13	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1a)	52	°C/W
R _{θJA}	Thermal Resistance, Junction-to-Ambient (Note 1b)	145	°C/W



WDFN6 (MicroFET 2 x 2)
CASE 511CZ



MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2 Digit Date Code (YW)
- &K = 2 Digit Lot Traceability Code
- 291 = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMA291P	WDFN6 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

FDMA291P

ELECTRICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$ unless otherwise noted.)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain–Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = -250\ \mu\text{A}$	-20	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	-	-12	-	mV/ $^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = -16\text{ V}, V_{GS} = 0\text{ V}$	-	-	-1	μA
I_{GSS}	Gate–Body Leakage	$V_{GS} = \pm 8\text{ V}, V_{DS} = 0\text{ V}$	-	-	± 100	nA

ON CHARACTERISTICS (Note 2)

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = -250\ \mu\text{A}$	-0.4	-0.7	-1.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate Threshold Voltage Temperature Coefficient	$I_D = -250\ \mu\text{A}$, Referenced to 25°C	-	3	-	mV/ $^\circ\text{C}$
$R_{DS(on)}$	Static Drain–Source On–Resistance	$V_{GS} = -4.5\text{ V}, I_D = -6.6\text{ A}$ $V_{GS} = -2.5\text{ V}, I_D = -5.1\text{ A}$ $V_{GS} = -1.8\text{ V}, I_D = -3.9\text{ A}$ $V_{GS} = -4.5\text{ V}, I_D = -6.6\text{ A}, T_J = 125^\circ\text{C}$	-	36 51 79 49	42 58 98 64	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = -5\text{ V}, I_D = -6.6\text{ A}$	-	16	-	S

DYNAMIC CHARACTERISTICS

C_{ISS}	Input Capacitance	$V_{DS} = -10\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	-	1000	-	pF
C_{OSS}	Output Capacitance		-	190	-	pF
C_{RSS}	Reverse Transfer Capacitance		-	100	-	pF

SWITCHING CHARACTERISTICS (Note 2)

$t_{d(on)}$	Turn–On Delay Time	$V_{DD} = -10\text{ V}, I_D = -1\text{ A},$ $V_{GS} = -4.5\text{ V}, R_{GEN} = 6\ \Omega$	-	13	23	ns
t_r	Turn–On Rise Time		-	9	18	ns
$t_{d(off)}$	Turn–Off Delay Time		-	42	68	ns
t_f	Turn–Off Fall Time		-	25	40	ns
Q_g	Total Gate Charge	$V_{DS} = -10\text{ V}, I_D = -6.6\text{ A}, V_{GS} = -4.5\text{ V}$	-	10	14	nC
Q_{gs}	Gate–Source Charge		-	2	-	nC
Q_{gd}	Gate–Drain Charge		-	3	-	nC

DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain–Source Diode Forward Current	-	-	-2	A	
V_{SD}	Drain–Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = -2\text{ A}$ (Note 2)	-	-0.8	-1.2	V
t_{rr}	Reverse Recovery Time	$I_F = -6.6\text{ A}$ $d_{IF}/dt = 100\text{ A}/\mu\text{s}$	-	20	-	ns
Q_{rr}	Reverse Recovery Charge		-	8	-	nC

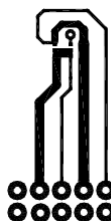
Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

NOTES:

- $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta JA}$ is determined by the user's board design.



a. 52 $^\circ\text{C}/\text{W}$ when mounted on a 1 in² pad of 2 oz copper



b. 145 $^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width $\leq 300\ \mu\text{s}$, Duty Cycle $\leq 2.0\%$.

TYPICAL CHARACTERISTICS

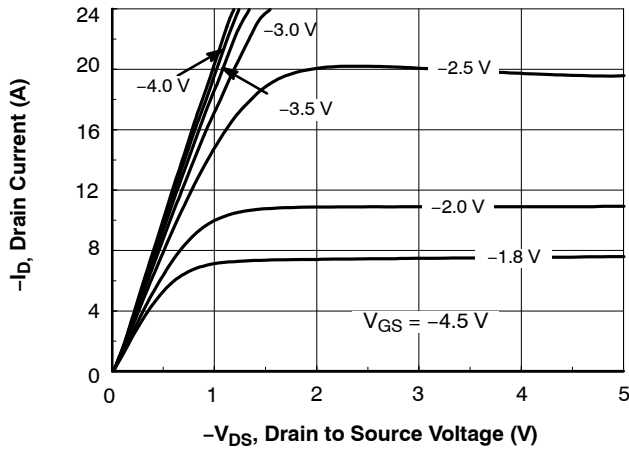


Figure 1. On-Region Characteristics

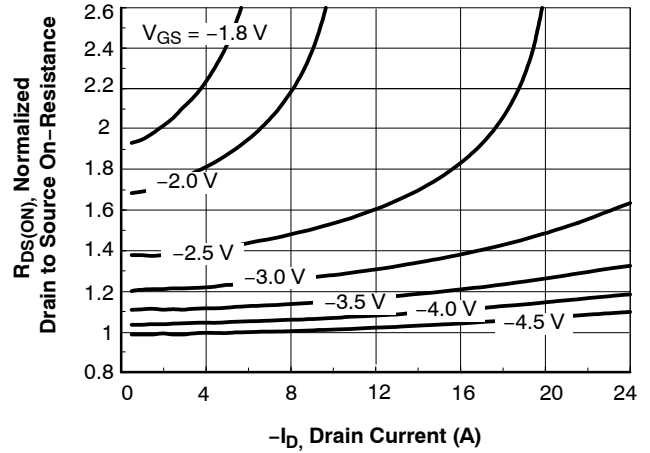


Figure 2. On-Resistance Variation with Drain Current and Gate Voltage

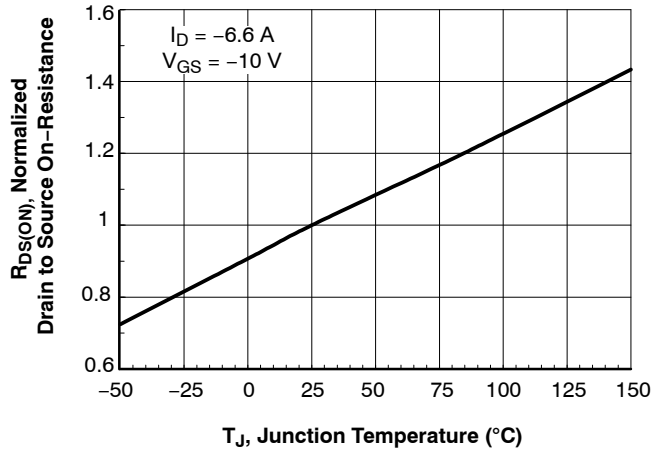


Figure 3. On-Resistance Variation with Temperature.

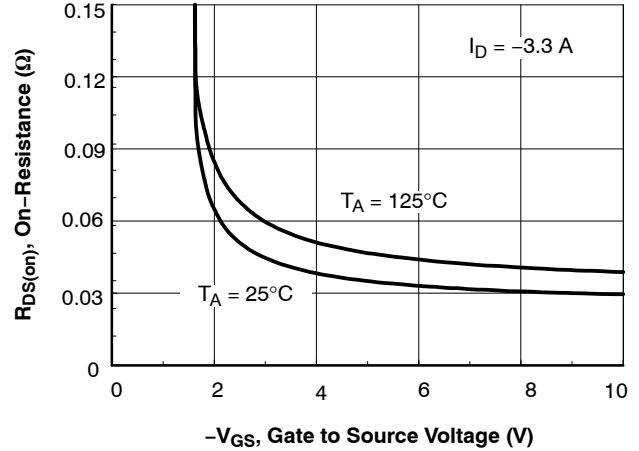


Figure 4. On-Resistance Variation with Gate-to-Source Voltage

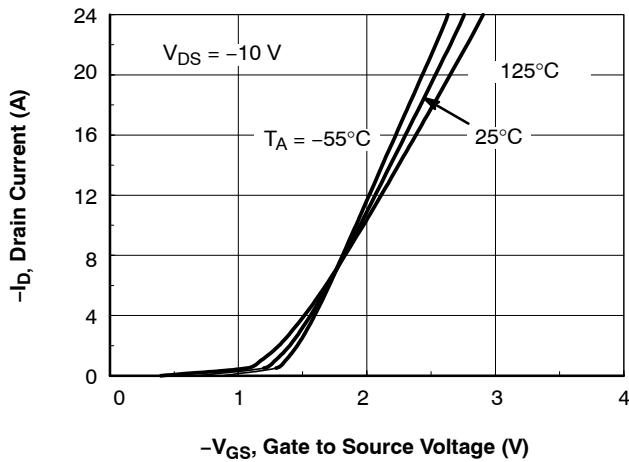


Figure 5. Transfer Characteristics

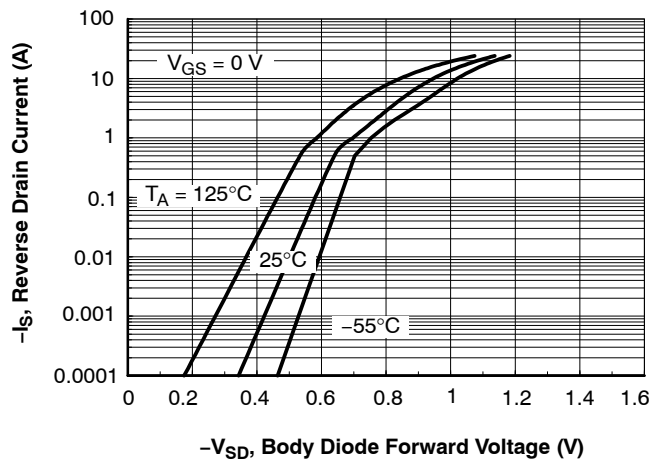


Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature

TYPICAL CHARACTERISTICS (Continue)

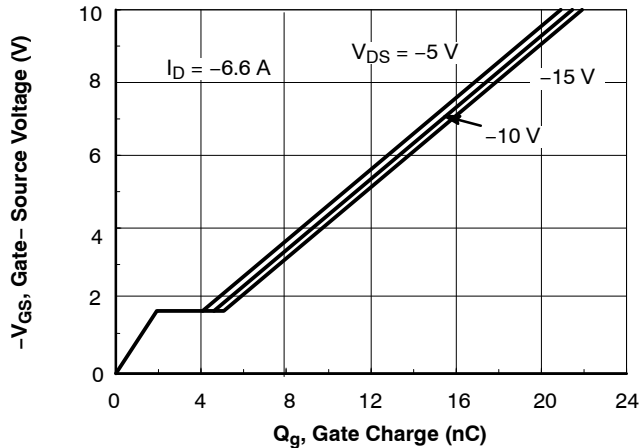


Figure 7. Gate Charge Characteristics

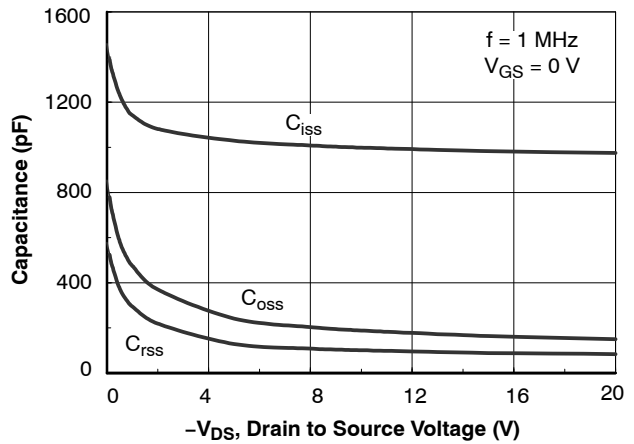


Figure 8. Capacitance Characteristics

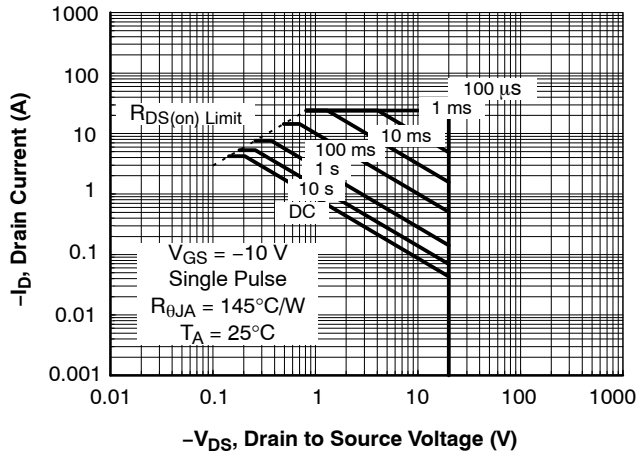


Figure 9. Maximum Safe Operating Area

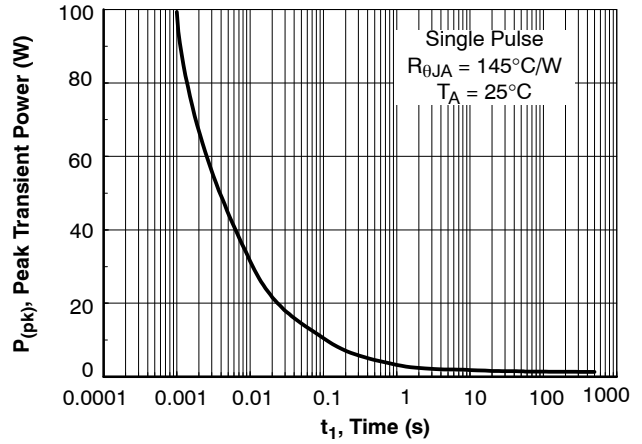


Figure 10. Single Pulse Maximum Power Dissipation

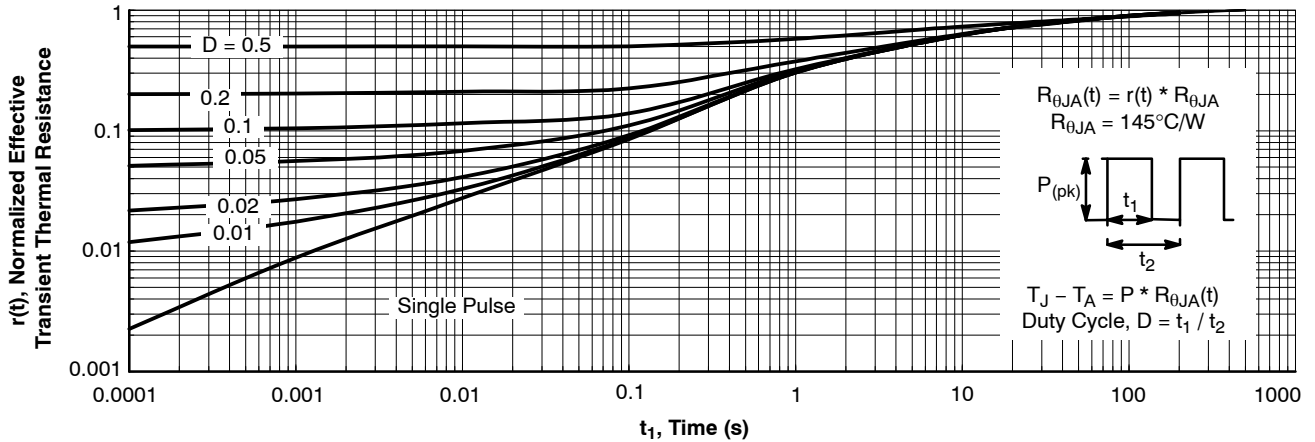


Figure 11. Transient Thermal Response Curve

Thermal characterization performed using the conditions described in Note1b.
 Transient thermal response will change depending on the circuit board design.

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MECHANICAL CASE OUTLINE

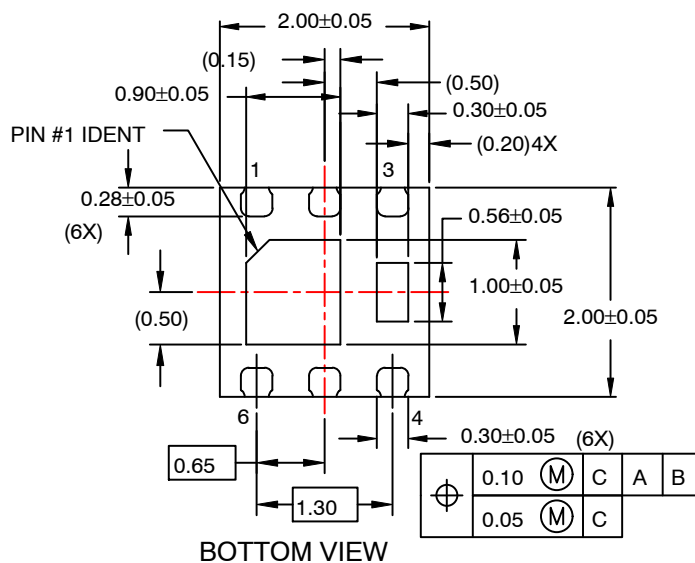
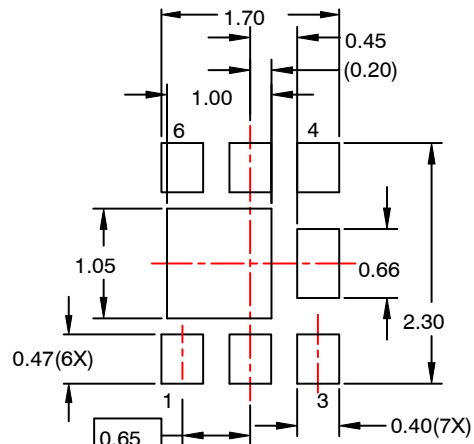
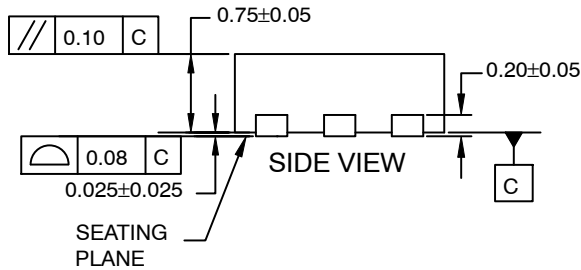
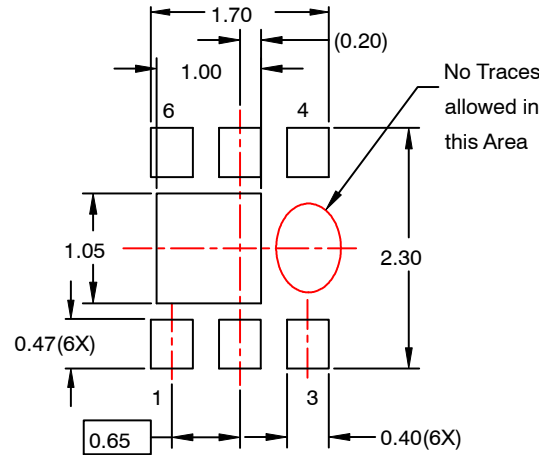
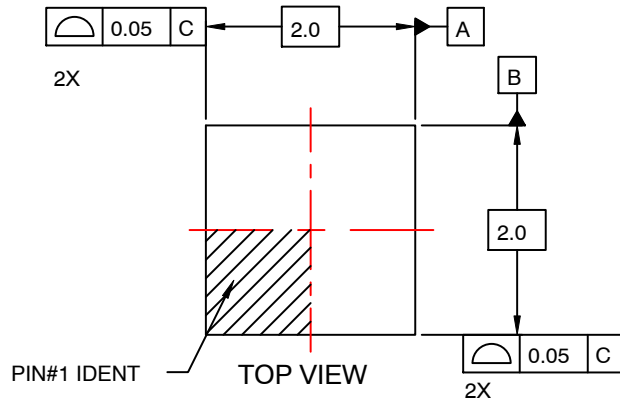
PACKAGE DIMENSIONS

ON Semiconductor®



WDFN6 2x2, 0.65P
CASE 511CZ
ISSUE O

DATE 31 JUL 2016



NOTES:

- A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC MO-229 REGISTRATION
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.

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