MOSFET – P-Channel, POWERTRENCH®

-30 V, -18 A, 20 mΩ

FDMC4435BZ, FDMC4435BZ-F127, FDMC4435BZ-F127-L701

General Description

This P−Channel MOSFET is produced using **onsemi**'s advanced POWERTRENCH process that has been especially tailored to minimize the on−state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

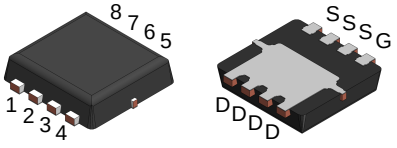
Features

- Max $r_{DS(on)}$ = 20 mΩ at V_{GS} = −10 V, I_D = −8.5 A
- Max $r_{DS(on)}$ = 37 mΩ at V_{GS} = −4.5 V, I_D = −6.3 A
- Extended V_{GSS} Range (−25 V) for Battery Applications
- High Performance Trench Technology for Extremely Low $r_{DS(on)}$
- High Power and Current Handling Capability
- HBM ESD Protection Level > 7 kV Typical*
- 100% UIL Tested
- These Devices are Pb−Free and are RoHS Compliant

Applications

- High Side in DC − DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook

*The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.



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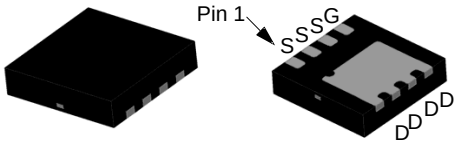
WDFN8 3.3x3.3, 0.65P
CASE 511DR
FMDC4435BZ/FDMC4435BZ−F127



Top Bottom

WDFN8 3.3x3.3, 0.65P
CASE 511DQ
(Option A)
FDMC4435BZ−F127−L701

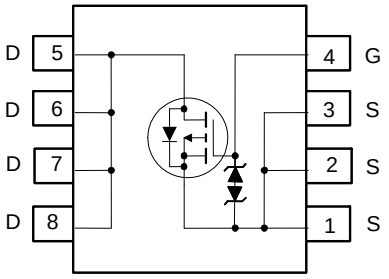
MARKING DIAGRAM

FDMC4435BZ/
FDMC4435BZ−F127

FDMC4435BZ−F127−L701

FDMC4435BZ = Specific Device Code
A = Assembly Location
XY = 2−Digit Date Code
KK = 2−Digit Lot Run Traceability Code
L = Wafer Lot Number
YW = Assembly Start Week

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

NOTE: Some of the devices on this data sheet have been **DISCONTINUED**. Please refer to the table on page 6.

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MOSFET MAXIMUM RATINGS (T_A = 25°C unless otherwise noted)

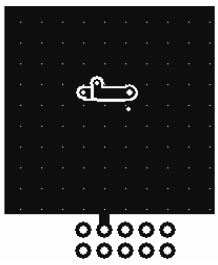
Symbol	Parameter			Rating	Unit
V_{DS}	Drain to Source Voltage			−30	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current	Continuous	T_C = 25°C	−18	A
		Continuous (Note 1a)	T_A = 25°C	−8.5	
		Pulsed		−50	
E_{AS}	Single Pulse Avalanche Energy (Note 2)			32	mJ
P_D	Power Dissipation		T_C = 25°C	31	W
	Power Dissipation (Note 1a)		T_A = 25°C	2.3	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			−55 to + 150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

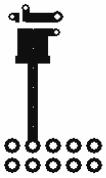
THERMAL CHARACTERISTICS

Symbol	Parameter	Rating	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	53	

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR−4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 53°C/W when mounted on a 1 in^2 pad of 2 oz copper



b. 125°C/W when mounted on a minimum pad of 2 oz copper

2. Starting T_J = 25°C; P−ch: L = 1 mH, I_{AS} = −8 A, V_{DD} = −27 V, V_{GS} = −10 V.

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ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = −250 μA, V_{GS} = 0 V	−30			V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C		21		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = −24 V, V_{GS} = 0 V			−1	μA
		V_{DS} = −24 V, V_{GS} = 0 V, T_J = 125°C			−100	
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±10	μA
ON CHARACTERISTICS						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = −250 μA	−1.0	−1.8	−3.0	V
$\Delta V_{GS(th)}$ / ΔT_J	Gate to Source Threshold Voltage Temperature Coefficient	I_D = −250 μA, referenced to 25°C		−5		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = −10 V, I_D = −8.5 A		14	20	mΩ
		V_{GS} = −4.5 V, I_D = −6.3 A		21	37	
		V_{GS} = −10 V, I_D = −8.5 A, T_J = 125°C		20	29	
g_{FS}	Forward Transconductance	V_{DD} = −5 V, I_D = −8.5 A		25		S
DYNAMIC CHARACTERISTICS						
C_{iss}	Input Capacitance	V_{DS} = −15 V, V_{GS} = 0 V, f = 1 MHz		1535	2040	pF
C_{oss}	Output Capacitance			310	410	pF
C_{rss}	Reverse Transfer Capacitance			280	420	pF
R_g	Gate Resistance	f = 1 MHz		4		Ω
SWITCHING CHARACTERISTICS						
$t_{d(on)}$	Turn−On Delay Time	V_{DD} = −15 V, I_D = −8.5 A, V_{GS} = −10 V, R_{GEN} = 6 Ω		10	20	ns
t_r	Rise Time			9	18	ns
$t_{d(off)}$	Turn−Off Delay Time			35	56	ns
t_f	Fall Time			19	34	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to −10 V, V_{DD} = −15 V, I_D = −8.5 A		38	53	nC
		V_{GS} = 0 V to −4.5 V, V_{DD} = −15 V, I_D = −8.5 A		20	28	nC
Q_{gs}	Gate to Source Charge	V_{DD} = −15 V, I_D = −8.5 A		4.3		nC
Q_{gd}	Gate to Drain “Miller” Charge			11		nC
DRAIN−SOURCE DIODE CHARACTERISTICS						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = −8.5 A (Note 3)		0.86	1.5	V
		V_{GS} = 0 V, I_S = −1.9 A (Note 3)		0.74	1.2	
t_{rr}	Reverse Recovery Time	I_F = −8.5 A, di/dt = 100 A/μs		26	40	ns
Q_{rr}	Reverse Recovery Charge			12	20	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

3. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

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TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED)

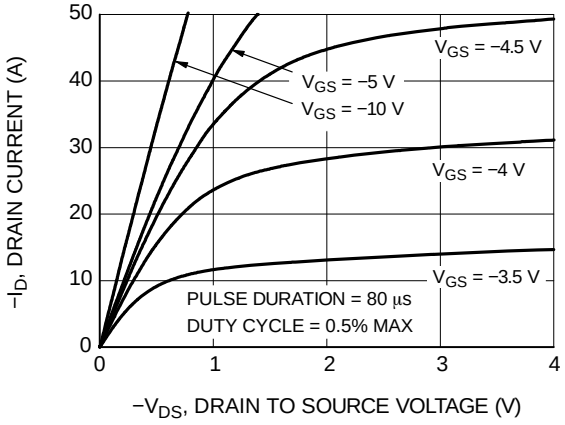

Figure 1. On Region Characteristics

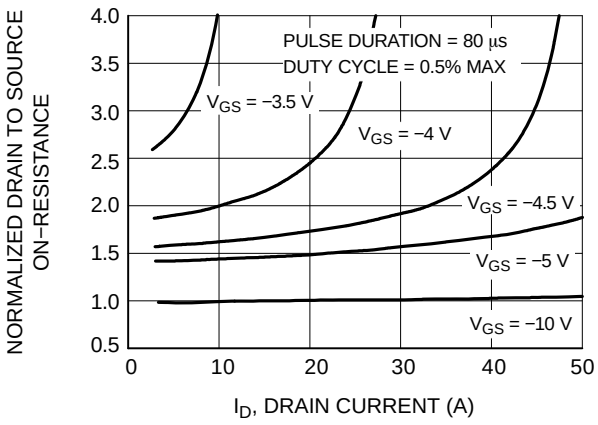

Figure 2. Normalized On−Resistance vs. Drain Current and Gate Voltage

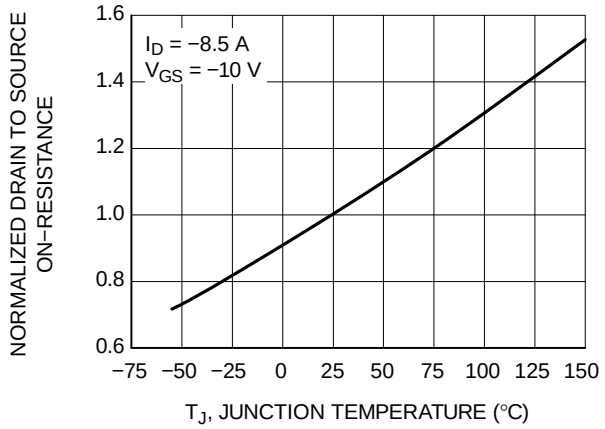

Figure 3. Normalized On Resistance vs. Junction Temperature

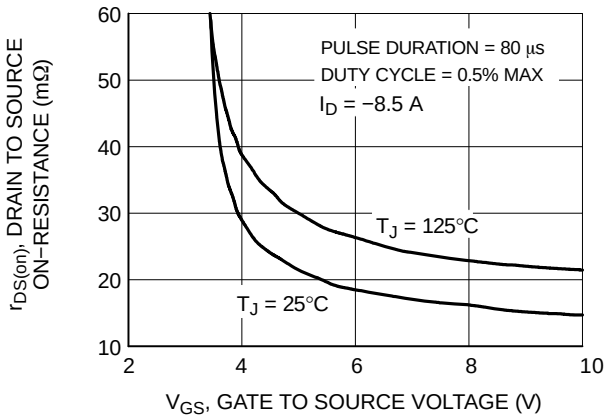

Figure 4. On−Resistance vs. Gate to Source Voltage

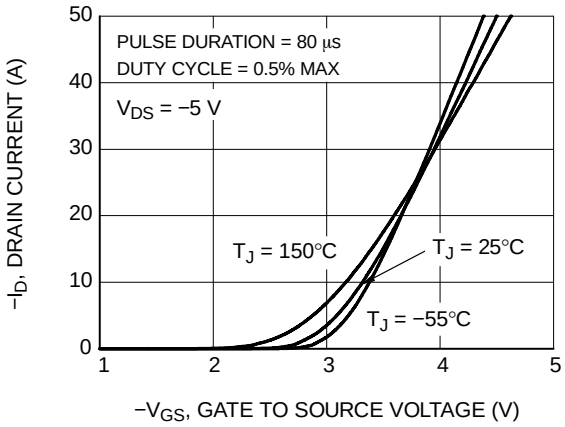

Figure 5. Transfer Characteristics

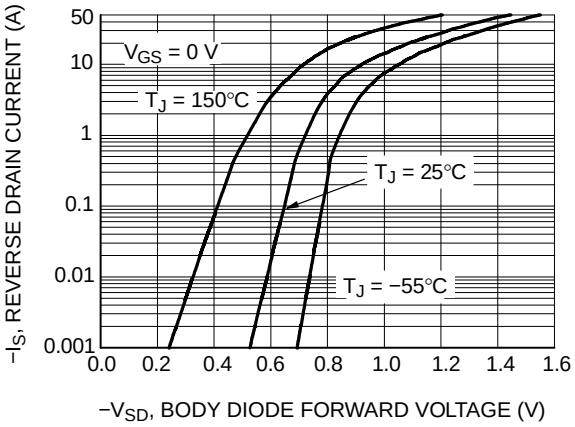

Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

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TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

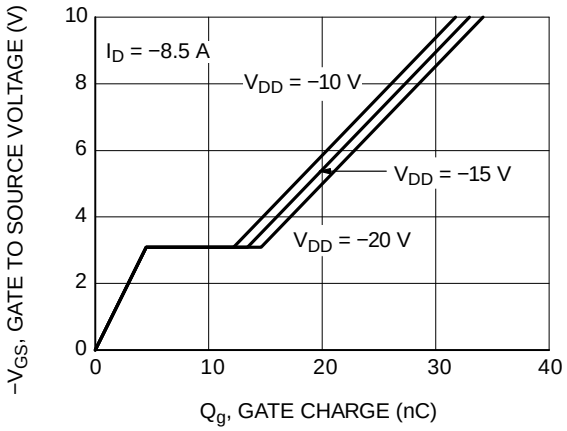

Figure 7. Gate Charge Characteristics

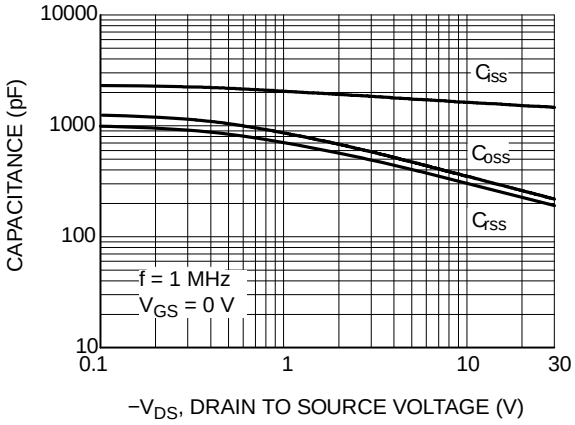

Figure 8. Capacitance vs. Drain to Source Voltage

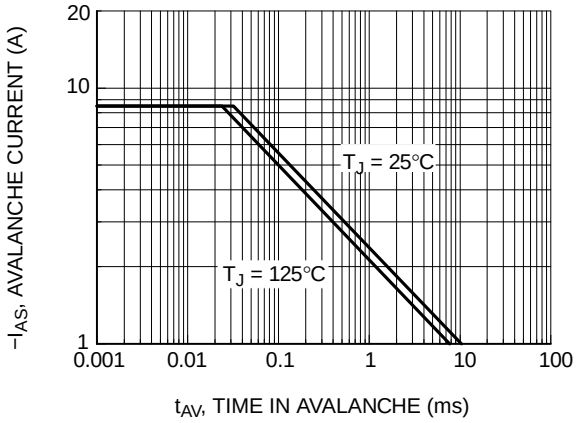

Figure 9. Unclamped Inductive Switching Capability

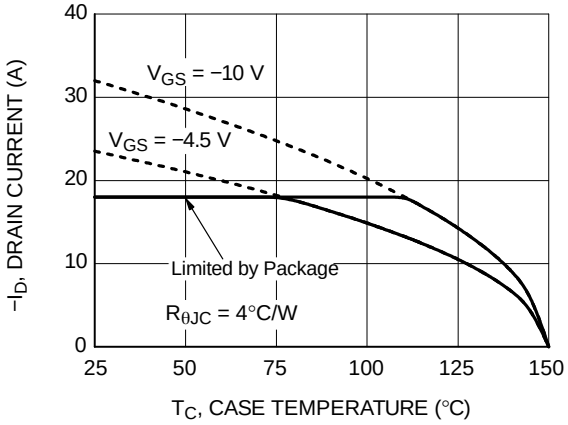

Figure 10. Maximum Continuous Drain Current vs. Case Temperature

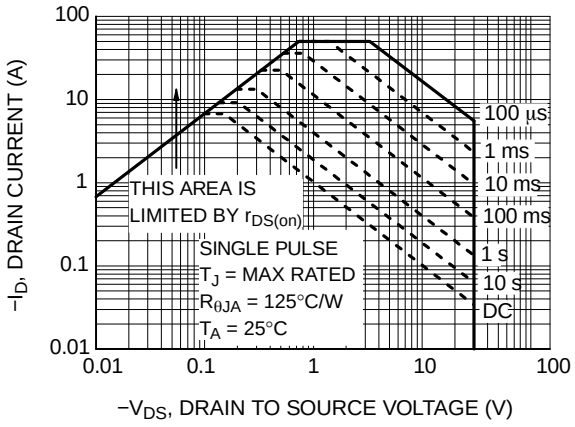

Figure 11. Forward Bias Safe Operating Area

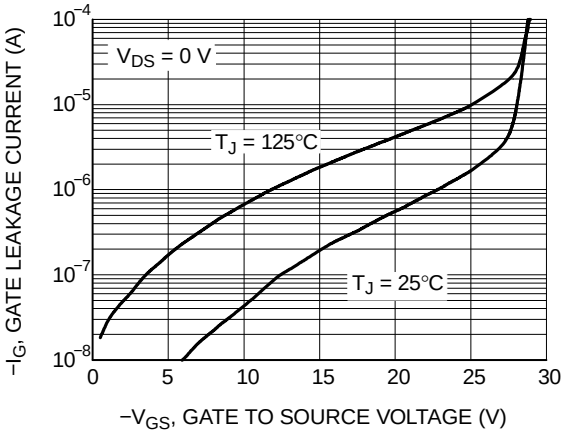

Figure 12. I_{GSS} vs. V_{GSS}

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TYPICAL CHARACTERISTICS (T_J = 25°C UNLESS OTHERWISE NOTED) (CONTINUED)

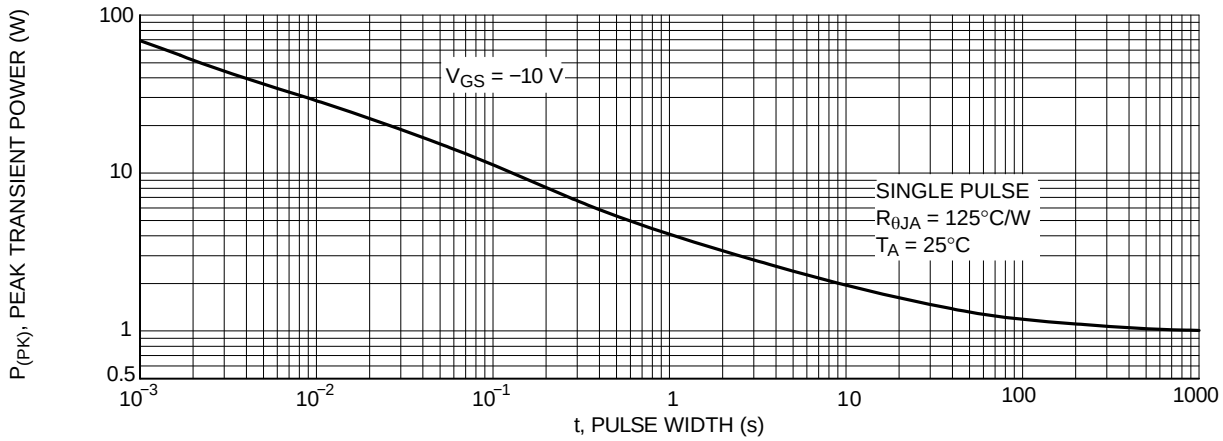

Figure 13. Single Pulse Maximum Power Dissipation

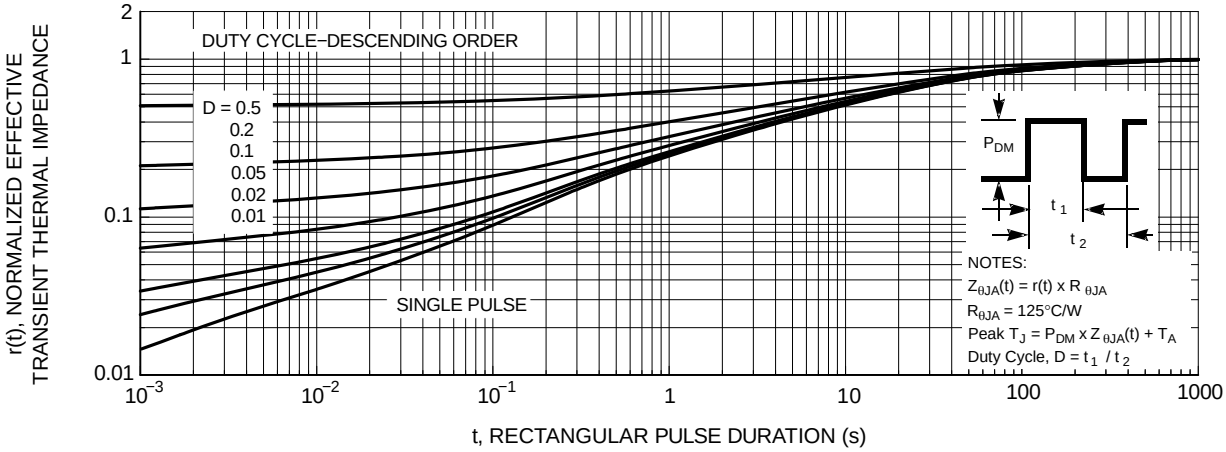

Figure 14. Junction−to−Ambient Transient Thermal Response Curve

ORDERING INFORMATION

Device	Device Marking	Package Type	Shipping†
FDMC4435BZ	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DR (Pb−Free)	3000 / Tape & Reel
FDMC4435BZ−F127	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DR (Pb−Free)	3000 / Tape & Reel

DISCONTINUED (Note 4)

FDMC4435BZ−F127−L701	FDMC4435BZ	WDFN8 3.3x3.3, 0.65P, case 511DQ (Pb−Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

4. **DISCONTINUED:** This device is not recommended for new design. Please contact your **onsemi** representative for information. The most current information on this device may be available on www.onsemi.com.

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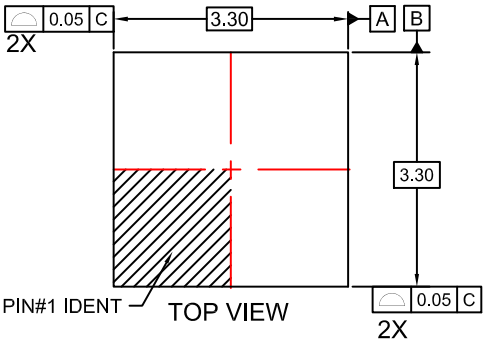
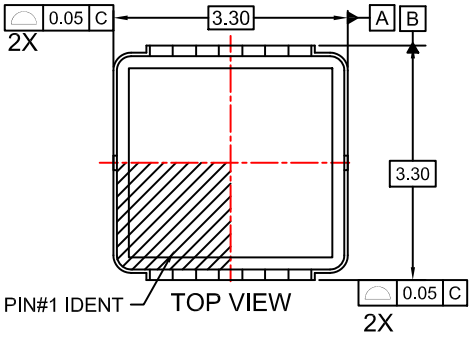
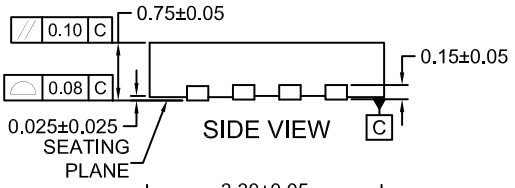
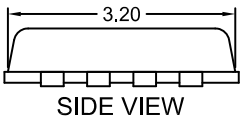
WDFN8 3.3x3.3, 0.65P
CASE 511DQ
ISSUE O

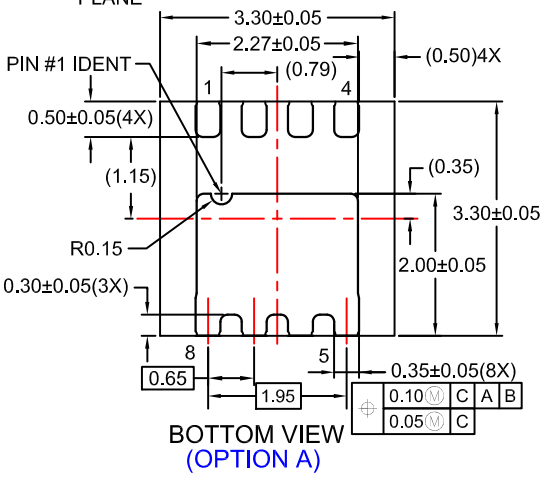
DATE 31 OCT 2016

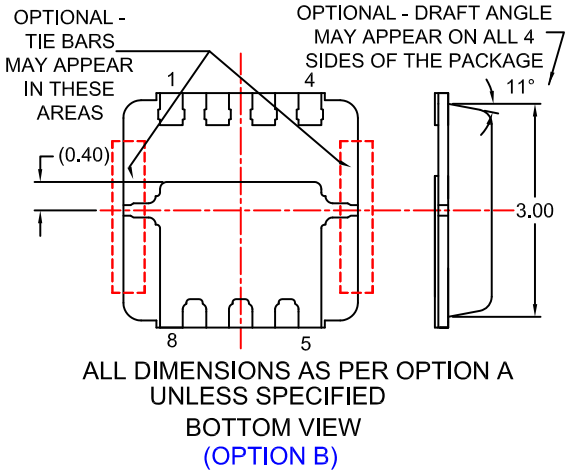


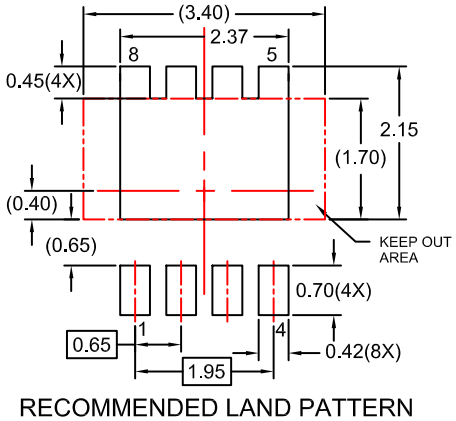












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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**		**PAGE 1 OF 2**

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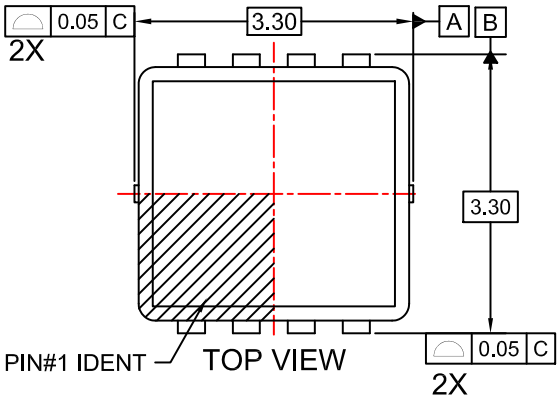
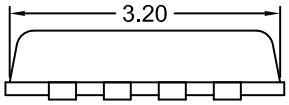
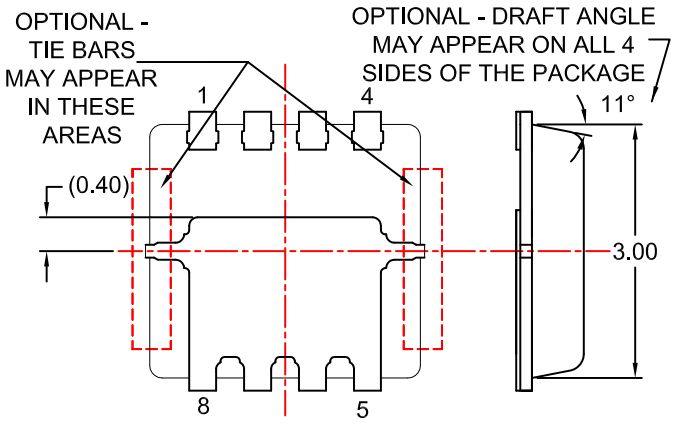
CASE 511DQ
ISSUE O

DATE 31 OCT 2016





SIDE VIEW



ALL DIMENSIONS AS PER OPTION A UNLESS SPECIFIED

BOTTOM VIEW
(OPTION C)

NOTES:

A. PACKAGE DOES NOT FULLY CONFORM TO JEDEC REGISTRATION MO-240.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN
E. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. BURRS OR MOLD FLASH SHALL NOT EXCEED 0.10MM.

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DESCRIPTION:	**WDFN8 3.3X3.3, 0.65P**		**PAGE 2 OF 2**

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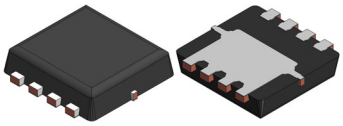
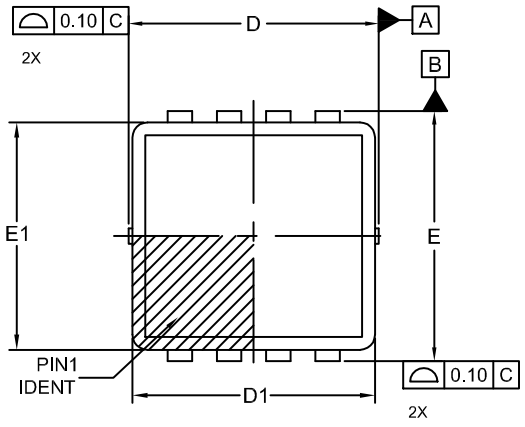
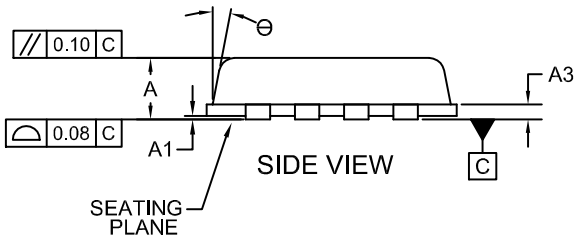


WDFN8 3.3x3.3, 0.65P
CASE 511DR
ISSUE B

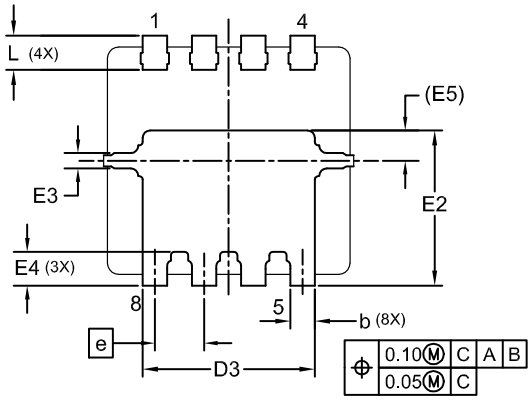
DATE 02 FEB 2022



TOP VIEW



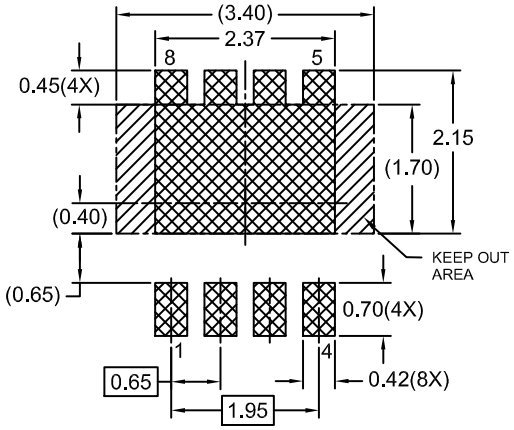
SIDE VIEW



BOTTOM VIEW

NOTES:
A. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
B. SEATING PLANE IS DEFINED BY TERMINAL TIPS ONLY
C. BODY DIMENSIONS DO NOT INCLUDE MOLD FLASH PROTRUSIONS NOR GATE BURRS. MOLD FLASH PROTRUSION OR GATE BURR DOES NOT EXCEED 0.150MM.

DIM	MILLIMETERS		
	MIN	NOM	MAX
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.15	0.20	0.25
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D1	3.10	3.20	3.30
D3	2.17	2.27	2.37
E	3.20	3.30	3.40
E1	2.90	3.00	3.10
E2	1.95	2.05	2.15
E3	0.15	0.20	0.25
E4	0.30	0.40	0.50
E5	0.40 REF		
e	0.65 BSC		
L	0.30	0.40	0.50
θ	0°	-	12°



RECOMMENDED LAND PATTERN

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

GENERIC MARKING DIAGRAM*

XXXX = Specific Device Code
A = Assembly Location
Y = Year
WW = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	**WDFN8 3.3x3.3, 0.65P**	**PAGE 1 OF 1**

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