

# MOSFET – N-Channel, POWER TRENCH®

25 V, 40 A, 5.7 mΩ

## FDMC8588

### General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low  $r_{DS(on)}$ , fast switching speed and body diode reverse recovery performance.

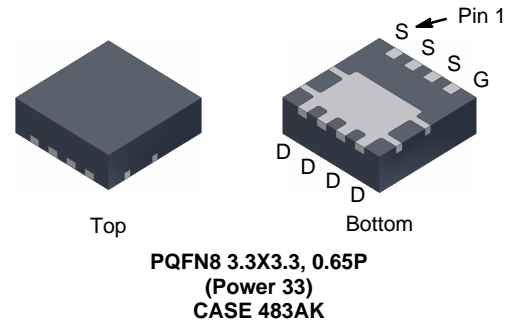
### Features

- Max  $r_{DS(on)}$  = 5.7 mΩ at  $V_{GS}$  = 4.5 V,  $I_D$  = 16.5 A
- State-of-the-art Switching Performance
- Lower Output Capacitance, Gate Resistance, and Gate Charge Boost Efficiency
- Shielded Gate Technology Reduces Switch Node Ringing and Increases Immunity to EMI and Cross Conduction
- This Device is Pb-Free, Halide Free and is RoHS Compliant

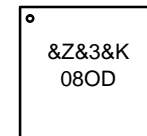
### Applications

- High Side Switching for High End Computing
- High Power Density DC-DC Synchronous Buck Converter

$V_{DS}$	$r_{DS(on)}$ MAX	$I_D$ MAX
25 V	5.7 mΩ @ 4.5 V	40 A

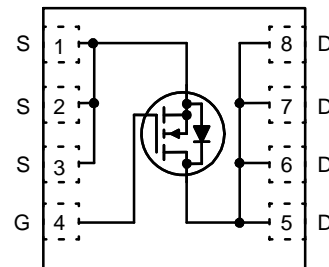


### MARKING DIAGRAM



&Z = Assembly Plant Code  
&3 = 3-Digit Date Code  
&K = 2-Digits Lot Run Traceability Code  
08OD = Device Code

### PIN ASSIGNMENT



### ORDERING INFORMATION

See detailed ordering and shipping information on page 6 of this data sheet.

# FDMC8588

## MOSFET MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$V_{DS}$	Drain to Source Voltage (Note 5)	25	V
$V_{GS}$	Gate to Source Voltage (Note 4)	$\pm 12$	V
$I_D$	Drain Current – Continuous (Package Limited) $T_C = 25^\circ\text{C}$	40	A
	– Continuous (Silicon Limited) $T_C = 25^\circ\text{C}$	59	
	– Continuous (Note 1a)	16.5	
	– Pulsed	60	
$E_{AS}$	Single Pulse Avalanche Energy (Note 3)	29	mJ
$P_D$	Power Dissipation $T_C = 25^\circ\text{C}$	26	W
	Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a)	2.4	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	$-55$ to $+150$	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

## THERMAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ , unless otherwise noted)

Symbol	Parameter	Ratings	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case $T_C = 25^\circ\text{C}$	4.7	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient $T_A = 25^\circ\text{C}$ (Note 1a)	53	

## ELECTRICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\ \mu\text{A}, V_{GS} = 0\ \text{V}$	25	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	17	–	$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20\ \text{V}, V_{GS} = 0\ \text{V}$	–	–	1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 12\ \text{V}, V_{DS} = 0\ \text{V}$	–	–	100	nA

### ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	0.8	1.4	1.8	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , referenced to $25^\circ\text{C}$	–	–4	–	$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\ \text{V}, I_D = 17\ \text{A}$	–	3.5	5.0	m $\Omega$
		$V_{GS} = 4.5\ \text{V}, I_D = 16.5\ \text{A}$	–	4.3	5.7	
		$V_{GS} = 10\ \text{V}, I_D = 17\ \text{A}, T_J = 125^\circ\text{C}$	–	4.8	6.9	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\ \text{V}, I_D = 16.5\ \text{A}$	–	85	–	S

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	$V_{DS} = 13\ \text{V}, V_{GS} = 0\ \text{V}, f = 1\ \text{MHz}$	–	1228	1720	pF
$C_{oss}$	Output Capacitance		–	441	620	pF
$C_{rss}$	Reverse Transfer Capacitance		–	69	100	pF
$R_g$	Gate Resistance		0.1	0.5	1.5	$\Omega$

**ELECTRICAL CHARACTERISTICS** ( $T_J = 25^\circ\text{C}$  unless otherwise noted) (continued)

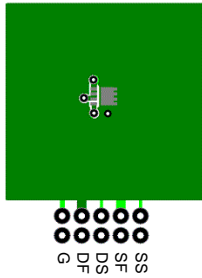
Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
<b>SWITCHING CHARACTERISTICS</b>						
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 13\text{ V}$ , $I_D = 16.5\text{ A}$ , $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\ \Omega$	–	8	16	ns
$t_r$	Rise Time		–	3	10	ns
$t_{d(off)}$	Turn-Off Delay Time		–	25	40	ns
$t_f$	Fall Time		–	2	10	ns
$Q_{g(TOT)}$	Total Gate Charge at 4.5 V	$V_{DD} = 13\text{ V}$ , $I_D = 16.5\text{ A}$	–	12	17	nC
$Q_{gs}$	Total Gate Charge		–	3.0	–	nC
$Q_{gd}$	Gate to Drain “Miller” Charge		–	3.3	–	nC

**DRAIN-SOURCE DIODE CHARACTERISTICS**

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 2\text{ A}$ (Note 2)	–	0.7	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 16.5\text{ A}$ (Note 2)	–	0.8	1.2	V
$t_{rr}$	Reverse Recovery Time	$I_F = 16.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$	–	25	–	ns
$Q_{rr}$	Reverse Recovery Charge		–	10	–	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a.  $53^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper



b.  $125^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper

- Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.
- $E_{AS}$  of 29 mJ is based on starting  $T_J = 25^\circ\text{C}$ ,  $L = 1.2\text{ mH}$ ,  $I_{AS} = 7\text{ A}$ ,  $V_{DD} = 23\text{ V}$ ,  $V_{GS} = 10\text{ V}$ . 100% tested at  $L = 0.1\text{ mH}$ ,  $I_{AS} = 16\text{ A}$ .
- As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.
- The continuous  $V_{ds}$  rating is 25 V; however, a pulse of 28 V peak voltage for no longer than 3 ns duration at 500 kHz frequency can be applied.

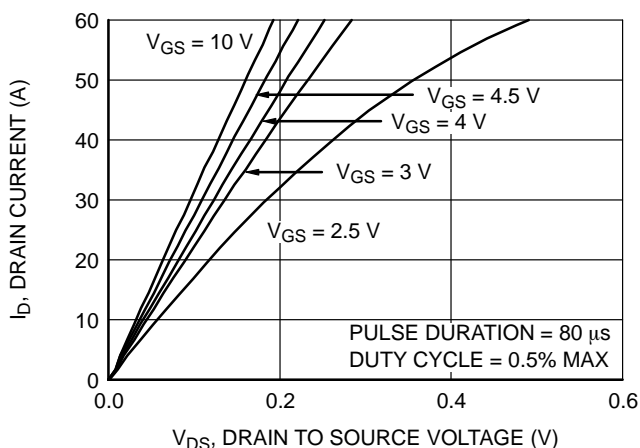
TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted)

Figure 1. On Region Characteristics

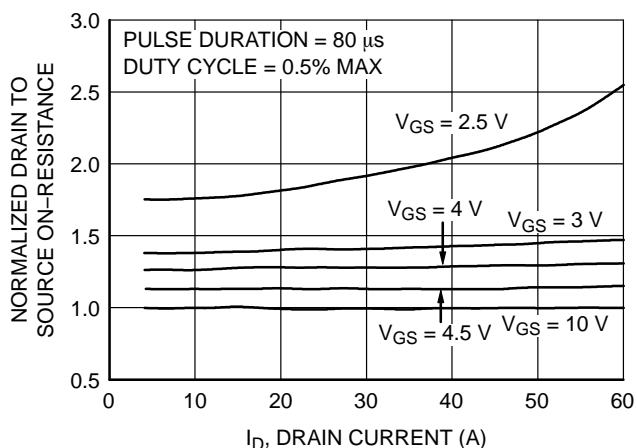


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

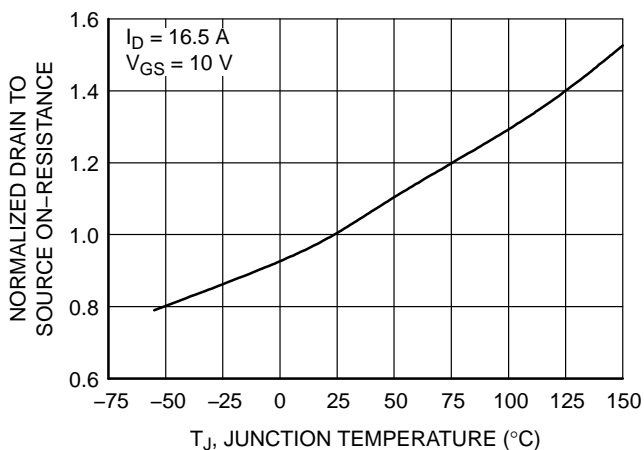


Figure 3. Normalized On Resistance vs. Junction Temperature

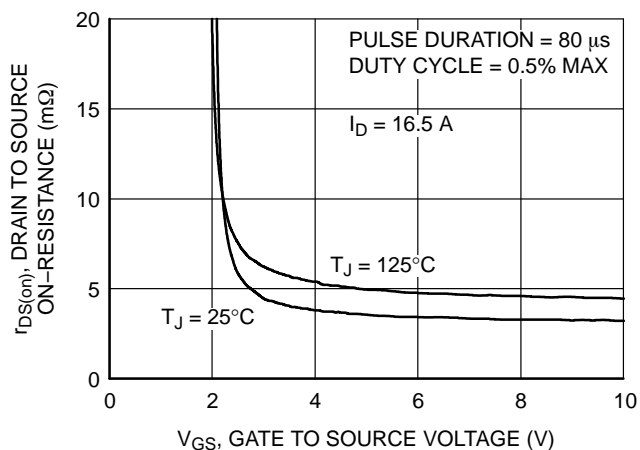


Figure 4. On-Resistance vs. Gate to Source Voltage

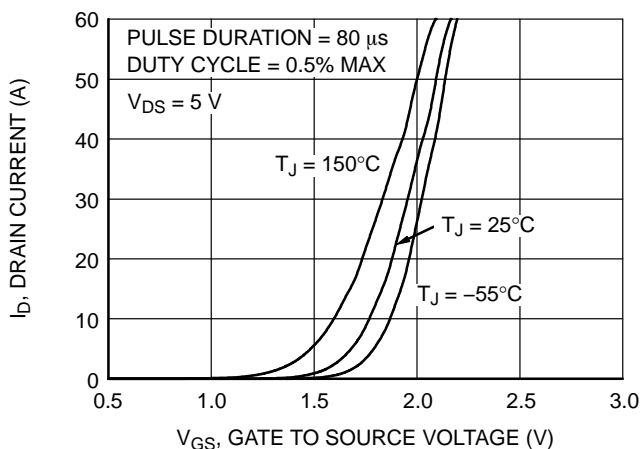


Figure 5. Transfer Characteristics

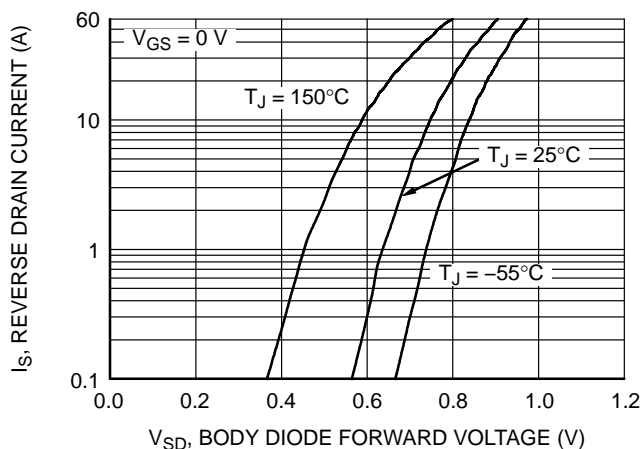


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

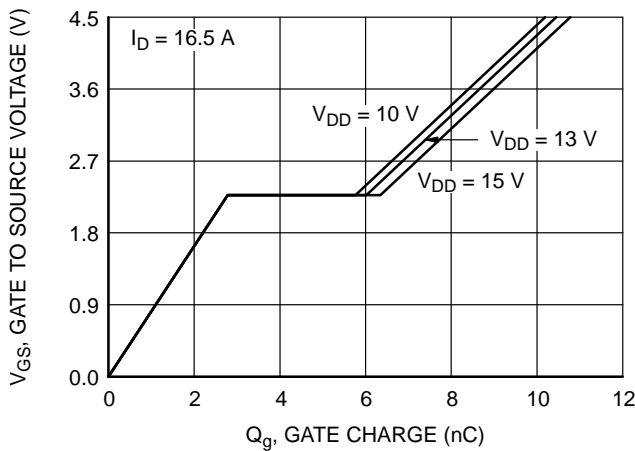


Figure 7. Gate Charge Characteristics

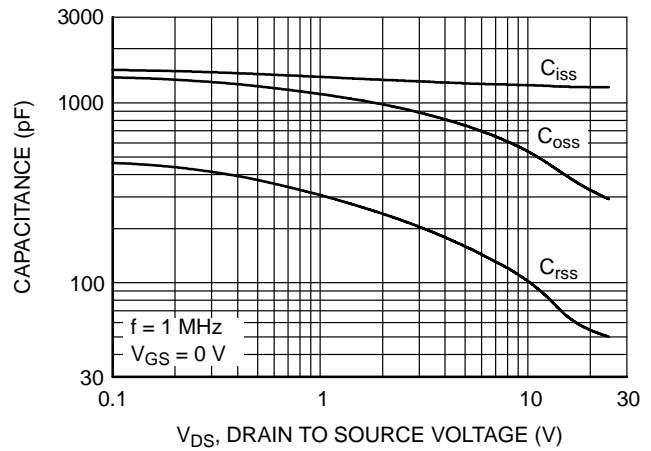


Figure 8. Capacitance vs. Drain to Source Voltage

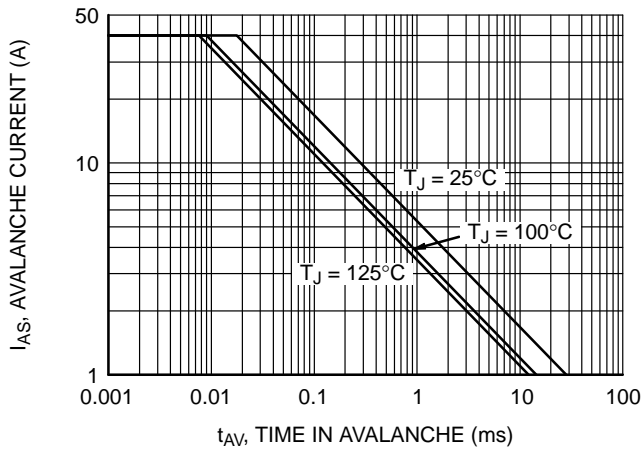


Figure 9. Unclamped Inductive Switching Capability

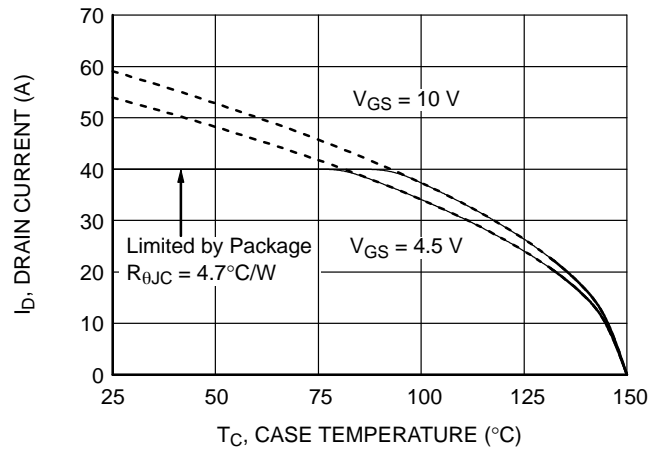


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

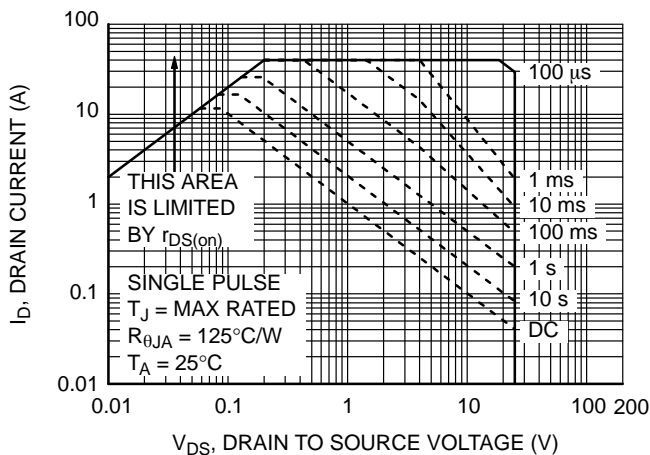


Figure 11. Forward Bias Safe Operating Area

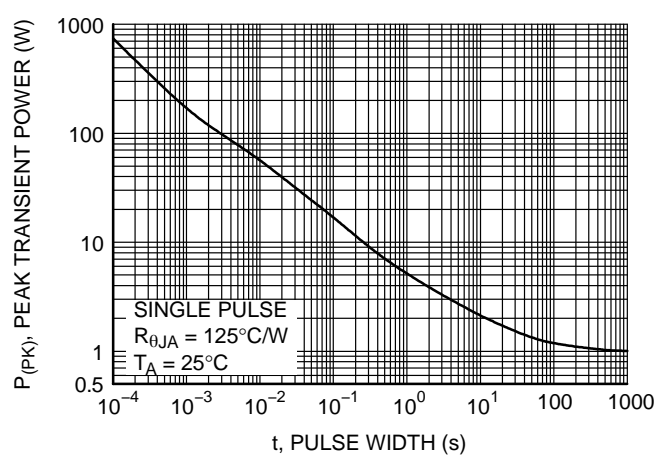


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS ( $T_J = 25^\circ\text{C}$ , unless otherwise noted) (continued)

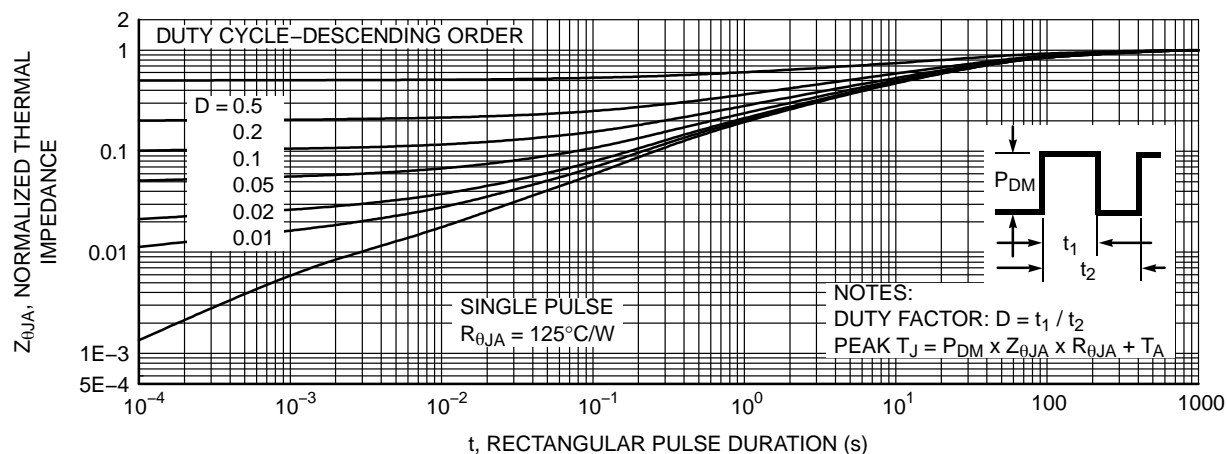
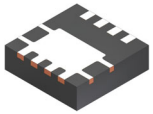


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

PACKAGE MARKING AND ORDERING INFORMATION

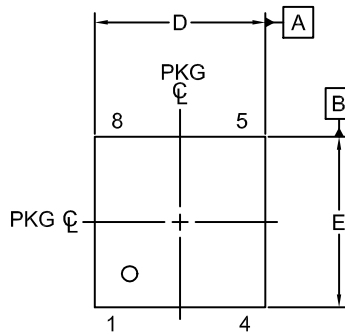
Device	Device Marking	Package	Reel Size	Tape Width	Shipping†
FDMC8588	08OD	PQFN8 3.3X3.3, 0.65P (Power 33) (Pb-Free, Halide Free)	13"	12 mm	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

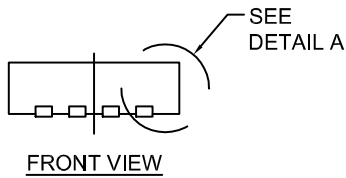


**PQFN8 3.3X3.3, 0.65P**  
**CASE 483AK**  
**ISSUE B**

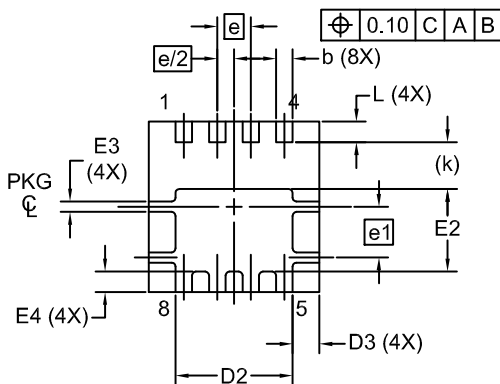
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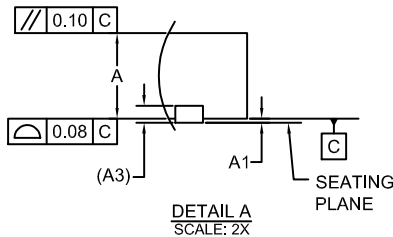
**TOP VIEW**



**FRONT VIEW**

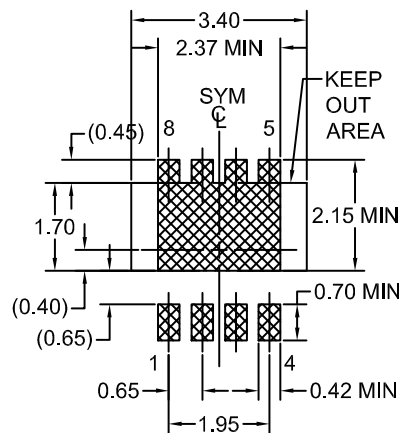


**BOTTOM VIEW**



**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



**LAND PATTERN  
RECOMMENDATION**

\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF		
b	0.27	0.32	0.37
D	3.20	3.30	3.40
D2	2.17	2.27	2.37
D3	0.42	0.52	0.62
E	3.20	3.30	3.40
E2	1.50	1.60	1.70
E3	0.10	0.20	0.30
E4	0.29	0.39	0.49
e	0.65 BSC		
e/2	0.325 BSC		
e1	0.98 BSC		
k	0.91 REF		
L	0.30	0.40	0.50

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