

MOSFET – N-Channel, POWERTRENCH®

80 V, 22 A, 11.7 mΩ

FDMC86320

General Description

This N-Channel MOSFET has been designed specifically to improve the overall efficiency and to minimize switch node ringing of DC/DC converters using either synchronous or conventional switching PWM controllers. It has been optimized for low gate charge, low $r_{DS(on)}$, fast switching speed and body diode reverse recovery performance.

Features

- Max $r_{DS(on)}$ = 11.7 mΩ at $V_{GS} = 10\text{ V}$, $I_D = 10.7\text{ A}$
- Max $r_{DS(on)}$ = 16 mΩ at $V_{GS} = 8\text{ V}$, $I_D = 8.5\text{ A}$
- MSL1 Robust Package Design
- 100% UIL Tested
- These Devices are Pb-Free, Halide Free and are RoHS Compliant

Applications

- Primary DC-DC Switch
- Motor Bridge Switch
- Synchronous Rectifier

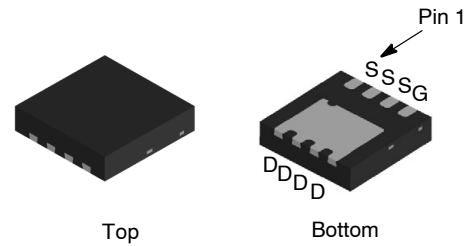
MOSFET MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

| Symbol | Parameter | Ratings | Units |
|----------------|--|-------------|------------------|
| V_{DS} | Drain to Source Voltage | 80 | V |
| V_{GS} | Gate to Source Voltage | ±20 | V |
| I_D | Drain Current | | A |
| | –Continuous $T_C = 25^\circ\text{C}$ | 22 | |
| | –Continuous $T_A = 25^\circ\text{C}$ (Note 1a) | 10.7 | |
| | –Pulsed | 50 | |
| EAS | Single Pulse Avalanche Energy (Note 3) | 60 | mJ |
| P_D | Power Dissipation $T_C = 25^\circ\text{C}$ | 40 | W |
| | Power Dissipation $T_A = 25^\circ\text{C}$ (Note 1a) | 2.3 | |
| T_J, T_{STG} | Operating and Storage Junction Temperature Range | –55 to +150 | $^\circ\text{C}$ |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

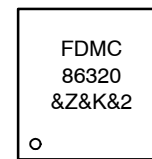
THERMAL CHARACTERISTICS

| Symbol | Parameter | Ratings | Unit |
|-----------------|---|---------|---------------------------|
| $R_{\theta JC}$ | Thermal Resistance, Junction to Case (Note 1) | 3.1 | $^\circ\text{C}/\text{W}$ |
| $R_{\theta JA}$ | Thermal Resistance, Junction to Ambient (Note 1a) | 53 | $^\circ\text{C}/\text{W}$ |



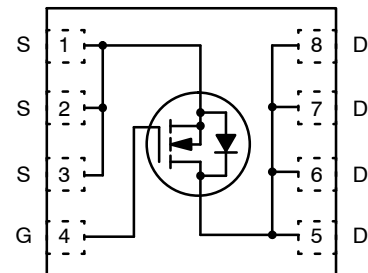
WDFN8 3.3x3.3, 0.65P
CASE 511DH

MARKING DIAGRAM



FDMC = Specific Device Code
86320 = Specific Device Code
&Z = Assembly Location
&K = Lot Run Traceability Code
&2 = Date Code (Year and Week)

PIN ASSIGNMENT



N-Channel MOSFET

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

FDMC86320

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|-------------------------------------|---|--|-----|-----|------|-------|
| OFF CHARACTERISTICS | | | | | | |
| BV _{DSS} | Drain to Source Breakdown Voltage | I _D = 250 μA, V _{GS} = 0 V | 80 | | | V |
| ΔBV _{DSS} /ΔT _J | Breakdown Voltage Temperature Coefficient | I _D = 250 μA, referenced to 25°C | | 56 | | mV/°C |
| I _{DSS} | Zero Gate Voltage Drain Current | V _{DS} = 48 V, V _{GS} = 0 V | | | 1 | μA |
| I _{GSS} | Gate to Source Leakage Current | V _{GS} = ±20 V, V _{DS} = 0 V | | | ±100 | nA |

ON CHARACTERISTICS

| | | | | | | |
|---------------------------------------|--|---|-----|------|------|-------|
| V _{GS(th)} | Gate to Source Threshold Voltage | V _{GS} = V _{DS} , I _D = 250 μA | 2.4 | 3.5 | 4.5 | V |
| ΔV _{GS(th)} /ΔT _J | Gate to Source Threshold Voltage Temperature Coefficient | I _D = 250 μA, referenced to 25°C | | -11 | | mV/°C |
| r _{DS(on)} | Static Drain to Source On Resistance | V _{GS} = 10 V, I _D = 10.7 A | | 9.7 | 11.7 | mΩ |
| | | V _{GS} = 8 V, I _D = 8.5 A | | 11.4 | 16 | |
| | | V _{GS} = 10 V, I _D = 10.7 A, T _J = 125°C | | 15 | 18 | |
| g _{FS} | Forward Transconductance | V _{DS} = 10 V, I _D = 10.7 A | | 20 | | S |

DYNAMIC CHARACTERISTICS

| | | | | | | |
|------------------|------------------------------|---|--|------|------|----|
| C _{iss} | Input Capacitance | V _{DS} = 40 V, V _{GS} = 0 V, f = 1 MHz | | 1985 | 2640 | pF |
| C _{oss} | Output Capacitance | | | 353 | 469 | pF |
| C _{rss} | Reverse Transfer Capacitance | | | 12 | 30 | pF |
| R _g | Gate Resistance | | | 0.5 | | Ω |

SWITCHING CHARACTERISTICS

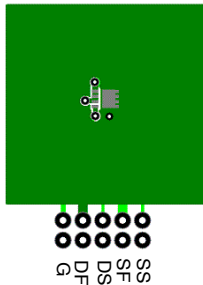
| | | | | | | |
|---------------------|-------------------------------|--|---|-----|----|----|
| t _{d(on)} | Turn-On Delay Time | V _{DD} = 40 V, I _D = 10.7 A, V _{GS} = 10 V, R _{GEN} = 6 Ω | | 15 | 28 | ns |
| t _r | Rise Time | | | 8 | 16 | ns |
| t _{d(off)} | Turn-Off Delay Time | | | 20 | 35 | ns |
| t _f | Fall Time | | | 5 | 10 | ns |
| Q _{g(TOT)} | Total Gate Charge | V _{GS} = 0 V to 10 V | V _{DD} = 40 V I _D = 10.7 A | 29 | 41 | nC |
| Q _{g(TOT)} | Total Gate Charge | V _{GS} = 0 V to 8 V | | 24 | 34 | nC |
| Q _{gs} | Gate to Source Charge | | | 10 | | nC |
| Q _{gd} | Gate to Drain "Miller" Charge | | | 6.9 | | nC |

DRAIN-SOURCE DIODE CHARACTERISTICS

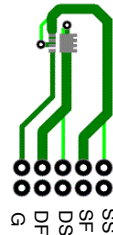
| | | | | | | |
|-----------------|---------------------------------------|---|--|------|-----|----|
| V _{SD} | Source to Drain Diode Forward Voltage | V _{GS} = 0 V, I _S = 10.7 A (Note 2) | | 0.84 | 1.3 | V |
| | | V _{GS} = 0 V, I _S = 2 A (Note 2) | | 0.75 | 1.2 | |
| t _{rr} | Reverse Recovery Time | I _F = 10.7 A, di/dt = 100 A/μs | | 38 | 61 | ns |
| Q _{rr} | Reverse Recovery Charge | | | 27 | 43 | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. R_{θJA} is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R_{θJC} is guaranteed by design while R_{θCA} is determined by the user's board design.



a. 53 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0 %.
3. Starting T_J = 25 °C, N-ch: L = 0.3 mH, I_{AS} = 20 A, V_{DD} = 72 V, V_{GS} = 10 V.

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

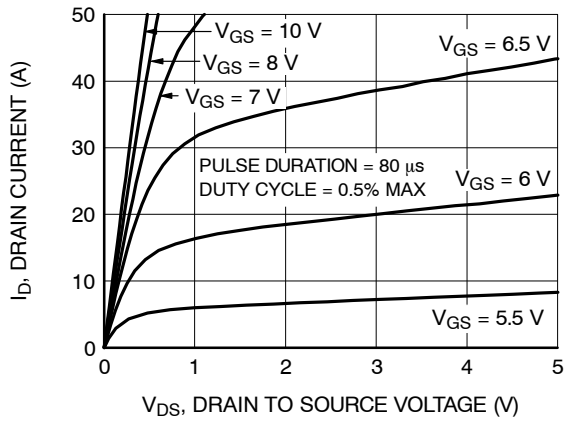


Figure 1. On-Region Characteristics

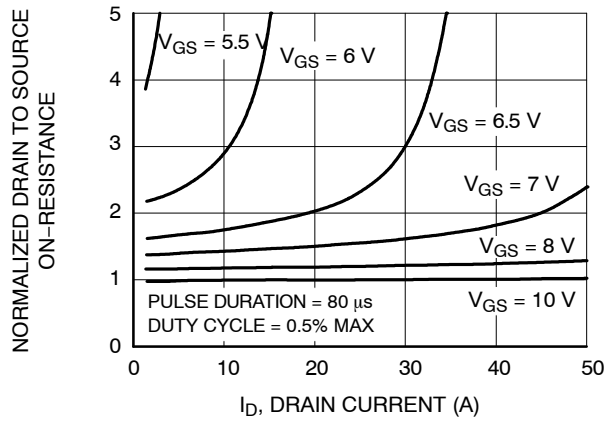


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

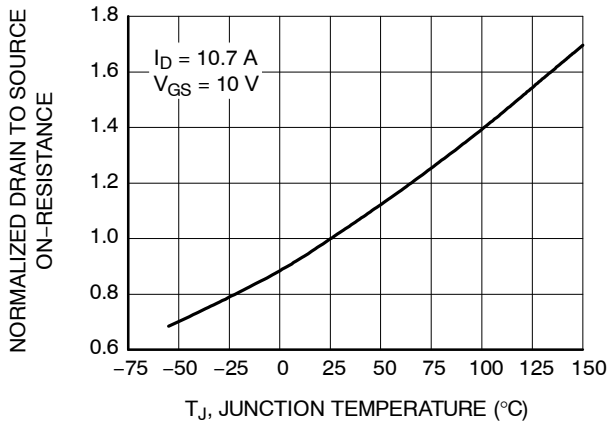


Figure 3. Normalized On-Resistance vs. Junction Temperature

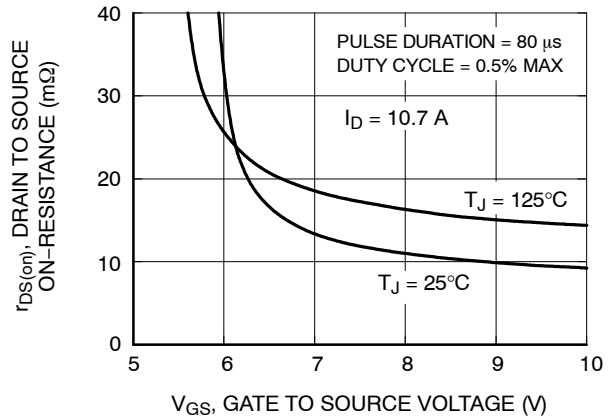


Figure 4. On-Resistance vs. Gate to Source Voltage

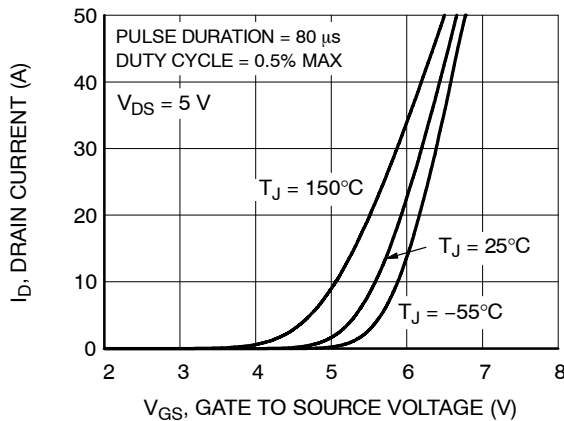


Figure 5. Transfer Characteristics

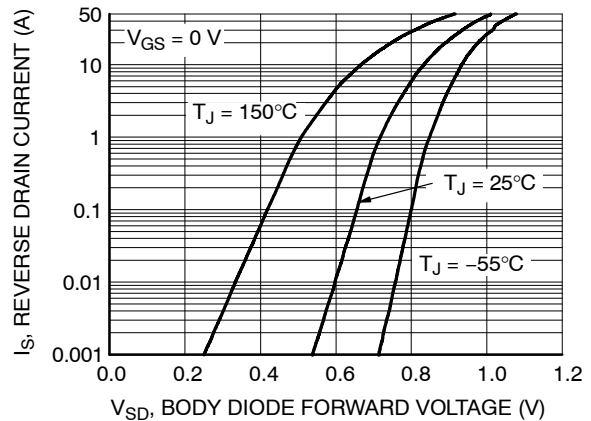


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

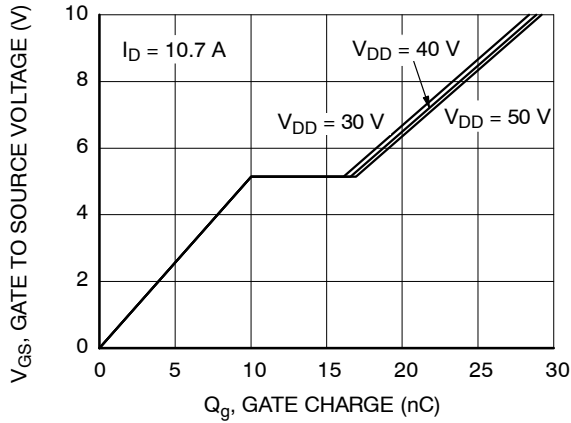


Figure 7. Gate Charge Characteristics

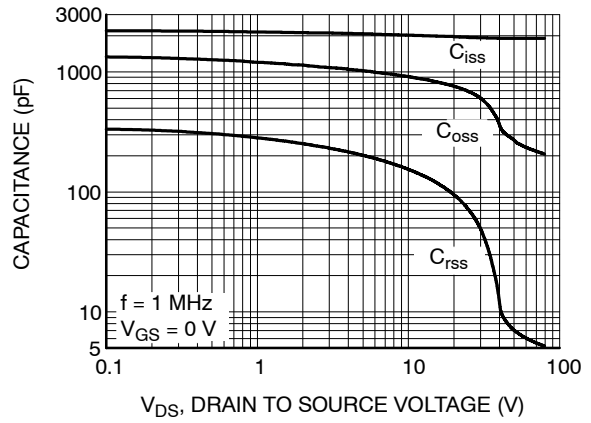


Figure 8. Capacitance vs. Drain to Source Voltage

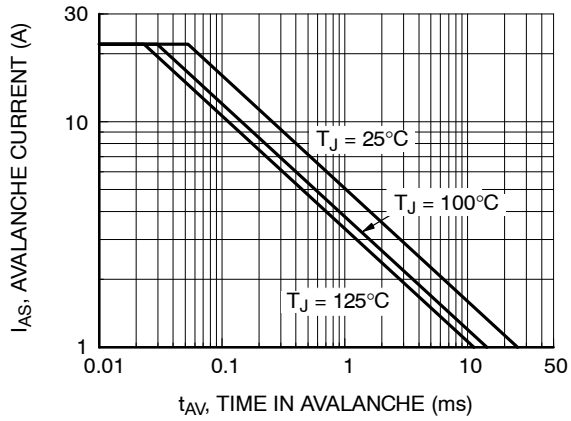


Figure 9. Unclamped Inductive Switching Capability

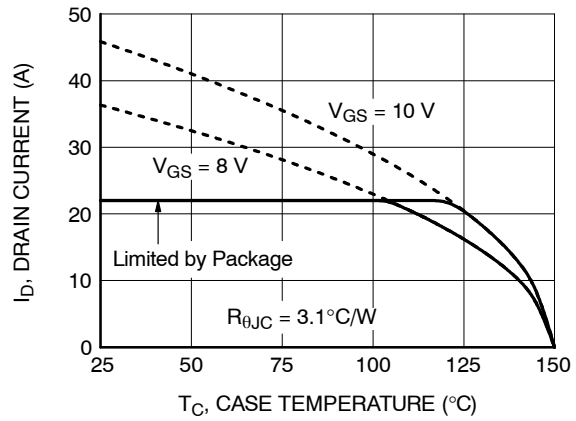


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

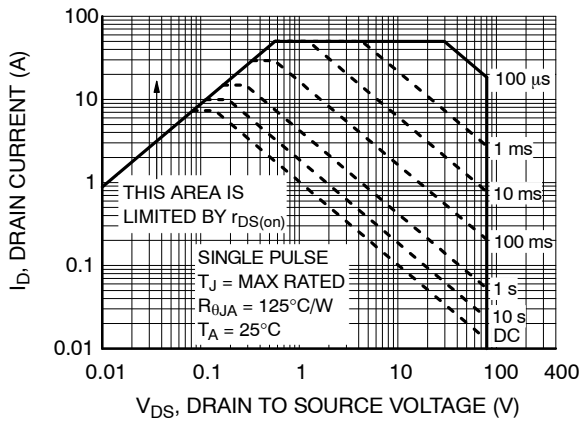


Figure 11. Forward Bias Safe Operating Area

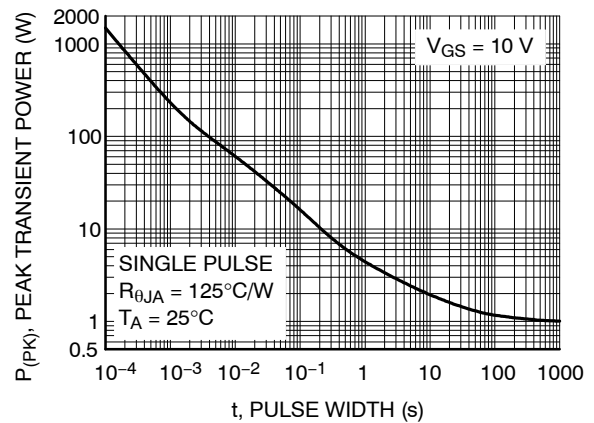


Figure 12. Single Pulse Maximum Power Dissipation

FDMC86320

TYPICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

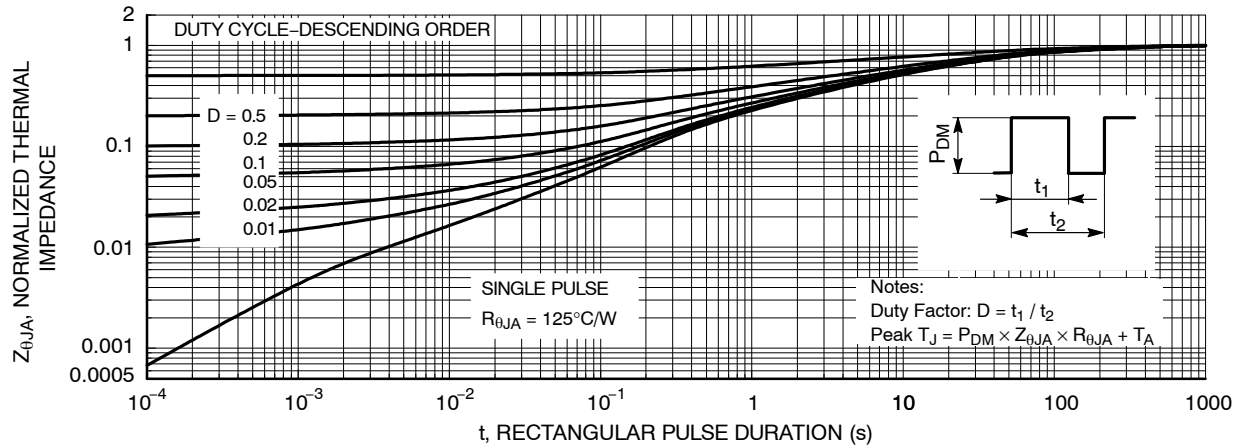


Figure 13. Junction-to-Case Transient Thermal Response Curve

ORDERING INFORMATION

| Device | Device Marking | Package Type | Shipping [†] |
|-----------|----------------|-----------------------------------|-----------------------|
| FDMC86320 | FDMC86320 | WDFN8 3.3x3.3, 0.65P (Pb-Free) | 3000 / Tape & Reel |

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

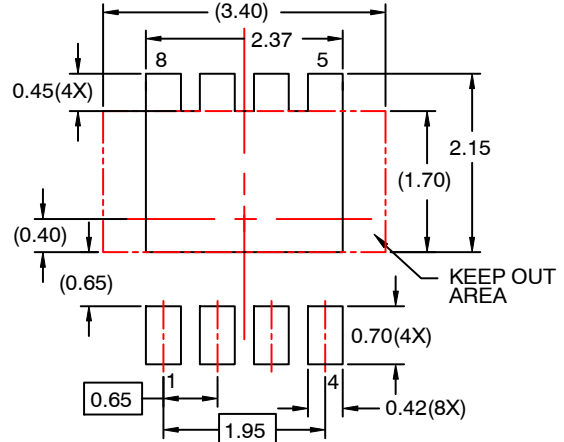
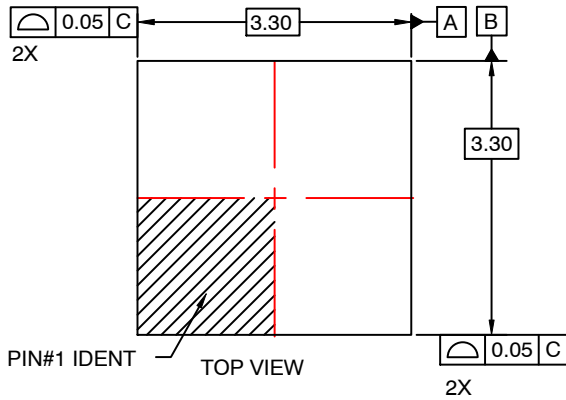
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MECHANICAL CASE OUTLINE
PACKAGE DIMENSIONS

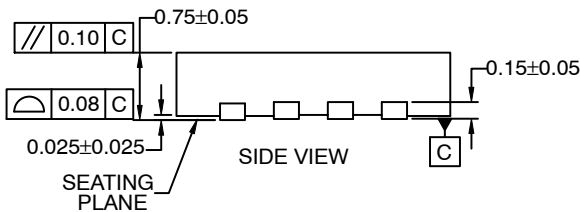


WDFN8 3.3x3.3, 0.65P
CASE 511DH
ISSUE O

DATE 31 JUL 2016

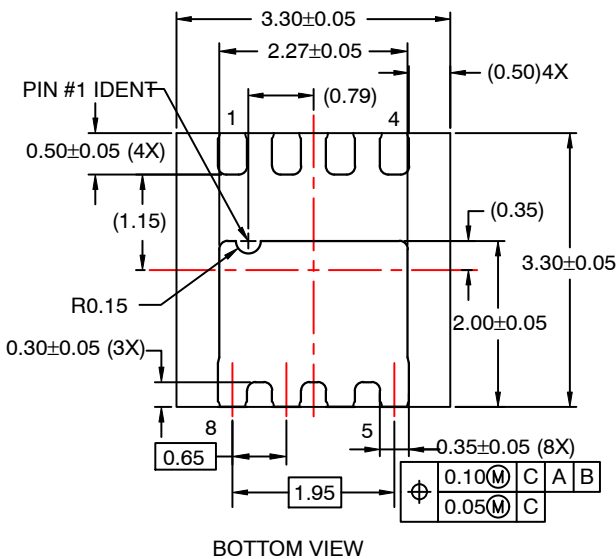


RECOMMENDED LAND PATTERN



NOTES:

- A. DOES NOT CONFORM TO JEDEC REGISTRATION MO-229
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS AND TOLERANCES PER ASME Y14.5M, 2009.
- D. LAND PATTERN RECOMMENDATION IS EXISTING INDUSTRY LAND PATTERN.



BOTTOM VIEW

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|-------------------------|-----------------------------|--|
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