

# FDMS001N025DSD

## PowerTrench® Power Clip

### 25 V Asymmetric Dual N-Channel MOSFET

#### General Description

This device includes two specialized N-Channel MOSFETs in a dual package. The switch node has been internally connected to enable easy placement and routing of synchronous buck converters. The control MOSFET (Q1) and synchronous SyncFET (Q2) have been designed to provide optimal power efficiency.

#### Features

Q1: N-Channel

- Max  $r_{DS(on)}$  = 3.25 mΩ at  $V_{GS} = 10$  V,  $I_D = 19$  A
- Max  $r_{DS(on)}$  = 4 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 17$  A

Q2: N-Channel

- Max  $r_{DS(on)}$  = 0.92 mΩ at  $V_{GS} = 10$  V,  $I_D = 38$  A
- Max  $r_{DS(on)}$  = 1.20 mΩ at  $V_{GS} = 4.5$  V,  $I_D = 34$  A
- Low Inductance Packaging Shortens Rise/Fall Times, Resulting in Lower Switching Losses
- MOSFET Integration Enables Optimum Layout for Lower Circuit Inductance and Reduced Switch Node Ringing
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

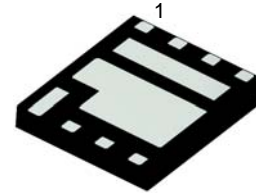
#### Applications

- Computing
- Communications
- General Purpose Point of Load

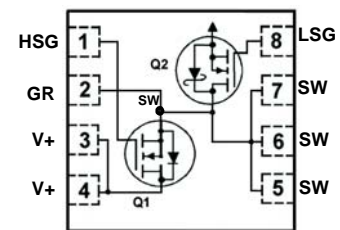
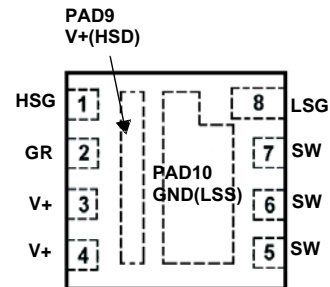


ON Semiconductor®

[www.onsemi.com](http://www.onsemi.com)



PQFN8  
POWER CLIP  
CASE 483AR



#### PIN ASSIGNMENT

Pin	Name	Description
1	HSG	High Side Gate
2	GR	Gate Return
3,4,9	V+(HSD)	High Side Drain
5,6,7	SW	Switching Node, Low Side Drain
8	LSG	Low Side Gate
10	GND(LSS)	Low Side Source

#### ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

# FDMS001N025DSD

**Table 1. MAXIMUM RATINGS**  $T_A = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Q1	Q2	Units	
$V_{DS}$	Drain to Source Voltage	25 (Note 1)	25	V	
$V_{GS}$	Gate to Source Voltage	+16/-12V	+16/-12V	V	
$I_D$	Drain Current –Continuous	$T_C = 25^\circ\text{C}$ (Note 2)	69	165	A
	–Continuous	$T_C = 100^\circ\text{C}$ (Note 2)	43	104	
	–Continuous	$T_A = 25^\circ\text{C}$	19 (Note 7a)	38 (Note 7b)	
	–Pulsed	$T_A = 25^\circ\text{C}$ (Note 3)	381	1240	
$E_{AS}$	Single Pulse Avalanche Energy	(Note 4)	121	337	mJ
$P_D$	Power Dissipation for Single Operation	$T_C = 25^\circ\text{C}$	26	42	W
	Power Dissipation for Single Operation	$T_A = 25^\circ\text{C}$	2.1 (Note 7a)	2.3 (Note 7b)	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150		$^\circ\text{C}$	

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

- The continuous  $V_{DS}$  rating is 25 V; However, a pulse of 30 V peak voltage for no longer than 100 ns duration at 600 KHz frequency can be applied.
- Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.
- Pulsed  $I_D$  please refer to Figure 11 and Figure 24 SOA graphs for more details.
- Q1:  $E_{AS}$  of 121 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N–ch:  $L = 3$  mH,  $I_{AS} = 9$  A,  $V_{DD} = 25$  V. 100% tested at  $L = 0.1$  mH,  $I_{AS} = 29$  A.  
Q2:  $E_{AS}$  of 337 mJ is based on starting  $T_J = 25^\circ\text{C}$ ; N–ch:  $L = 3$  mH,  $I_{AS} = 15$  A,  $V_{DD} = 25$  V. 100% tested at  $L = 0.1$  mH,  $I_{AS} = 48$  A.

**Table 2. THERMAL CHARACTERISTICS**

Symbol	Parameter	Q1	Q2	Units
$R_{\theta JC}$	Thermal Resistance, Junction to Case	4.9	3.0	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	60 (Note 7a)	55 (Note 7b)	
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	130 (Note 7c)	120 (Note 7d)	

**Table 3. ELECTRICAL CHARACTERISTICS**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>OFF CHARACTERISTICS</b>							
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 1$ mA, $V_{GS} = 0$ V $I_D = 1$ mA, $V_{GS} = 0$ V	Q1 Q2	25 25			V
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 10$ mA, referenced to $25^\circ\text{C}$ $I_D = 10$ mA, referenced to $25^\circ\text{C}$	Q1 Q2		15 28		$\text{mV}/^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 20$ V, $V_{GS} = 0$ V $V_{DS} = 20$ V, $V_{GS} = 0$ V	Q1 Q2			1 500	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current	$V_{GS} = +16$ V/-12 V, $V_{DS} = 0$ V $V_{GS} = +16$ V/-12 V, $V_{DS} = 0$ V	Q1 Q2			$\pm 100$ $\pm 100$	nA nA
<b>ON CHARACTERISTICS</b>							
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 320$ $\mu\text{A}$ $V_{GS} = V_{DS}$ , $I_D = 1$ mA	Q1 Q2	0.8 1.0	1.3 1.5	2.5 3.0	V
$\Delta V_{GS(th)}/\Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 1$ mA, referenced to $25^\circ\text{C}$ $I_D = 10$ mA, referenced to $25^\circ\text{C}$	Q1 Q2		–4 –3		$\text{mV}/^\circ\text{C}$
$r_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 10$ V, $I_D = 19$ A $V_{GS} = 4.5$ V, $I_D = 17$ A $V_{GS} = 10$ V, $I_D = 19$ A, $T_J = 125^\circ\text{C}$	Q1		2.5 3.0 3.5	3.25 4.0 5.0	m $\Omega$
		$V_{GS} = 10$ V, $I_D = 38$ A $V_{GS} = 4.5$ V, $I_D = 34$ A $V_{GS} = 10$ V, $I_D = 38$ A, $T_J = 125^\circ\text{C}$	Q2		0.70 0.92 0.96	0.92 1.20 1.38	

# FDMS001N025DSD

**Table 3. ELECTRICAL CHARACTERISTICS**  $T_J = 25^\circ\text{C}$  unless otherwise noted

Symbol	Parameter	Test Conditions	Type	Min	Typ	Max	Units
<b>ON CHARACTERISTICS</b>							
$g_{FS}$	Forward Transconductance	$V_{DS} = 5\text{ V}, I_D = 19\text{ A}$	Q1		98		S
		$V_{DS} = 5\text{ V}, I_D = 38\text{ A}$	Q2		262		

### DYNAMIC CHARACTERISTICS

$C_{iss}$	Input Capacitance	Q1: $V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1		1370		pF
			Q2		5105		
$C_{oss}$	Output Capacitance	Q2: $V_{DS} = 13\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	Q1		625		pF
			Q2		1810		
$C_{rss}$	Reverse Transfer Capacitance		Q1		44		pF
			Q2		173		
$R_g$	Gate Resistance		Q1	0.1	0.4	1.2	$\Omega$
			Q2	0.1	0.3	1.0	

### SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	Q1: $V_{DD} = 13\text{ V}, I_D = 19\text{ A}, R_{GEN} = 6\ \Omega$	Q1		8	16	ns	
			Q2		15	26		
$t_r$	Rise Time	Q2: $V_{DD} = 13\text{ V}, I_D = 38\text{ A}, R_{GEN} = 6\ \Omega$	Q1		2	10	ns	
			Q2		5	10		
$t_{d(off)}$	Turn-Off Delay Time		Q1		22	34	ns	
			Q2		39	62		
$t_f$	Fall Time		Q1		2	10	ns	
			Q2		4	10		
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 10\text{ V}$	Q1 $V_{DD} = 13\text{ V}, I_D = 19\text{ A}$	Q1		21	30	nC
				Q2		75	104	
$Q_g$	Total Gate Charge	$V_{GS} = 0\text{ V to } 4.5\text{ V}$	Q2 $V_{DD} = 13\text{ V}, I_D = 38\text{ A}$	Q1		9.7	14	nC
				Q2		35	49	
$Q_{gs}$	Gate to Source Gate Charge			Q1		2.9		nC
				Q2		12		
$Q_{gd}$	Gate to Drain "Miller" Charge			Q1		2.0		nC
				Q2		7.9		

### DRAIN-SOURCE DIODE CHARACTERISTICS

$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 19\text{ A}$ (Note 6) $V_{GS} = 0\text{ V}, I_S = 38\text{ A}$ (Note 6)	Q1		0.8	1.2	V
			Q2		0.8	1.2	
$I_S$	Diode continuous forward current	$T_C = 25^\circ\text{C}$ (Note 2)	Q1			69	A
			Q2			125	
$I_{S,pulse}$	Diode pulse current	$T_C = 25^\circ\text{C}$ (Note 3)	Q1			381	A
			Q2			1240	
$t_{rr}$	Reverse Recovery Time	Q1 $I_F = 19\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$ Q2 $I_F = 38\text{ A}, di/dt = 300\text{ A}/\mu\text{s}$	Q1		27	44	ns
			Q2		39	62	
$Q_{rr}$	Reverse Recovery Charge		Q1		12	21	nC
			Q2		55	87	

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

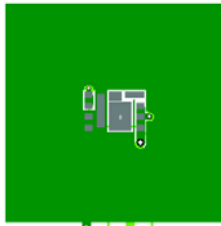
5.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta CA}$  is determined by the user's board design.

6. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0%.

### PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS001N025DSD	FDMS001N025DSD	Power Clip 56	13"	12 mm	3000 units

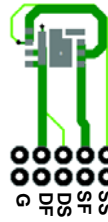
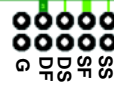
# FDMS001N025DSD



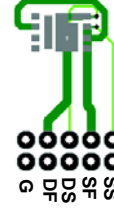
(Note 7a)



(Note 7b)



(Note 7c)



(Note 7d)

7. a) 60°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper  
b) 55°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper  
c) 130°C/W when mounted on a minimum pad of 2 oz copper  
d) 120°C/W when mounted on a minimum pad of 2 oz copper

TYPICAL CHARACTERISTICS (Q1 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

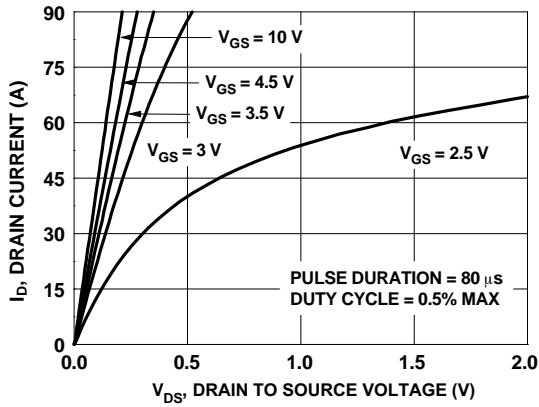


Figure 1. On Region Characteristics

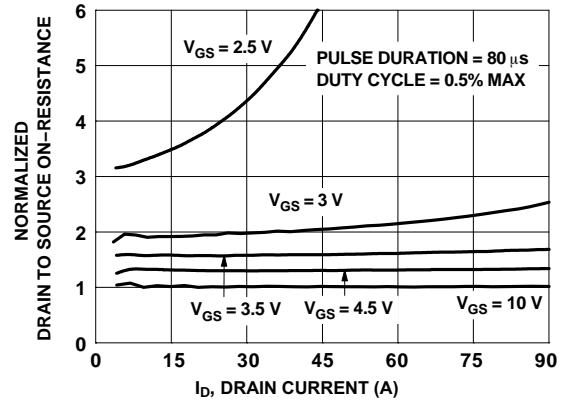


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

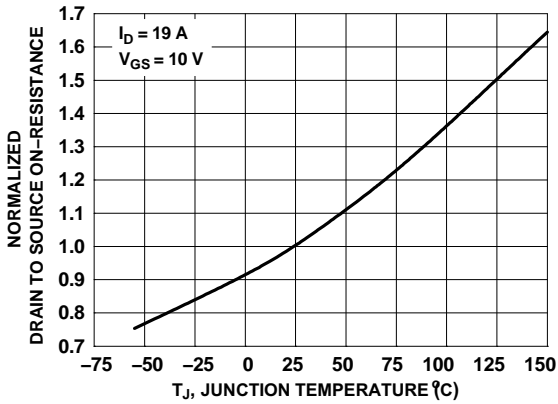


Figure 3. Normalized On Resistance vs. Junction Temperature

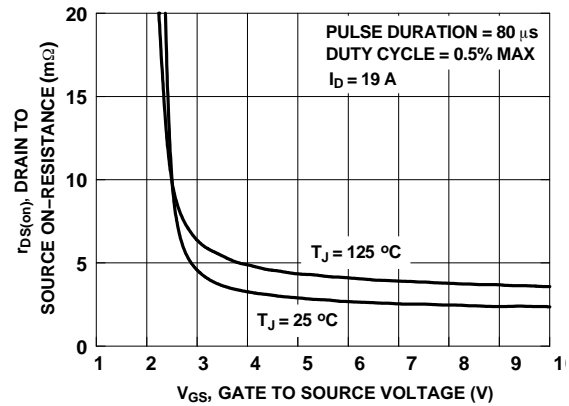


Figure 4. On-Resistance vs. Gate to Source Voltage

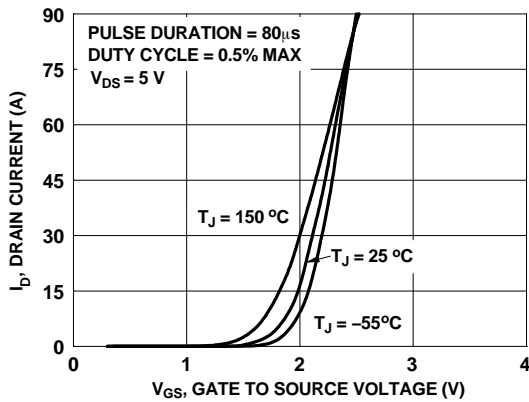


Figure 5. Transfer Characteristics

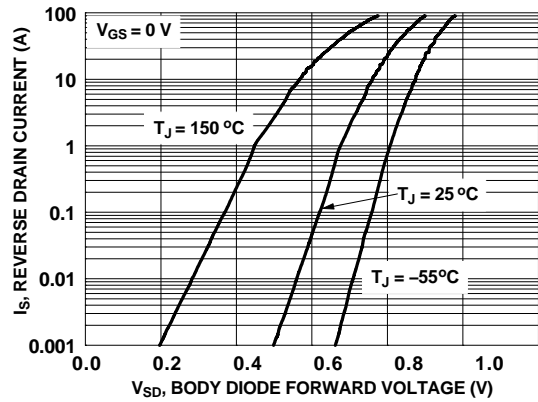


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (Q1 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

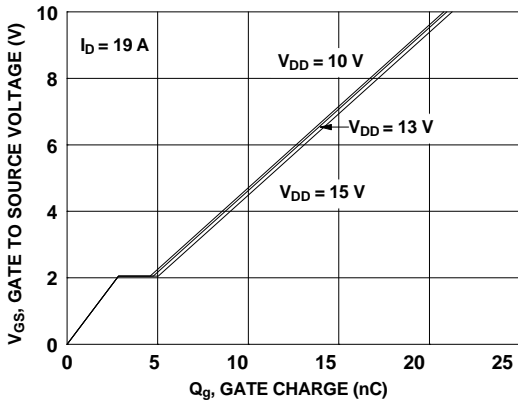


Figure 7. Gate Charge Characteristics

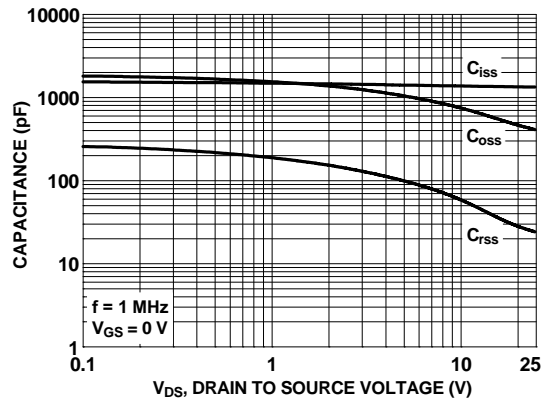


Figure 8. Capacitance vs. Drain to Source Voltage

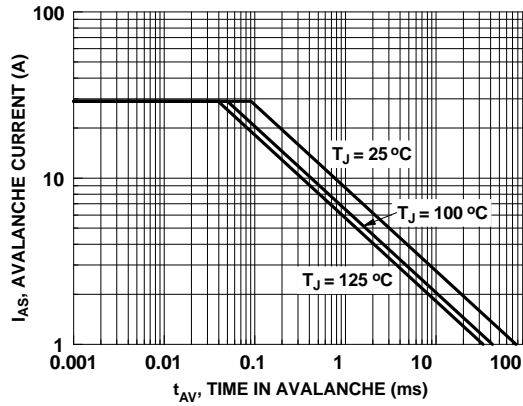


Figure 9. Unclamped Inductive Switching Capability

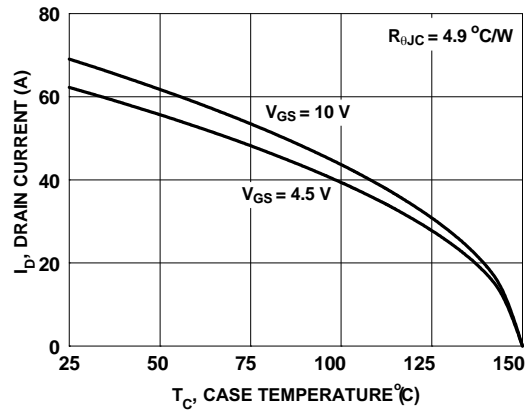


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

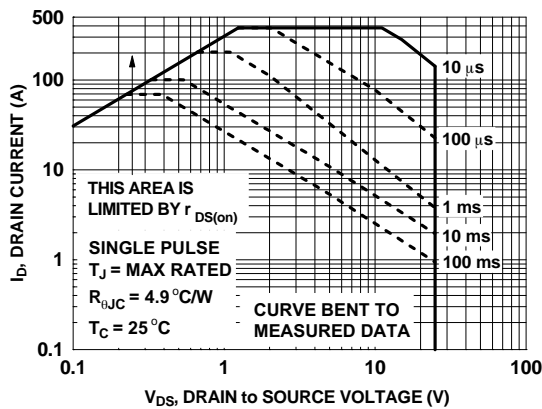


Figure 11. Forward Bias Safe Operating Area

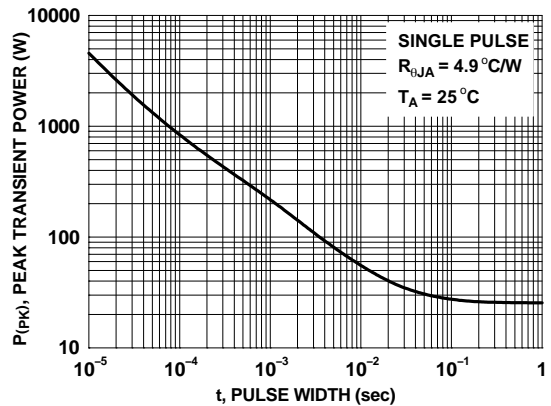


Figure 12. Single Pulse Maximum Power Dissipation

# FDMS001N025DSD

TYPICAL CHARACTERISTICS (Q1 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

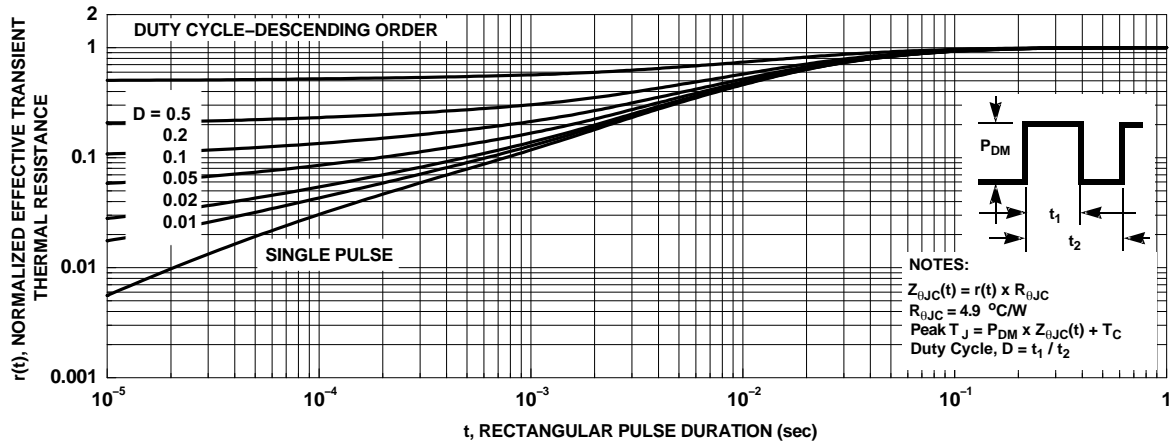


Figure 13. Junction-to-Case Transient Thermal Response Curve

TYPICAL CHARACTERISTICS (Q2 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

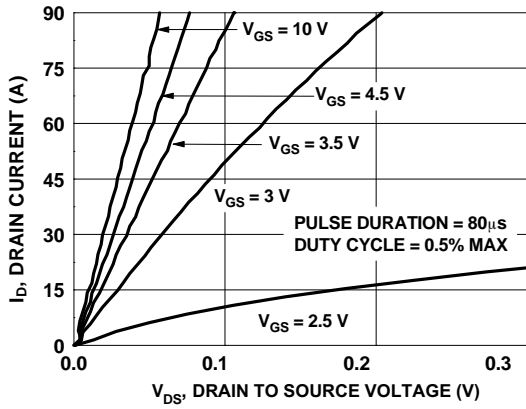


Figure 14. On Region Characteristics

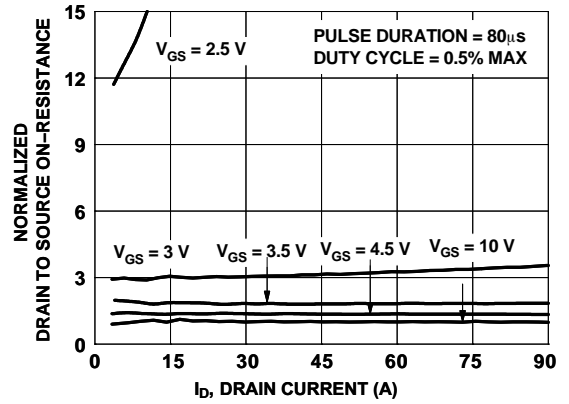


Figure 15. Normalized On-Resistance vs. Drain Current and Gate Voltage

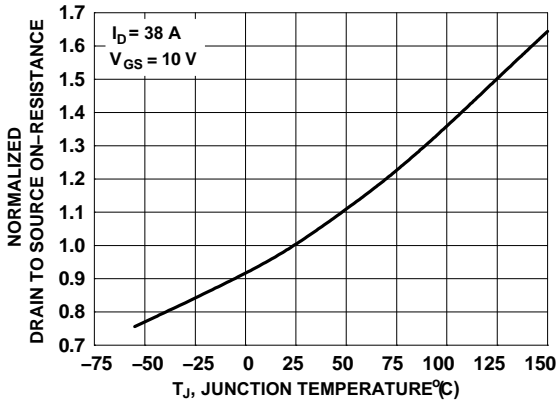


Figure 16. Normalized On Resistance vs. Junction Temperature

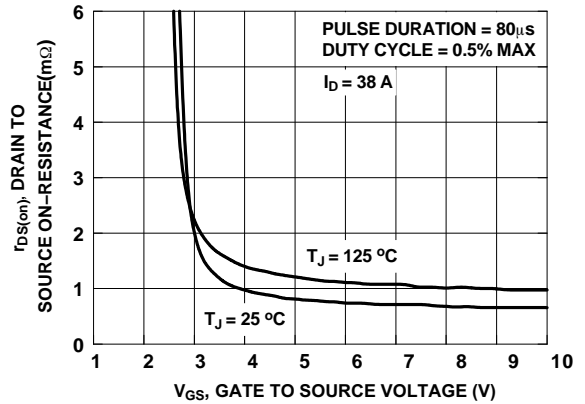


Figure 17. On-Resistance vs. Gate to Source Voltage

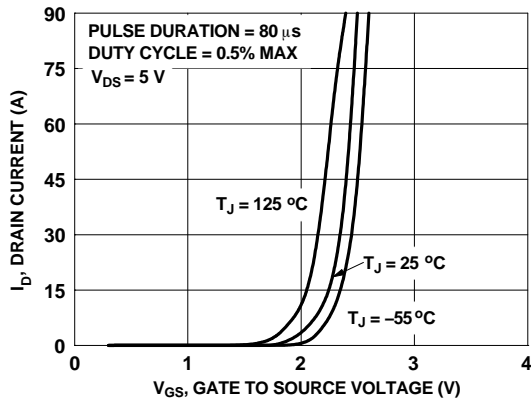


Figure 18. Transfer Characteristics

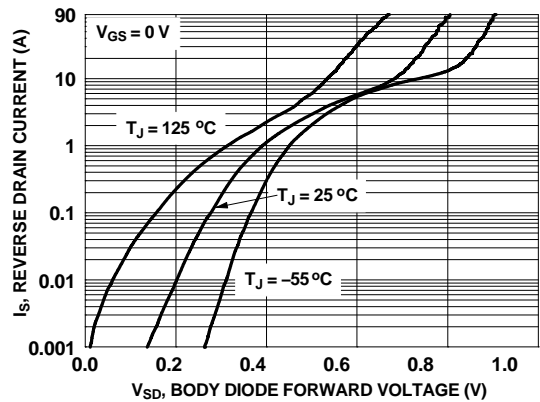


Figure 19. Source to Drain Diode Forward Voltage vs. Source Current



# FDMS001N025DSD

## TYPICAL CHARACTERISTICS (Q2 N-Channel) $T_J = 25^\circ\text{C}$ unless otherwise noted

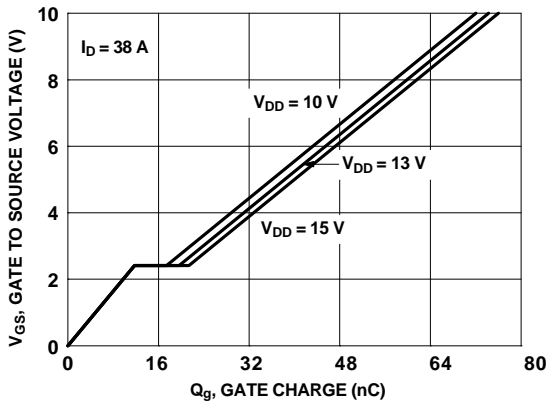


Figure 20. Gate Charge Characteristics

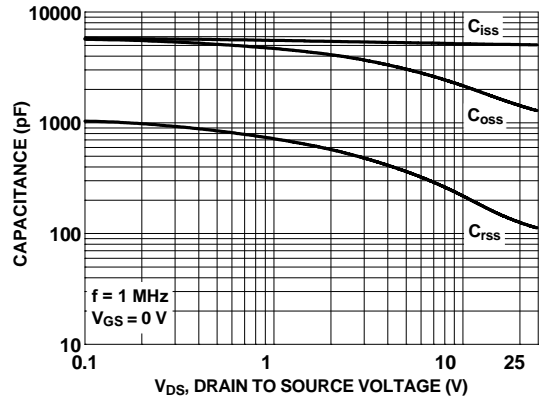


Figure 21. Capacitance vs. Drain to Source Voltage

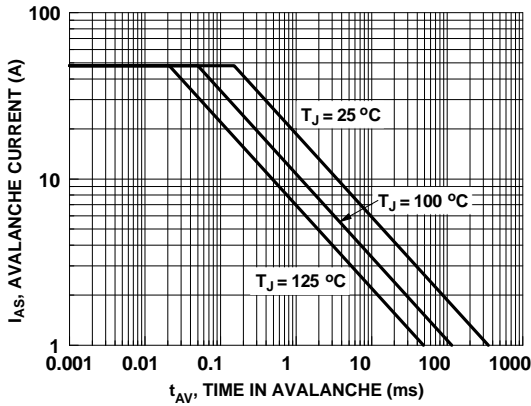


Figure 22. Unclamped Inductive Switching Capability

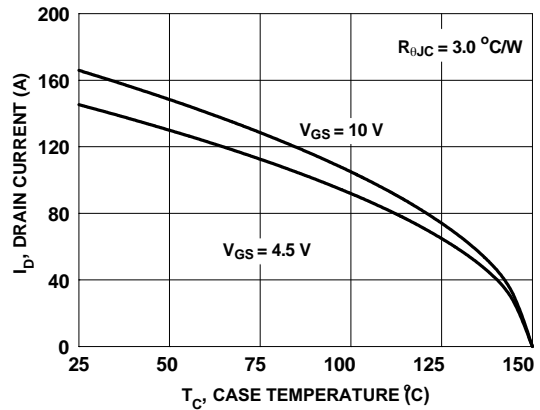


Figure 23. Maximum Continuous Drain Current vs. Case Temperature

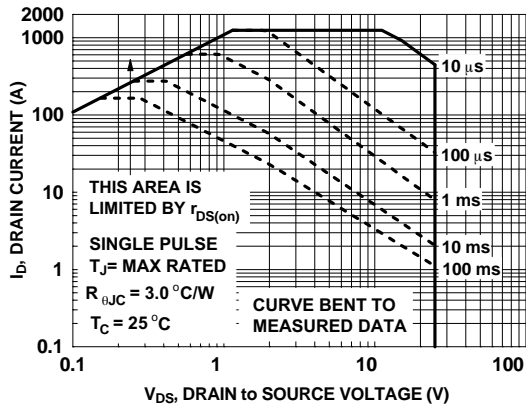


Figure 24. Forward Bias Safe Operating Area

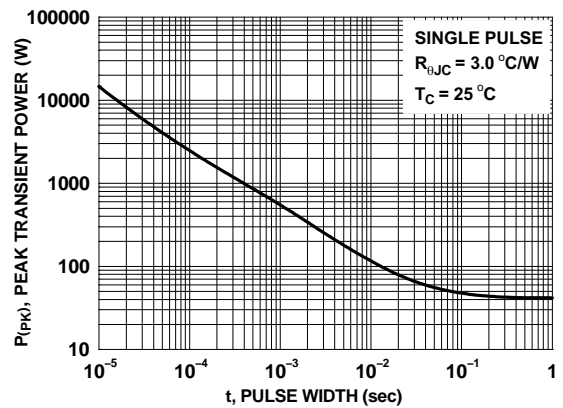


Figure 25. Single Pulse Maximum Power Dissipation

# FDMS001N025DSD

TYPICAL CHARACTERISTICS (Q2 N-Channel)  $T_J = 25^\circ\text{C}$  unless otherwise noted

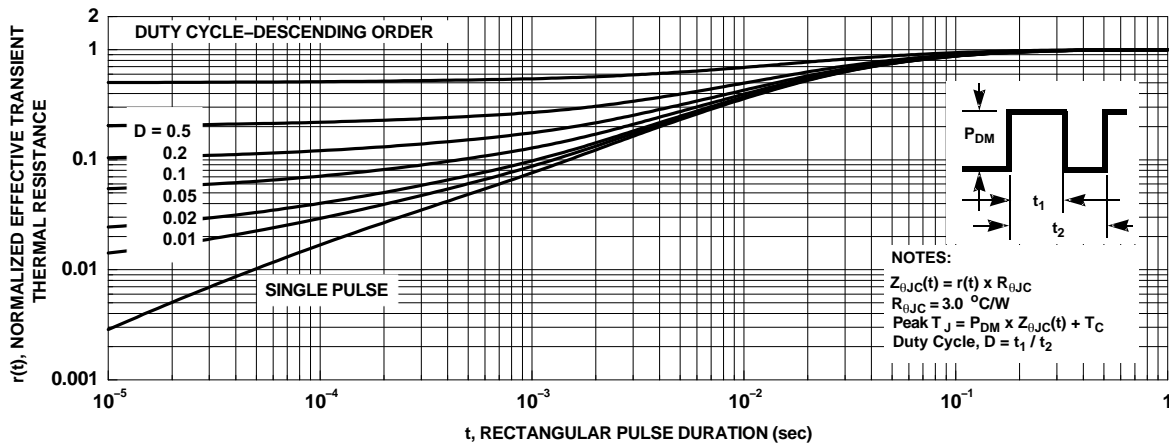


Figure 26. Junction-to-Case Transient Thermal Response Curve

# FDMS001N025DSD

## TYPICAL CHARACTERISTICS (continued)

ON Semiconductor's SyncFET process embeds a Schottky diode in parallel with PowerTrench MOSFET. This diode exhibits similar characteristics to a discrete external Schottky diode in parallel with a MOSFET. Figure 27 shows the reverse recovery characteristic of the FDMS001N025DSD.

Schottky barrier diodes exhibit significant leakage at high temperature and high reverse voltage. This will increase the power in the device.

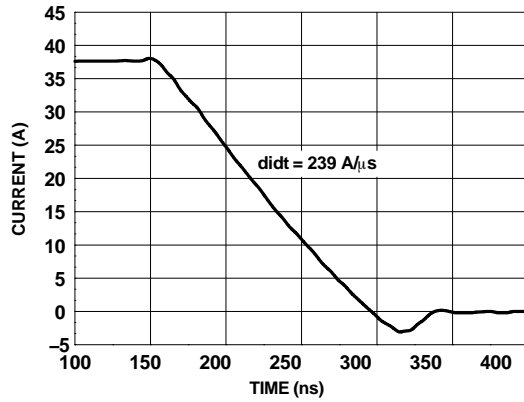


Figure 27. FDMS001N025DSD SyncFET Body Diode Reverse Recovery Characteristic

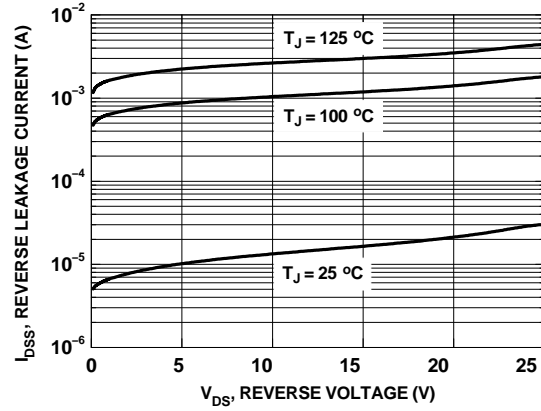
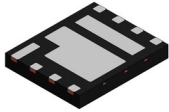


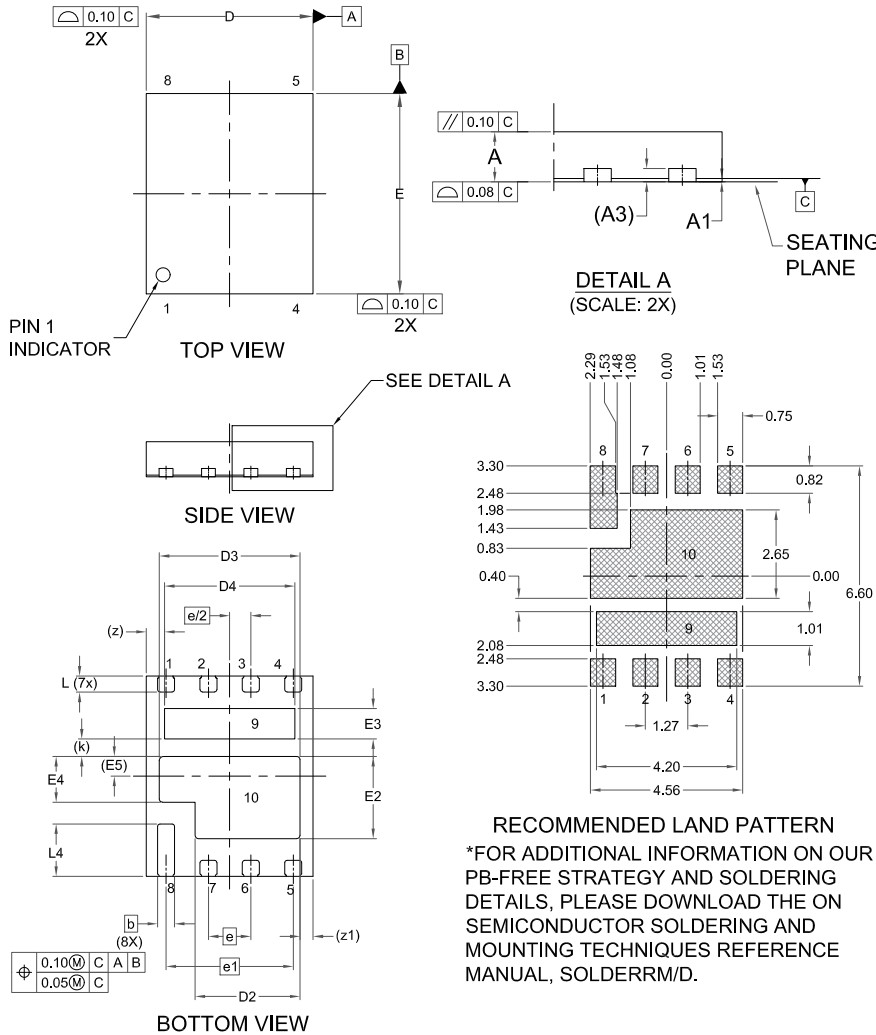
Figure 28. SyncFET Body Diode Reverse Leakage vs. Drain-Source Voltage

# MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



**PQFN8 5.00x6.00x0.75, 1.27P**  
**CASE 483AR**  
**ISSUE D**

DATE 06 NOV 2023



NOTES: UNLESS OTHERWISE SPECIFIED

- A) DOES NOT FULLY CONFORM TO JEDEC REGISTRATION, MO-229, DATED 11/2001.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.70	0.75	0.80
A1	0.00	-	0.05
A3	0.20 REF		
b	0.51 BSC		
D	4.90	5.00	5.10
D2	3.05	3.15	3.25
D3	4.12	4.22	4.32
D4	3.80	3.90	4.00
E	5.90	6.00	6.10
E2	2.36	2.46	2.56
E3	0.81	0.91	1.01
E4	1.27	1.37	1.47
E5	0.59 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
k	0.52 REF		
L	0.38	0.48	0.58
L4	1.47	1.57	1.67
z	0.55 REF		
z1	0.39 REF		

**RECOMMENDED LAND PATTERN**  
\*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

<b>DOCUMENT NUMBER:</b>	<b>98AON13666G</b>	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
<b>DESCRIPTION:</b>	<b>PQFN8 5.00x6.00x0.75, 1.27P</b>	<b>PAGE 1 OF 1</b>

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

**onsemi**, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at [www.onsemi.com/site/pdf/Patent-Marking.pdf](http://www.onsemi.com/site/pdf/Patent-Marking.pdf). **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

---

## ADDITIONAL INFORMATION

### TECHNICAL PUBLICATIONS:

Technical Library: [www.onsemi.com/design/resources/technical-documentation](http://www.onsemi.com/design/resources/technical-documentation)  
onsemi Website: [www.onsemi.com](http://www.onsemi.com)

### ONLINE SUPPORT: [www.onsemi.com/support](http://www.onsemi.com/support)

For additional information, please contact your local Sales Representative at [www.onsemi.com/support/sales](http://www.onsemi.com/support/sales)