

# MOSFET – N-Channel, UltraFET Trench

**250 V, 14 A, 122 mΩ**

## FDMS2734

### General Description

UltraFET devices combine characteristics that enable benchmark efficiency in power conversion applications. Optimized for  $R_{DS(on)}$ , low ESR, low total and Miller gate charge, these devices are ideal for high frequency DC to DC converters.

### Features

- Max  $R_{DS(on)}$  = 122 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 2.8\text{ A}$
- Max  $R_{DS(on)}$  = 130 mΩ at  $V_{GS} = 6\text{ V}$ ,  $I_D = 1.7\text{ A}$
- Low Miller Charge
- Optimized Efficiency at High Frequencies
- Pb-Free, Halide Free and RoHS Compliant

### Applications

- DC – DC Conversion

### MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

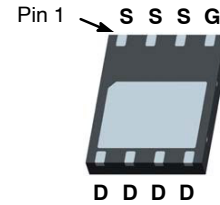
Symbol	Parameter	Value	Unit
$V_{DS}$	Drain to Source Voltage	250	V
$V_{GS}$	Gate to Source Voltage	±20	V
$I_D$	Drain Current: – Continuous (Silicon limited) $T_C = 25^\circ\text{C}$ – Continuous $T_A = 25^\circ\text{C}$ (Note 1a) – Pulsed	14 2.8 30	A
$P_D$	Power Dissipation: $T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	78 2.5	W
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.6	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

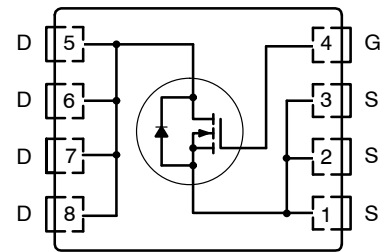
$V_{DS}$	$R_{DS(on)}$ MAX	$I_D$ MAX
250 V	122 mΩ @ 10 V	14 A
	130 mΩ @ 6 V	



Bottom View

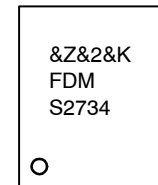
WDFN8 5×6, 1.27P  
(Power 56)  
CASE 506DP

### ELECTRICAL CONNECTION



N-CHANNEL MOSFET

### MARKING DIAGRAM



- &Z = Assembly Plant Code
- &2 = 2-Digit Date Code (Year and Week)
- &K = 2-Digit Lot Run Code
- FDMS2734 = Specific Device Code

### ORDERING INFORMATION

Device	Package	Shipping†
FDMS2734	WDFN8 5×6, 1.27P (Power 56) (Pb-Free, Halide Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, [BRD8011/D](#).

# FDMS2734

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
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### OFF CHARACTERISTICS

BV <sub>DSS</sub>	Drain to Source Breakdown Voltage	I <sub>D</sub> = 250 μA, V <sub>GS</sub> = 0 V	250	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	250	–	mV/°C
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	V <sub>DS</sub> = 200 V	–	–	1	μA
I <sub>GSS</sub>	Gate to Source Leakage Current	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V	–	–	±100	nA

### ON CHARACTERISTICS (Note 2)

V <sub>GS(th)</sub>	Gate to Source Threshold Voltage	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250 μA	2	3	4	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I <sub>D</sub> = 250 μA, Referenced to 25°C	–	–11	–	mV/°C
R <sub>DS(on)</sub>	Static Drain to Source On Resistance	V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.8 A	–	105	122	mΩ
		V <sub>GS</sub> = 6 V, I <sub>D</sub> = 1.7 A	–	110	130	
		V <sub>GS</sub> = 10 V, I <sub>D</sub> = 2.8 A, T <sub>J</sub> = 125°C	–	217	258	
g <sub>FS</sub>	Forward Transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 2.8 A	–	11	–	S

### DYNAMIC CHARACTERISTICS

C <sub>iss</sub>	Input Capacitance	V <sub>DS</sub> = 100 V, V <sub>GS</sub> = 0 V, f = 1 MHz	–	1775	2365	pF
C <sub>oss</sub>	Output Capacitance		–	80	110	pF
C <sub>rss</sub>	Reverse Transfer Capacitance		–	25	40	pF
R <sub>g</sub>	Gate Resistance	f = 1 MHz	–	0.9	–	Ω

### SWITCHING CHARACTERISTICS

t <sub>d(on)</sub>	Turn-On Delay Time	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 2.8 A, V <sub>GS</sub> = 10 V, R <sub>GEN</sub> = 6 Ω	–	22	36	ns
t <sub>r</sub>	Rise Time		–	10	20	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		–	36	58	ns
t <sub>f</sub>	Fall Time		–	12	22	ns
Q <sub>g(TOT)</sub>	Total Gate Charge at 10 V	V <sub>GS</sub> = 0 V to 10 V, V <sub>DD</sub> = 125 V, I <sub>D</sub> = 2.8 A	–	30	42	nC
Q <sub>gs</sub>	Gate to Source Gate Charge	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 2.8 A	–	7	–	nC
Q <sub>gd</sub>	Gate to Drain “Miller” Charge	V <sub>DD</sub> = 125 V, I <sub>D</sub> = 2.8 A	–	9	–	nC

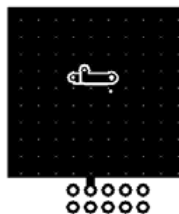
### DRAIN-SOURCE DIODE CHARACTERISTICS

V <sub>SD</sub>	Source to Drain Diode Forward Voltage	V <sub>GS</sub> = 0 V, I <sub>S</sub> = 2.8 A (Note 2)	–	0.75	1.20	V
t <sub>rr</sub>	Reverse Recovery Time	I <sub>F</sub> = 2.8 A, di/dt = 100 A/μs	–	79	119	ns
Q <sub>rr</sub>	Reverse Recovery Charge		–	214	321	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

#### NOTES:

- R<sub>θJA</sub> is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. R<sub>θJC</sub> is guaranteed by design while R<sub>θCA</sub> is determined by the user's board design.



a) 50°C/W when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b) 125°C/W when mounted on a minimum pad of 2 oz copper.

- Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.

TYPICAL CHARACTERISTICS

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

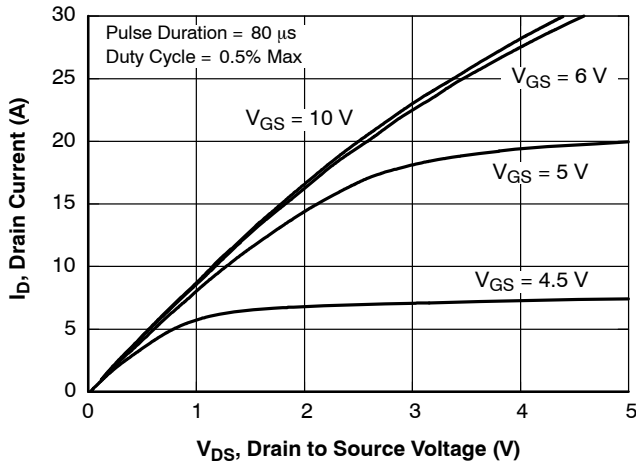


Figure 1. On Region Characteristics

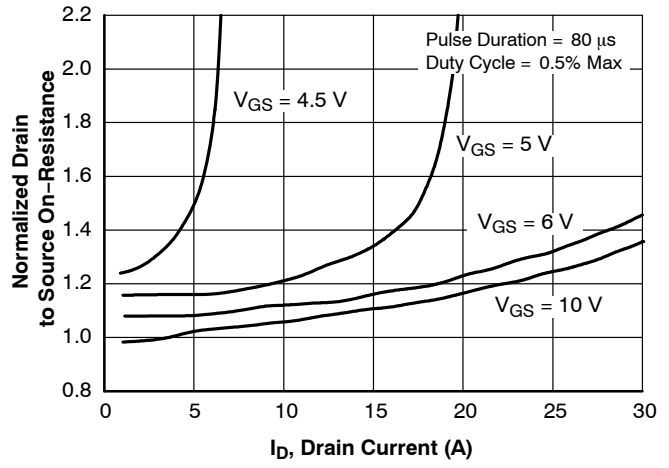


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

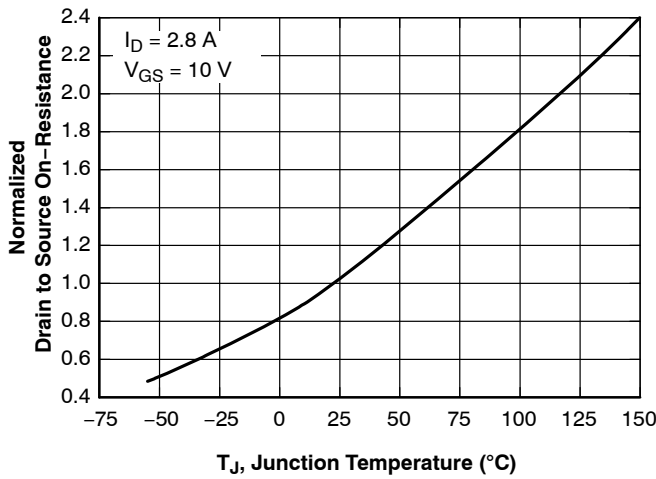


Figure 3. Normalized On Resistance vs. Junction Temperature

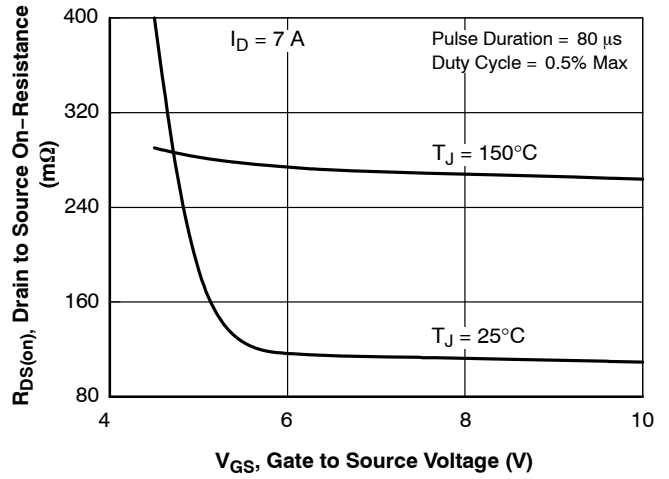


Figure 4. On-Resistance vs. Gate to Source Voltage

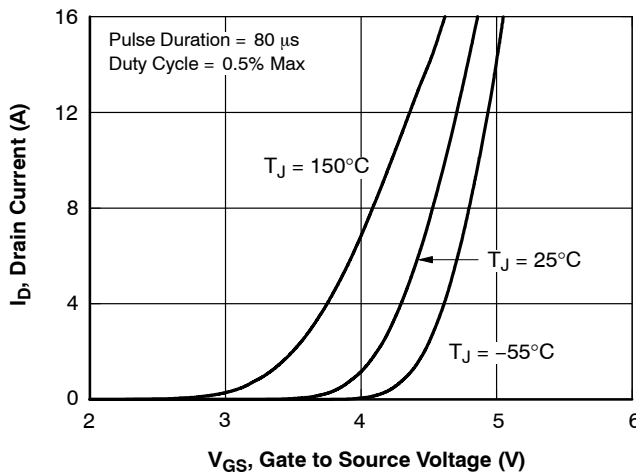


Figure 5. Transfer Characteristics

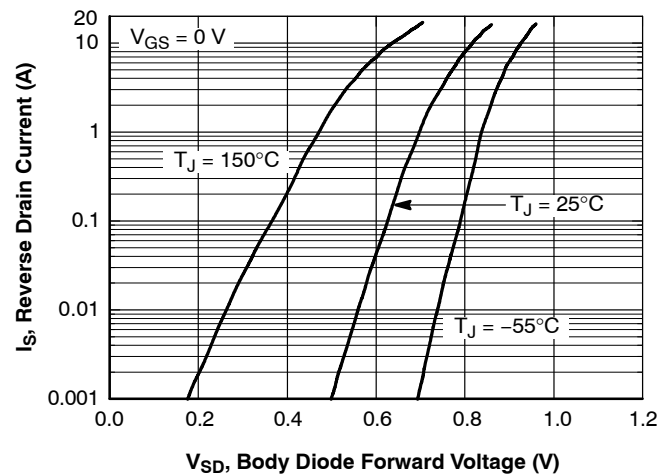


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

TYPICAL CHARACTERISTICS (continued)

(T<sub>J</sub> = 25°C unless otherwise noted)

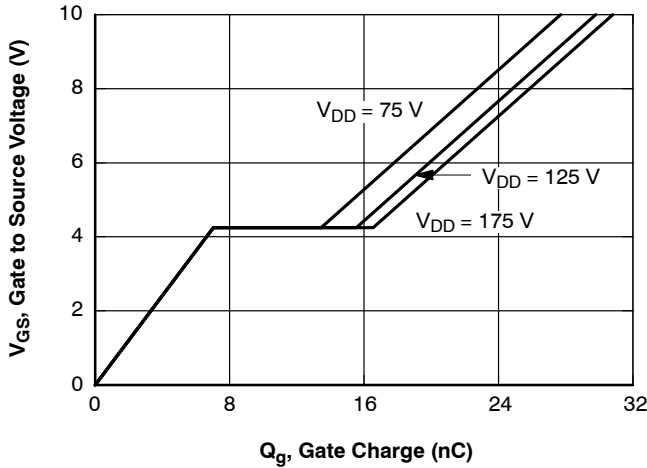


Figure 7. Gate Charge Characteristics

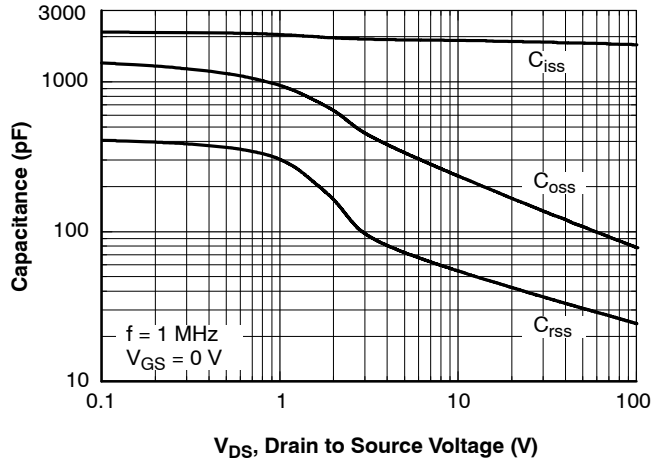


Figure 8. Capacitance vs. Drain to Source Voltage

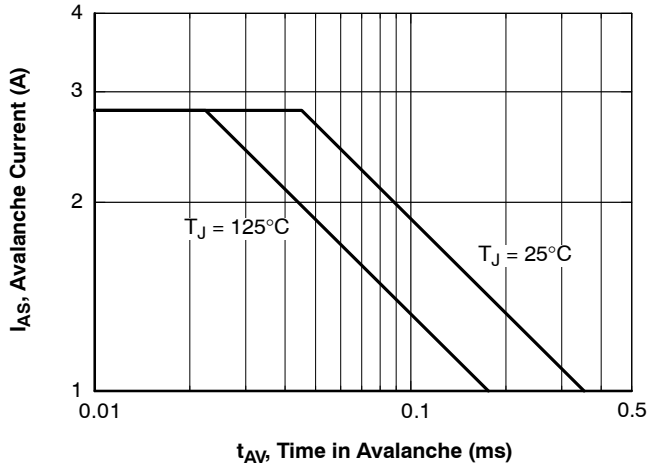


Figure 9. Unclamped Inductive Switching Capability

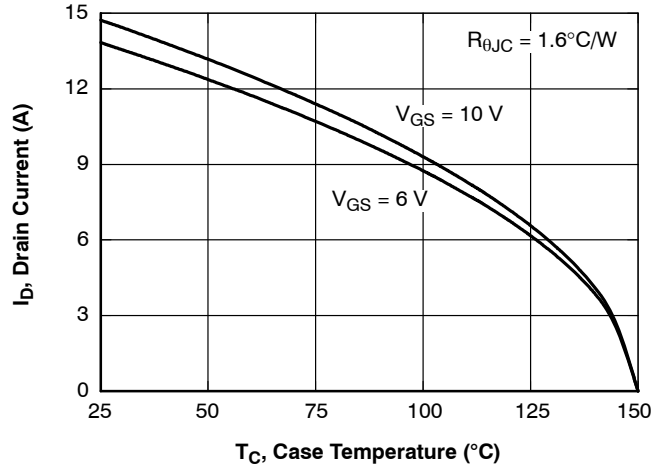


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

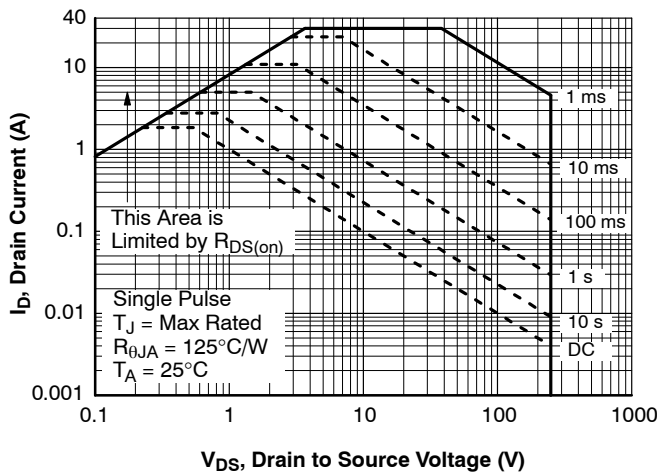


Figure 11. Forward Bias Safe Operating Area

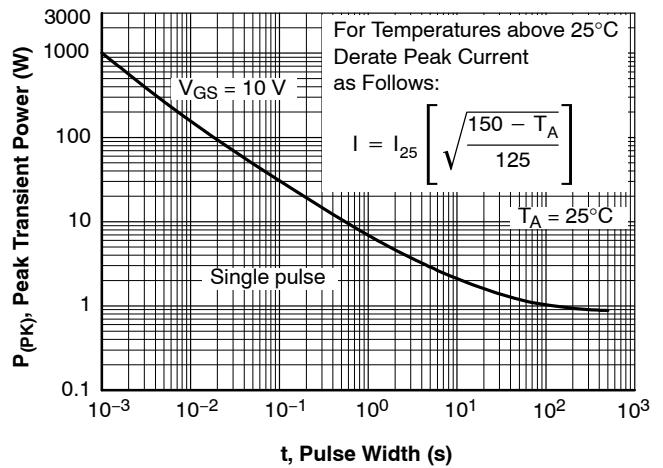


Figure 12. Single Pulse Maximum Power Dissipation

TYPICAL CHARACTERISTICS (continued)

( $T_J = 25^\circ\text{C}$  unless otherwise noted)

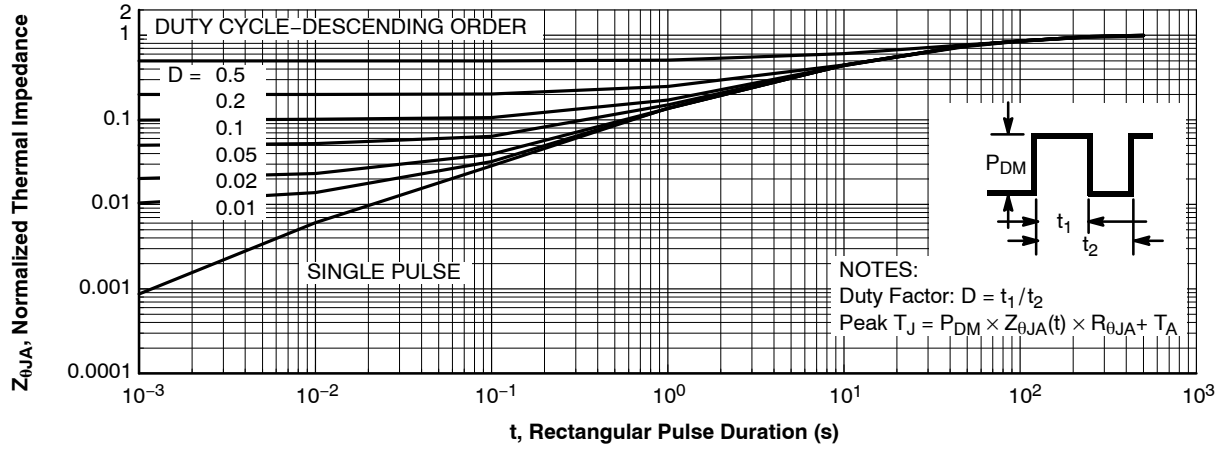


Figure 13. Transient Thermal Response Curve

# MECHANICAL CASE OUTLINE

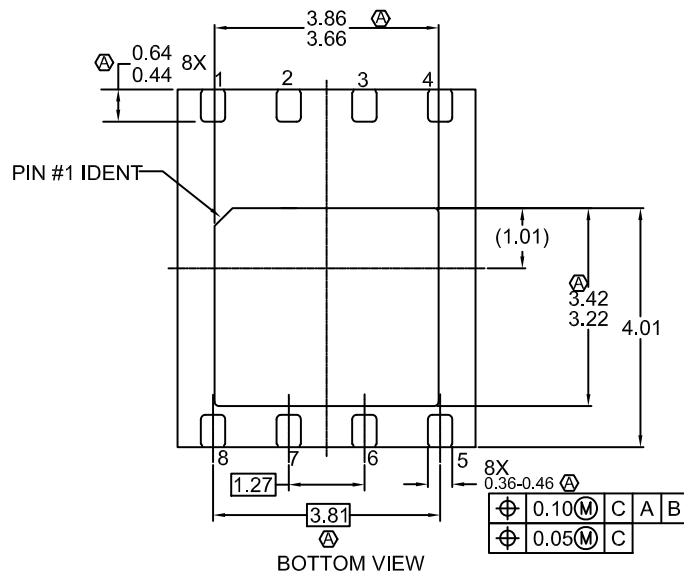
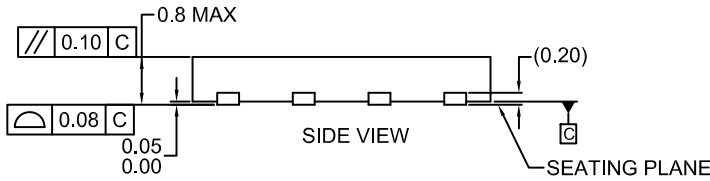
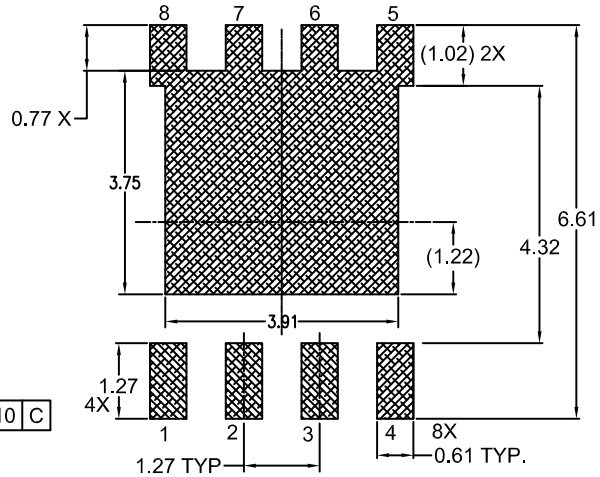
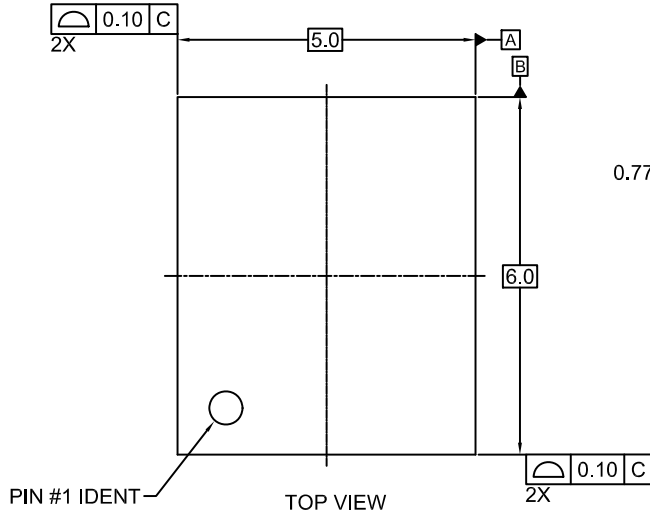
## PACKAGE DIMENSIONS

ON Semiconductor®



**WDFN8 5x6, 1.27P**  
CASE 506DP  
ISSUE O

DATE 31 AUG 2016



**NOTES:**

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