

MOSFET - Dual, N-Channel, Shielded Gate, POWER trench®

80 V, 166 A, 2.7 mΩ

FDMS2D5N08C

Description

This N-Channel MV MOSFET is Produced using onsemi's Advanced POWER trench Process that Incorporates Shielded Gate technology. This process has been optimized to minimise on-state resistance and yet maintain superior switching performance with best in class soft body diode.

Features

- Shielded Gate MOSFET Technology
- Max $R_{DS(on)}$ = 2.7 mΩ at V_{GS} = 10 V, I_D = 68 A
- Max $R_{DS(on)}$ = 6.7 mΩ at V_{GS} = 6 V, I_D = 34 A
- 50% Lower Q_{rr} than Other MOSFET Suppliers
- Lowers Switching Noise/EMI
- MSL1 Robust Package Design
- 100% UIL Tested
- These Device is Pb-Free and RoHS Compliant

Typical Applications

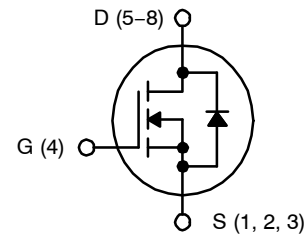
- Primary DC-DC MOSFET
- Synchronous Rectifier in DC-DC and AC-DC
- Motor Drive
- Solar

ABSOLUTE MAXIMUM RATINGS T_A = 25 °C unless otherwise noted

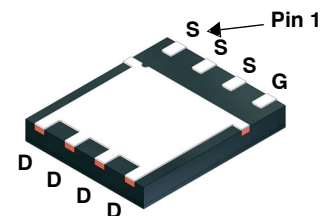
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	80	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current – Continuous T_C = 25 °C (Note 5) – Continuous T_C = 100 °C (Note 5) – Continuous T_A = 25 °C (Note 1a) – Pulsed (Note 4)	166 105 24 823	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)	600	mJ
P_D	Power Dissipation T_A = 25 °C Power Dissipation T_A = 25 °C (Note 1a)	138 2.7	W
T_J, T_{stg}	Operating and Storage Junction Temperature Range	–55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

$V_{(BR)DSS}$	$R_{DS(on)}$ MAX	I_D MAX
80 V	2.7 mΩ @ 10 V	166 A

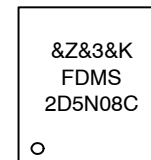


N-CHANNEL MOSFET



PQFN8 5X6, 1.27P
CASE 483AF

MARKING DIAGRAM



&Z = Assembly Plant Code
&3 = Numeric Date Code
&K = 2-Digit Lot Code
FDMS2D5N08C = Specific Device Code

ORDERING INFORMATION

Device	Package	Shipping†
FDMS2D5N08C	PQFN-8 (Pb-Free)	3000 / Tape & Reel

† For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	0.9	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	45	

ELECTRICAL CHARACTERISTICS $T_J = 25\text{ }^{\circ}\text{C}$ unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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Off Characteristics

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$, $V_{GS} = 0\text{ V}$	80	–	–	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$, Referenced to $25\text{ }^{\circ}\text{C}$	–	62	–	mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 64\text{ V}$, $V_{GS} = 0\text{ V}$	–	–	1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20\text{ V}$, $V_{DS} = 0\text{ V}$	–	–	100	nA

On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 380\text{ }\mu\text{A}$	2.0	2.9	4.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 380\text{ }\mu\text{A}$, Referenced to $25\text{ }^{\circ}\text{C}$	–	–8.3	–	mV/°C
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}$, $I_D = 68\text{ A}$ $V_{GS} = 6\text{ V}$, $I_D = 34\text{ A}$, $V_{GS} = 10\text{ V}$, $I_D = 68\text{ A}$, $T_J = 125\text{ }^{\circ}\text{C}$	–	2.2 3.3 3.7	2.7 6.7 4.7	m Ω
g_{FS}	Forward Transconductance	$V_{DS} = 5\text{ V}$, $I_D = 68\text{ A}$	–	148	–	S

Dynamic Characteristics

C_{iss}	Input Capacitance	$V_{DS} = 40\text{ V}$, $V_{GS} = 0\text{ V}$, $f = 1\text{ MHz}$	–	4455	6240	pF
C_{oss}	Output Capacitance		–	1480	2070	pF
C_{rss}	Reverse Transfer Capacitance		–	59	85	pF
R_g	Gate Resistance	–	–	0.8	1.6	Ω

Switching Characteristics

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 40\text{ V}$, $I_D = 68\text{ A}$, $V_{GS} = 10\text{ V}$, $R_{GEN} = 6\text{ }\Omega$	–	21	34	ns
t_r	Rise Time		–	11	20	ns
$t_{d(off)}$	Turn-Off Delay Time		–	29	47	ns
t_f	Fall Time		–	7	13	ns
Q_g	Total Gate Charge	$V_{GS} = 0\text{ V to }10\text{ V}$, $V_{DD} = 40\text{ V}$, $I_D = 68\text{ A}$	–	60	84	nC
		$V_{GS} = 0\text{ V to }10\text{ V}$, $V_{DD} = 40\text{ V}$, $I_D = 68\text{ A}$	–	38	54	nC
Q_{gs}	Gate to Source Gate Charge	$V_{DD} = 40\text{ V}$, $I_D = 68\text{ A}$	–	19	–	nC
Q_{gd}	Gate to Drain “Miller” Charge		–	12	–	nC
Q_{OSS}	Output Charge	$V_{DD} = 40\text{ V}$, $V_{GS} = 0\text{ V}$	–	84	–	nC
Q_{SYNC}	Total Gate Charge Sync	$V_{DD} = 0\text{ V}$, $I_D = 68\text{ A}$	–	51	–	nC

Drain-Source Diode Characteristics and Maximum Ratings

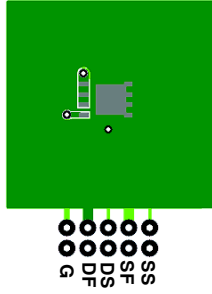
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 2.2\text{ A}$ (Note 2)	–	0.7	1.2	V
		$V_{GS} = 0\text{ V}$, $I_S = 68\text{ A}$ (Note 2)	–	0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 34\text{ A}$, $di/dt = 300\text{ A}/\mu\text{s}$	–	30	48	ns
Q_{rr}	Reverse Recovery Charge		–	55	88	nC
t_{rr}	Reverse Recovery Time	$I_F = 34\text{ A}$, $di/dt = 1000\text{ A}/\mu\text{s}$	–	24	39	ns
Q_{rr}	Reverse Recovery Charge		–	139	222	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

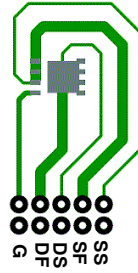
FDMS2D5N08C

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² oz. copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.



a) 45 °C/W when mounted on a 1 in² pad of 2 oz copper.



b) 115 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width $\leq 300 \mu s$, Duty Cycle $\leq 2.0\%$.
3. E_{AS} of 600 mJ is based on starting $T_J = 125^\circ C$; N-ch: $L = 3 mH$, $I_{AS} = 20 A$, $V_{DD} = 80 V$, $V_{GS} = 10 V$. 100% test at $L = 0.1 mH$, $I_{AS} = 63 A$.
4. Pulsed I_d please refer to Figure 11 SOA graph for more details.
5. Computed continuous current limited to Max Junction Temperature only, actual continuous current will be limited by thermal & electro-mechanical application board design.

TYPICAL CHARACTERISTICS

Tc = 25 °C unless otherwise noted

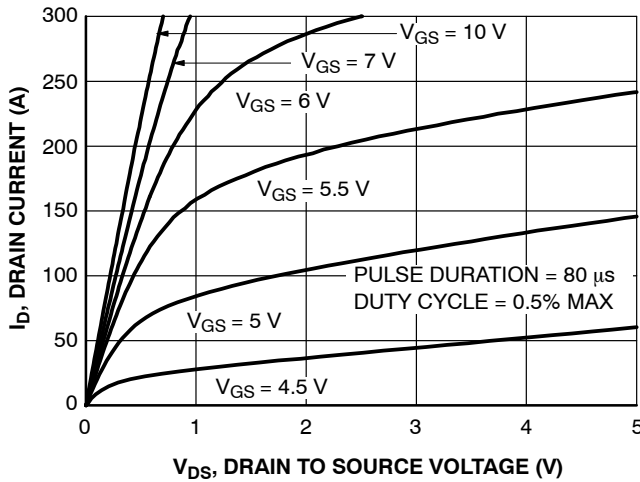


Figure 1. On-Region Characteristics

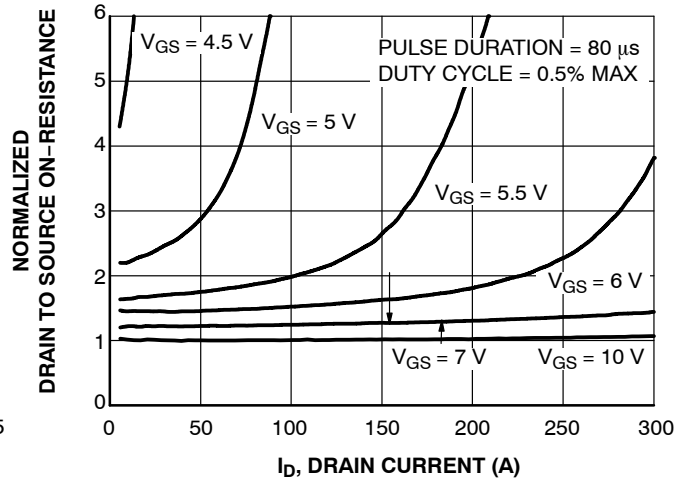


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

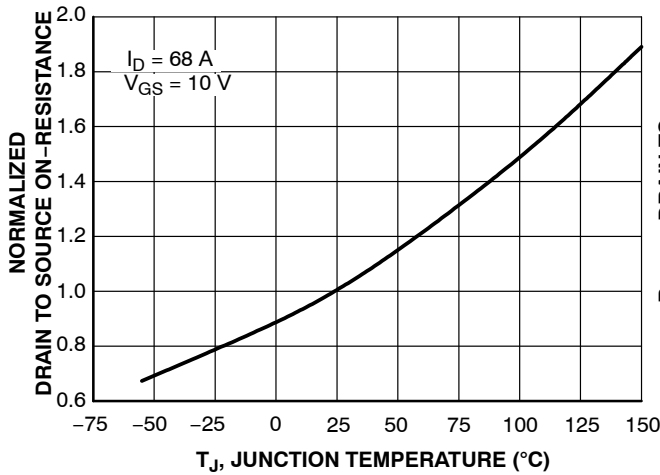


Figure 3. Normalized On-Resistance vs Junction Temperature

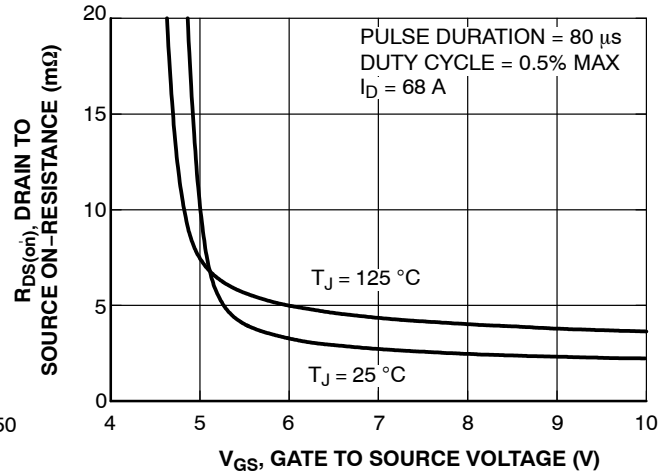


Figure 4. On-Resistance vs Gate to Source Voltage

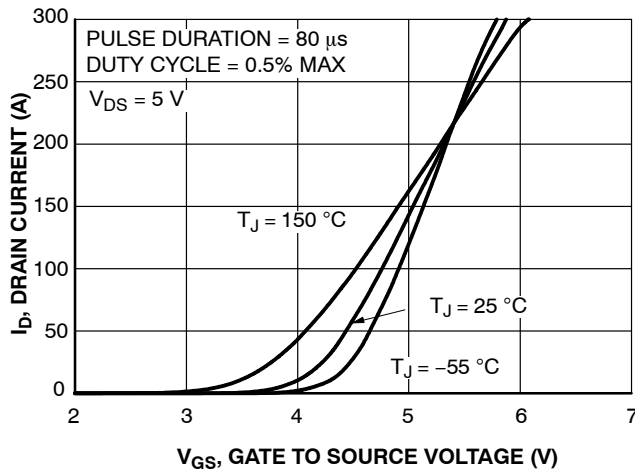


Figure 5. Transfer Characteristics

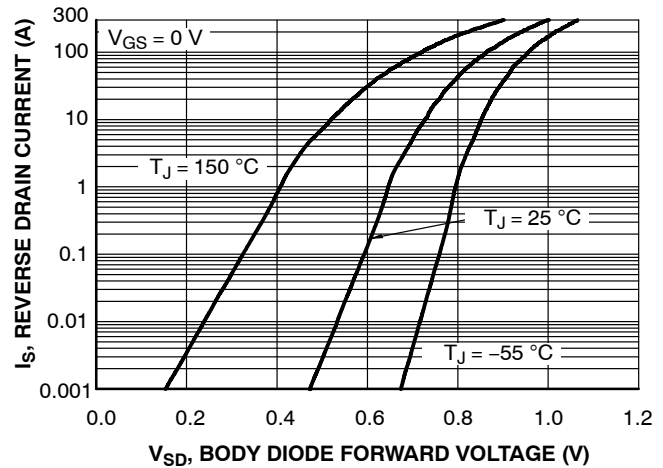


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

TYPICAL CHARACTERISTICS (CONTINUED)

$T_c = 25^\circ\text{C}$ unless otherwise noted

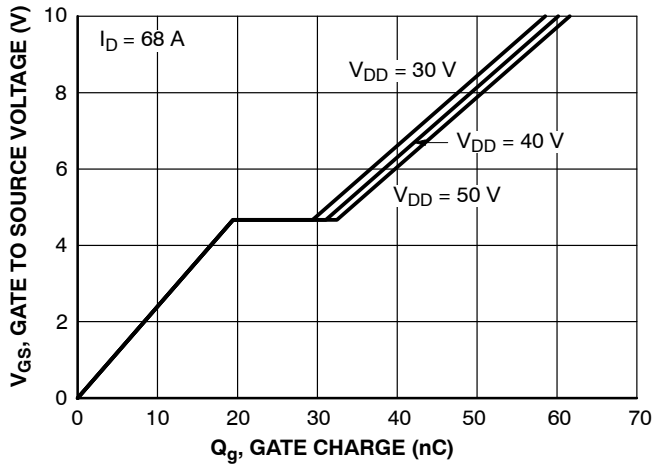


Figure 7. Gate Charge Characteristics

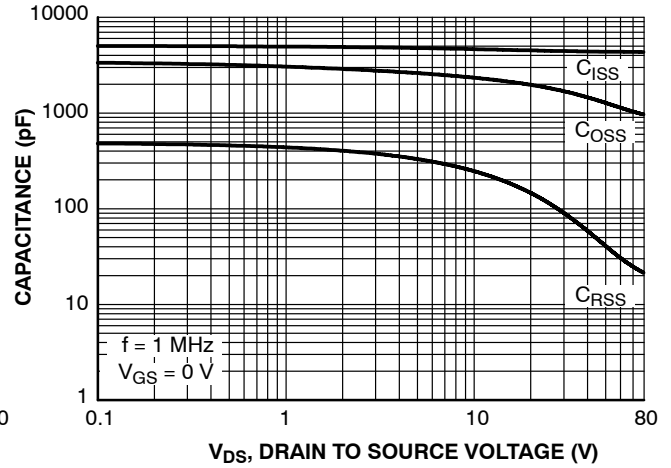


Figure 8. Capacitance vs Drain to Source Voltage

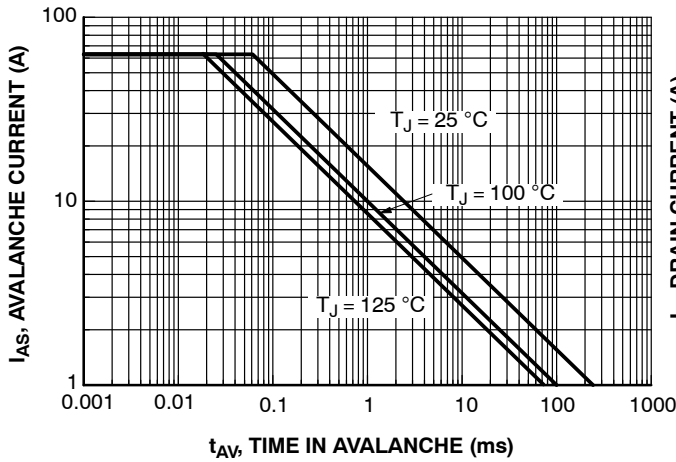


Figure 9. Unclamped Inductive Switching Capability

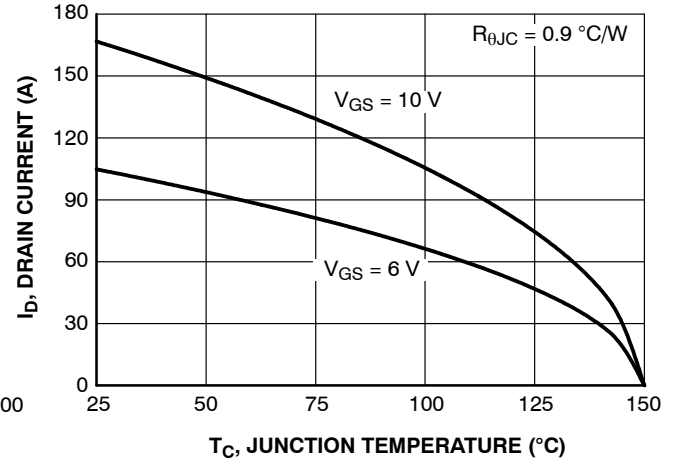


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

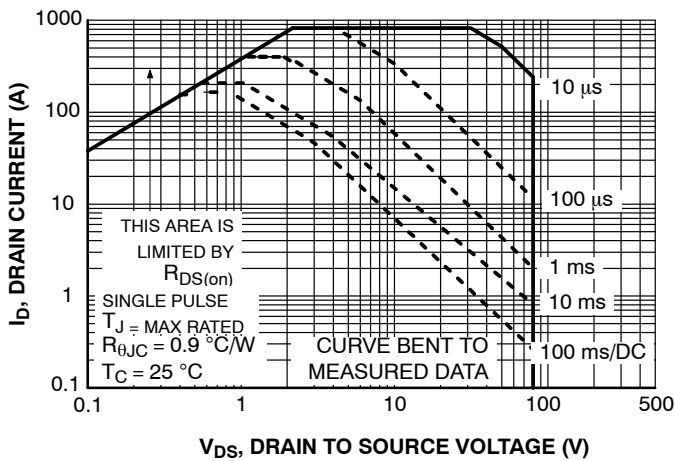


Figure 11. Forward Bias Safe Operating Area

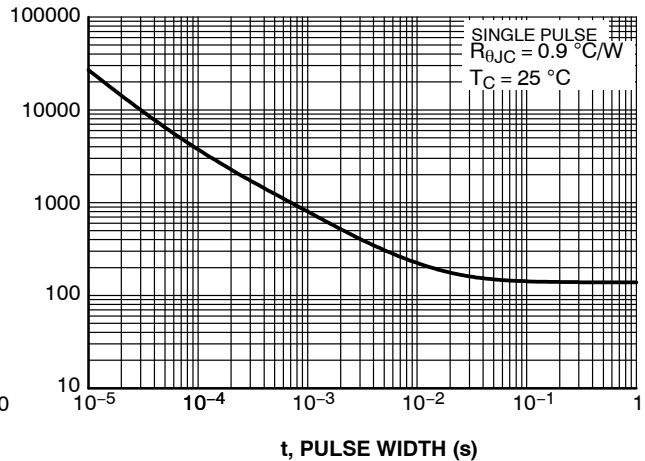
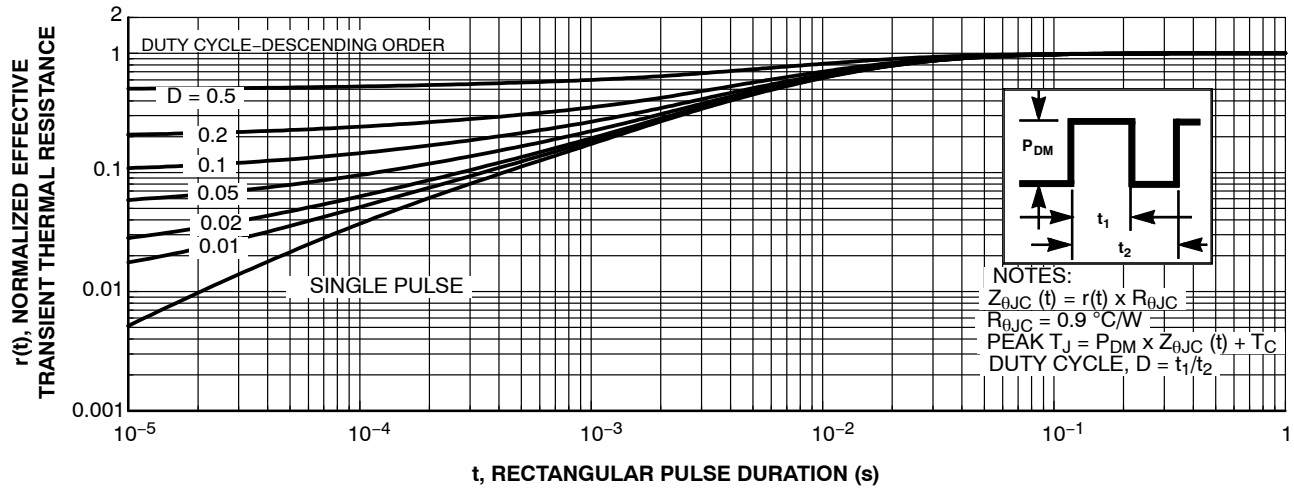


Figure 12. Single Pulse Maximum Power Dissipation

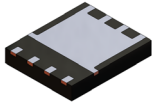
TYPICAL CHARACTERISTICS (CONTINUED)

T_c = 25 °C unless otherwise noted

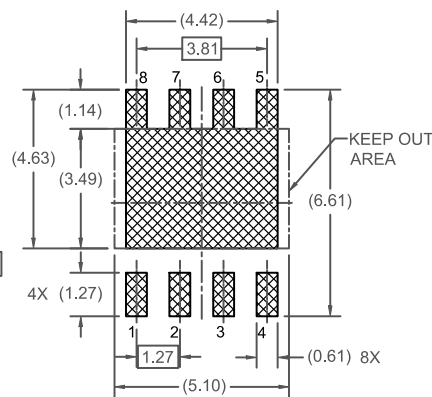
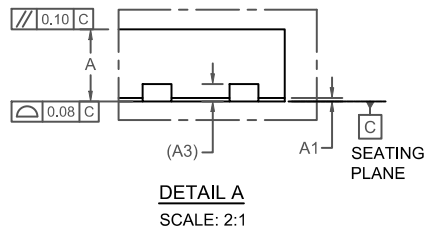
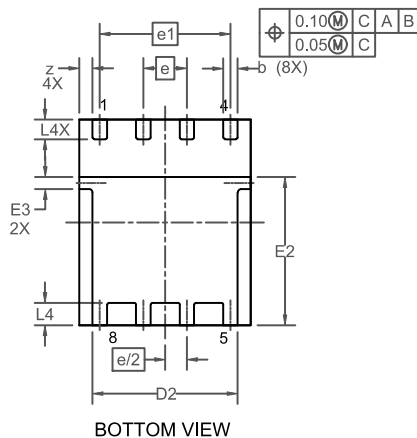
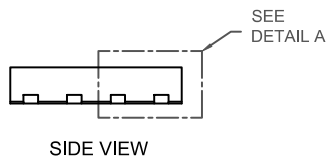
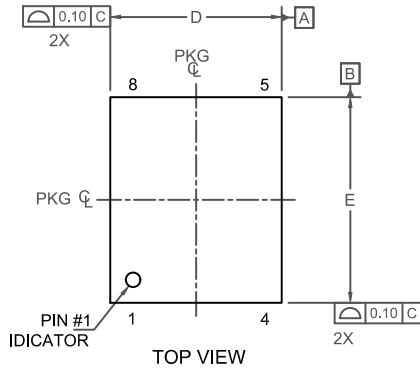
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REVISION HISTORY

Revision	Description of Changes	Date
Ex-FCS	Preview Datasheet (or Advanced datasheet) Rev A published by Fairchild Semiconductor.	7/1/2016
1.0	Final Datasheet Released and Change to ON Semiconductor Brand name logo.	3/1/2017
1.1	By using official ON Semiconductor datasheet format.	5/1/2017
2	Converted the Data Sheet to onsemi format.	8/19/2025


PQFN8 5X6, 1.27P
CASE 483AF
ISSUE A

DATE 06 JUL 2021


LAND PATTERN
RECOMMENDATION

*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERM/D.

NOTES: UNLESS OTHERWISE SPECIFIED

- A) PACKAGE STANDARD REFERENCE:
JEDEC MO-240, ISSUE A, VAR. AA,
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
E) IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
A3	0.20 REF.		
b	0.37	0.42	0.47
D	4.90	5.00	5.10
D2	4.13	4.23	4.33
E	5.90	6.00	6.10
E2	4.23	4.33	4.43
E3	0.35 REF.		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
L	0.52	0.57	0.62
L4	0.55	0.65	0.75
z	0.38 REF		

DOCUMENT NUMBER: 98AON13656G

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