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# FDMS7678

## N-Channel Power Trench<sup>®</sup> MOSFET 30 V, 26 A, 5.5 mΩ

### Features

- Max  $r_{DS(on)}$  = 5.5 mΩ at  $V_{GS} = 10\text{ V}$ ,  $I_D = 17.5\text{ A}$
- Max  $r_{DS(on)}$  = 6.8 mΩ at  $V_{GS} = 4.5\text{ V}$ ,  $I_D = 15\text{ A}$
- High Performance Technology for Extremely Low  $r_{DS(on)}$
- Termination is Lead-Free
- RoHS Compliant

### General Description

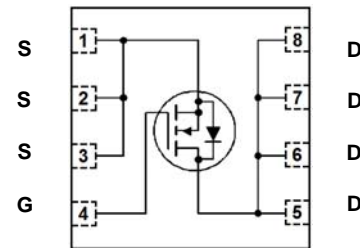
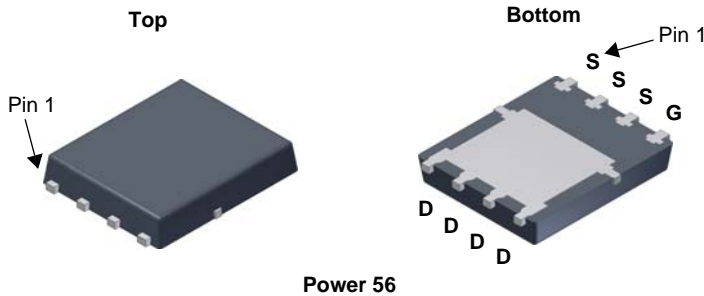
This N-Channel MOSFET is produced using Fairchild Semiconductor's advanced Power Trench<sup>®</sup> process that has been especially tailored to minimize the on-state resistance. This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Applications

- DC - DC Buck Converters
- Notebook Battery Power Management
- Load Switch in Notebook



FDMS7678 N-Channel Power Trench<sup>®</sup> MOSFET



### MOSFET Maximum Ratings $T_A = 25\text{ °C}$ unless otherwise noted.

Symbol	Parameter	Ratings	Units
$V_{DS}$	Drain to Source Voltage	30	V
$V_{GS}$	Gate to Source Voltage (Note 3)	±20	V
$I_D$	Drain Current -Continuous (Package limited) $T_C = 25\text{ °C}$	26	A
	Drain Current -Continuous (Silicon limited) $T_C = 25\text{ °C}$	72	
	-Continuous $T_A = 25\text{ °C}$ (Note 1a)	17.5	
	-Pulsed	70	
$E_{AS}$	Single Pulse Avalanche Energy (Note 4)	54	mJ
$P_D$	Power Dissipation $T_C = 25\text{ °C}$	41	W
	Power Dissipation $T_A = 25\text{ °C}$ (Note 1a)	2.3	
$T_J, T_{STG}$	Operating and Storage Junction Temperature Range	-55 to +150	°C

### Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case	3	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

### Package Marking and Ordering Information

Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS7678	FDMS7678	Power 56	13 "	12 mm	3000 units

## Electrical Characteristics $T_J = 25\text{ }^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Test Conditions	Min.	Typ.	Max.	Units
$BV_{DSS}$	Drain to Source Breakdown Voltage	$I_D = 250\text{ }\mu\text{A}$ , $V_{GS} = 0\text{ V}$	30			V
$BV_{DSS(t)}$	Drain to Source Breakdown Voltage (transient)	$V_{GS} = 0\text{ V}$ , $I_{D(aval)} = 14.2\text{ A}$ , $T_{case} = 25\text{ }^\circ\text{C}$ , $t_{transient} = 10\text{ ns}$	34			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		21		mV/ $^\circ\text{C}$
$I_{DSS}$	Zero Gate Voltage Drain Current	$V_{DS} = 24\text{ V}$ , $V_{GS} = 0\text{ V}$			1	$\mu\text{A}$
$I_{GSS}$	Gate to Source Leakage Current, Forward	$V_{GS} = 20\text{ V}$ , $V_{DS} = 0\text{ V}$			100	nA

### On Characteristics

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$ , $I_D = 250\text{ }\mu\text{A}$	1.2	1.5	3.0	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250\text{ }\mu\text{A}$ , referenced to $25\text{ }^\circ\text{C}$		-5		mV/ $^\circ\text{C}$
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$		4.7	5.5	m $\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 15\text{ A}$		5.6	6.8	
		$V_{GS} = 10\text{ V}$ , $I_D = 17.5\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$		6.3	7.4	
$g_{FS}$	Forward Transconductance	$V_{DD} = 5\text{ V}$ , $I_D = 17.5\text{ A}$		90		S

### Dynamic Characteristics

$C_{iss}$	Input Capacitance	$V_{DS} = 15\text{ V}$ , $V_{GS} = 0\text{ V}$ $f = 1\text{ MHz}$		1810	2410	pF
$C_{oss}$	Output Capacitance			620	820	pF
$C_{riss}$	Reverse Transfer Capacitance			75	110	pF
$R_g$	Gate Resistance		0.1	0.7	2.5	$\Omega$

### Switching Characteristics

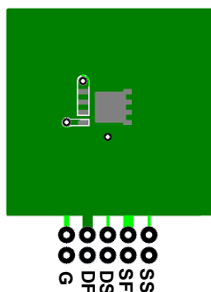
$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 15\text{ V}$ , $I_D = 17.5\text{ A}$ $V_{GS} = 10\text{ V}$ , $R_{GEN} = 6\text{ }\Omega$		10	19	ns
$t_r$	Rise Time			4	10	ns
$t_{d(off)}$	Turn-Off Delay Time			26	41	ns
$t_f$	Fall Time			3	10	ns
$Q_{g(TOT)}$	Total Gate Charge		$V_{GS} = 0\text{ V to }10\text{ V}$		28	39
	Total Gate Charge	$V_{GS} = 0\text{ V to }4.5\text{ V}$	$V_{DD} = 15\text{ V}$ $I_D = 17.5\text{ A}$	14	19	nC
$Q_{gs}$	Gate to Source Charge			4.4		nC
$Q_{gd}$	Gate to Drain "Miller" Charge			3.9		nC

### Drain-Source Diode Characteristics

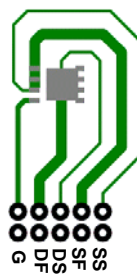
$V_{SD}$	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$ , $I_S = 1.9\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}$ , $I_S = 17.5\text{ A}$ (Note 2)		0.8	1.2	
$t_{rr}$	Reverse Recovery Time	$I_F = 17.5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$		30	49	ns
$Q_{rr}$	Reverse Recovery Charge			13	23	nC

#### NOTES:

1.  $R_{\theta JA}$  is determined with the device mounted on a 1 in<sup>2</sup> pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design.



a. 50  $^\circ\text{C}/\text{W}$  when mounted on a 1 in<sup>2</sup> pad of 2 oz copper.



b. 125  $^\circ\text{C}/\text{W}$  when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300  $\mu\text{s}$ , Duty cycle < 2.0 %.

3. As an N-ch device, the negative  $V_{GS}$  rating is for low duty cycle pulse occurrence only. No continuous rating is implied.

4.  $E_{AS}$  of 54 mJ is based on starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 0.3\text{ mH}$ ,  $I_{AS} = 19\text{ A}$ ,  $V_{DD} = 27\text{ V}$ ,  $V_{GS} = 10\text{ V}$ .

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.

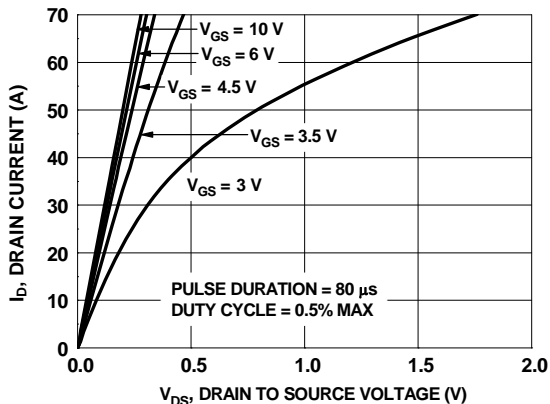


Figure 1. On Region Characteristics

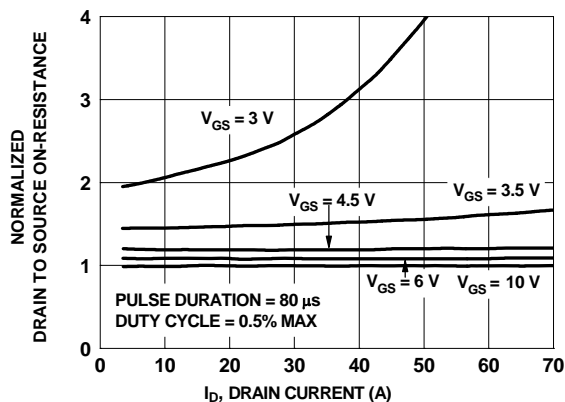


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

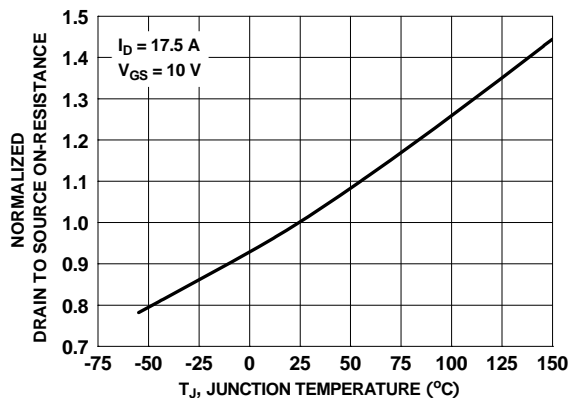


Figure 3. Normalized On Resistance vs. Junction Temperature

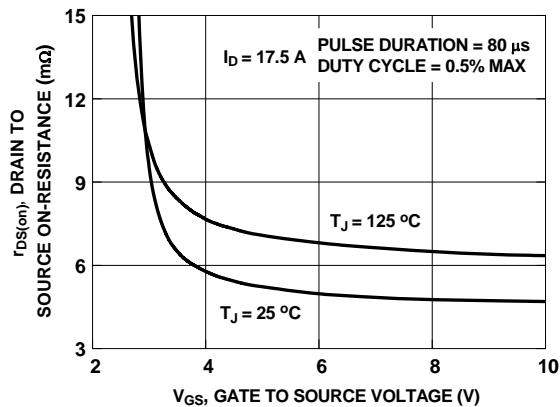


Figure 4. On-Resistance vs. Gate to Source Voltage

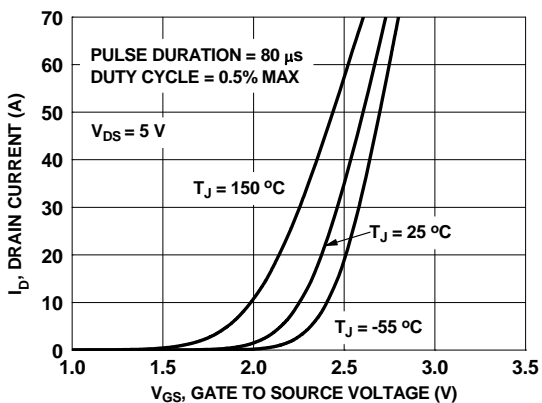


Figure 5. Transfer Characteristics

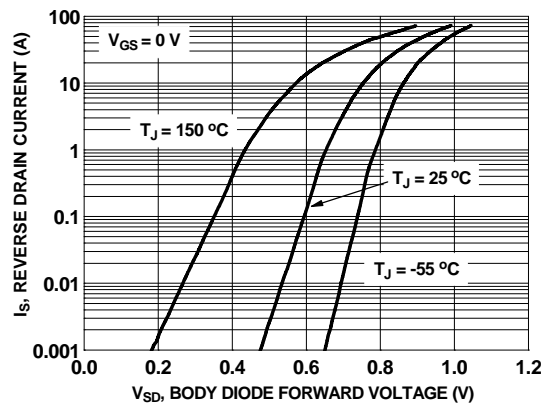
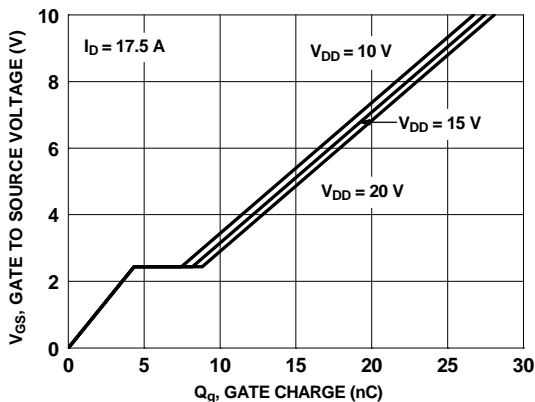
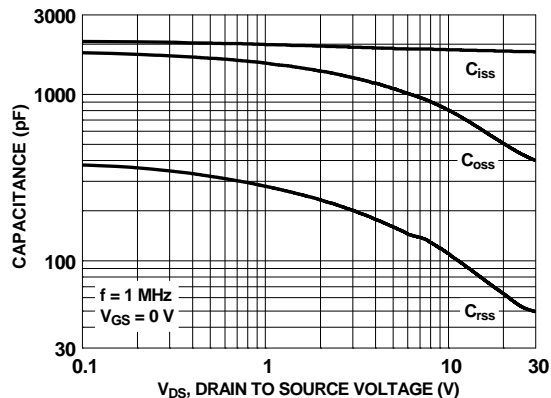


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

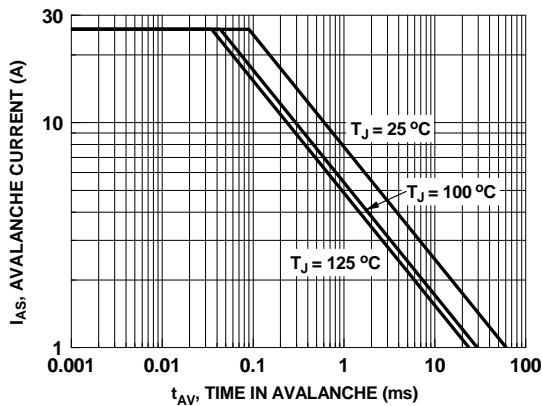
**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



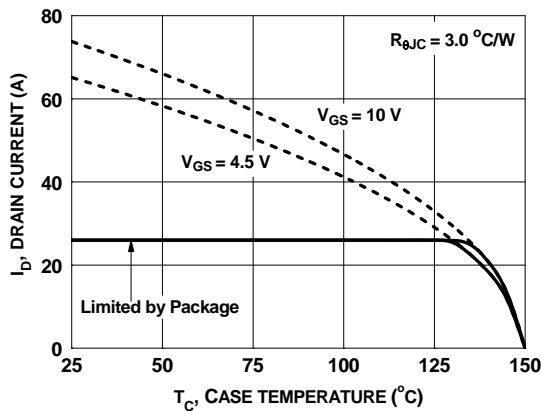
**Figure 7. Gate Charge Characteristics**



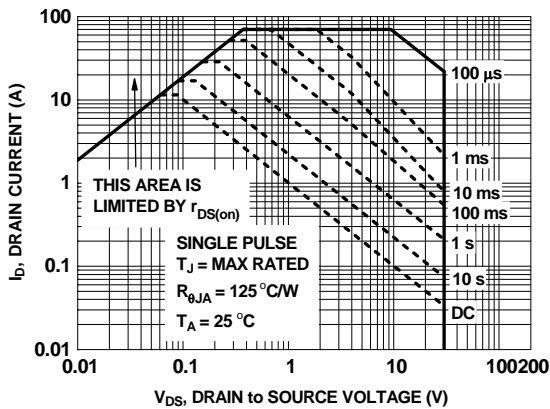
**Figure 8. Capacitance vs. Drain to Source Voltage**



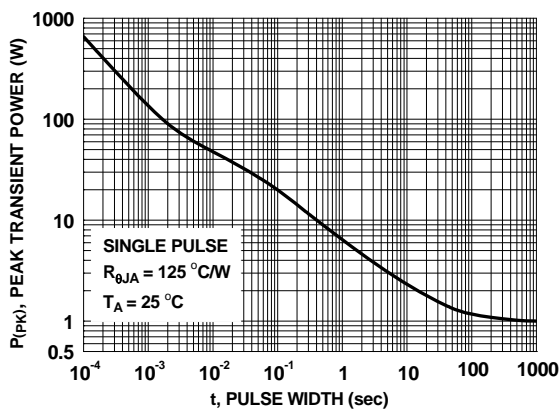
**Figure 9. Unclamped Inductive Switching Capability**



**Figure 10. Maximum Continuous Drain Current vs. Case Temperature**

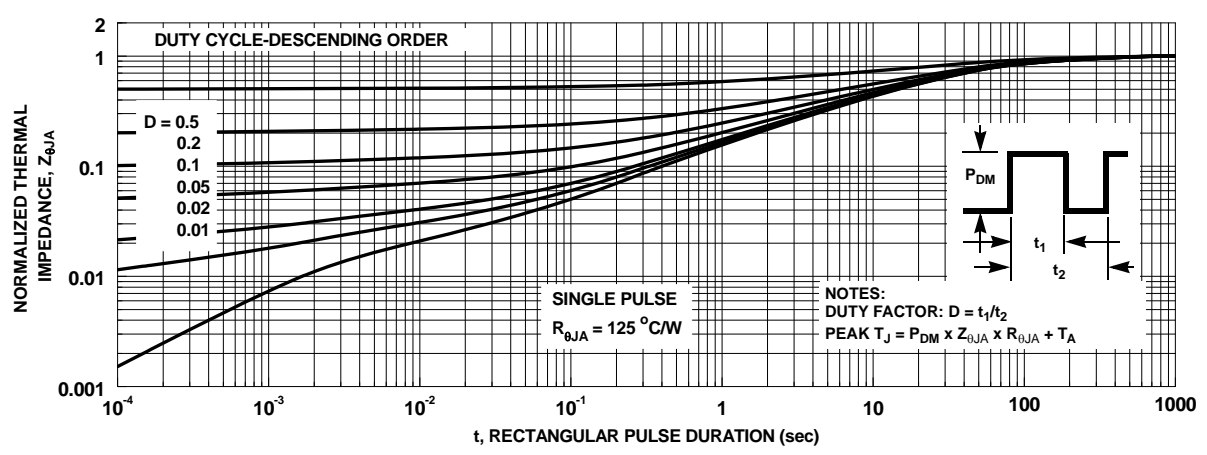


**Figure 11. Forward Bias Safe Operating Area**



**Figure 12. Single Pulse Maximum Power Dissipation**

**Typical Characteristics**  $T_J = 25\text{ }^\circ\text{C}$  unless otherwise noted.



**Figure 13. Junction-to-Ambient Transient Thermal Response Curve**

PQFN8 5X6, 1.27P  
CASE 483AE  
ISSUE A



TOP VIEW



LAND PATTERN RECOMMENDATION



SIDE VIEW

OPTIONAL DRAFT ANGLE MAY APPEAR ON FOUR SIDES OF THE PACKAGE



DETAIL C  
SCALE: 2:1



DETAIL B  
SCALE: 2:1



BOTTOM VIEW

NOTES: UNLESS OTHERWISE SPECIFIED

- A. PACKAGE STANDARD REFERENCE: JEDEC MO-240, ISSUE A, VAR. AA.
- B. DIMENSIONS DO NOT INCLUDE BURRS OR MOLD FLASH. MOLD FLASH OR BURRS DOES NOT EXCEED 0.10MM.
- C. ALL DIMENSIONS ARE IN MILLIMETERS.
- D. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-2009.
- E. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.

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