

MOSFET - N-Channel, POWERTRENCH®

100 V, 60 A, 8 mΩ

FDMS86101

General Description

This N-Channel MOSFET is produced using ON Semiconductor's advanced POWERTRENCH® process that has been especially tailored to minimize the on-state resistance and yet maintain superior switching performance.

Features

- Max $r_{DS(on)}$ = 8 mΩ at $V_{GS} = 10$ V, $I_D = 13$ A
- Max $r_{DS(on)}$ = 13.5 mΩ at $V_{GS} = 6$ V, $I_D = 9.5$ A
- Advanced Package and Silicon combination for low $r_{DS(on)}$ and high efficiency
- MSL1 robust package design
- 100% UIL tested
- 100% Rg tested
- These Devices are Pb-Free and are RoHS Compliant

Applications

- DC-DC Conversion

MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$ unless otherwise noted)

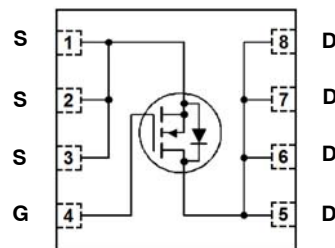
Symbol	Parameter	Value	Unit
V_{DS}	Drain to Source Voltage	100	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Drain Current:		A
	Continuous, $T_C = 25^\circ\text{C}$	60	
	Continuous, $T_A = 25^\circ\text{C}$ (Note 1a)	12.4	
	Pulsed	200	
E_{AS}	Single Pulse Avalanche Energy (Note 3)	173	mJ
P_D	Power Dissipation:		W
	$T_C = 25^\circ\text{C}$ $T_A = 25^\circ\text{C}$ (Note 1a)	104 2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range	-55 to +150	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.



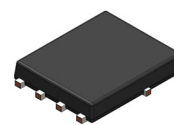
ON Semiconductor®

www.onsemi.com

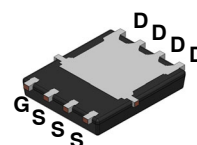


N-Channel MOSFET

Top

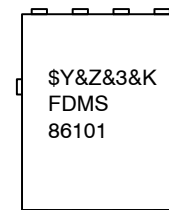


Bottom



Power 56
(PQFN8)
CASE 483AE

MARKING DIAGRAM



- \$Y = ON Semiconductor Logo
- &Z = Assembly Plant Code
- &3 = Data Code (Year & Week)
- &K = Lot
- FDMS86101 = Specific Device Code

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

FDMS86101

PACKAGE MARKING AND ORDERING INFORMATION

Device Marking	Device	Package	Quantity
FDMS86101	FDMS86101	Power 56 (PQFN8) (Pb-Free / Halogen Free)	3000/Tape&Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case	1.2	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)	50	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
--------	-----------	----------------	-----	-----	-----	------

OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}$, $V_{GS} = 0 \text{ V}$	100			V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		66		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}$, $V_{GS} = 0 \text{ V}$			800	nA
I_{GSS}	Gate to Source Leakage Current, Forward	$V_{GS} = \pm 20 \text{ V}$, $V_{DS} = 0 \text{ V}$			100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}$, $I_D = 250 \mu\text{A}$	2.0	2.9	4.0	V
$\Delta V_{GS(th)} / \Delta T_J$	Gate to Source Threshold Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, referenced to 25°C		-9		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}$, $I_D = 13 \text{ A}$		6.3	8	mΩ
		$V_{GS} = 6 \text{ V}$, $I_D = 9.5 \text{ A}$		8.4	13.5	
		$V_{GS} = 10 \text{ V}$, $I_D = 13 \text{ A}$, $T_J = 125^\circ\text{C}$		10.9	14	
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}$, $I_D = 13 \text{ A}$		45		S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}$, $V_{GS} = 0 \text{ V}$, $f = 1 \text{ MHz}$		2255	3000	pF
C_{oss}	Output Capacitance			460	610	pF
C_{rss}	Reverse Transfer Capacitance			30	45	pF
R_g	Gate Resistance			0.1	1.0	3.0

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50 \text{ V}$, $I_D = 13 \text{ A}$, $V_{GS} = 10 \text{ V}$, $R_{GEN} = 6 \Omega$		15	27	ns
t_r	Rise Time			11	20	ns
$t_{d(off)}$	Turn-Off Delay Time			27	44	ns
t_f	Fall Time			7	13	ns
Q_g	Total Gate Charge	$V_{GS} = 0 \text{ V}$ to 10 V , $V_{DD} = 50 \text{ V}$, $I_D = 13 \text{ A}$		39	55	nC
		$V_{GS} = 0 \text{ V}$ to 5 V , $V_{DD} = 50 \text{ V}$, $I_D = 13 \text{ A}$		22	31	nC
Q_{gs}	Gate to Source Charge	$V_{DD} = 40 \text{ V}$, $I_D = 68 \text{ A}$		9.5		nC
Q_{gd}	Gate to Drain "Miller" Charge	$V_{DD} = 40 \text{ V}$, $I_D = 68 \text{ A}$		10.8		nC

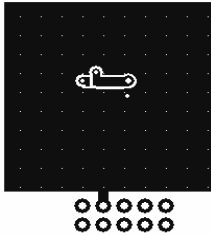
ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Condition	Min	Typ	Max	Unit
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 2.1\text{ A}$ (Note 2)		0.7	1.2	V
		$V_{GS} = 0\text{ V}, I_S = 13\text{ A}$ (Note 2)		0.8	1.3	
t_{rr}	Reverse Recovery Time	$I_F = 13\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$		56	90	ns
Q_{rr}	Reverse Recovery Charge			61	98	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in² pad 2 oz copper pad on a 1.5 × 1.5 in. board of FR-4 material. $R_{\theta CA}$ is determined by the user's board design.

NOTES:



a. 50 °C/W when mounted on a 1 in² pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

- 2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
- 3. E_{AS} of 173 mJ is based on starting $T_J = 25^\circ\text{C}$, $L = 0.3\text{ mH}$, $I_{AS} = 34\text{ A}$, $V_{DD} = 75\text{ V}$, $V_{GS} = 10\text{ V}$. 100% test at $L = 0.1\text{ mH}$, $I_{AS} = 49\text{ A}$.

TYPICAL CHARACTERISTICS

($T_J = 25^\circ\text{C}$ unless otherwise noted)

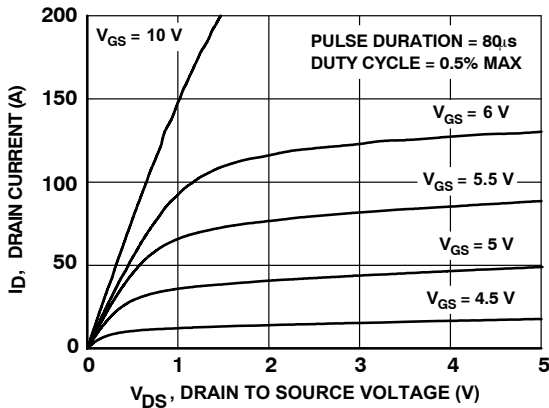


Figure 1. On Region Characteristics

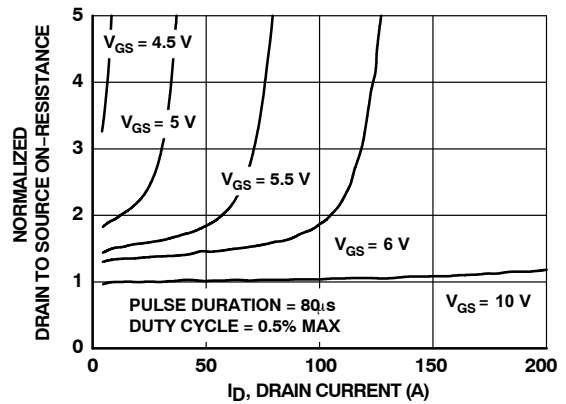


Figure 2. Normalized On-Resistance vs. Drain Current and Gate Voltage

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

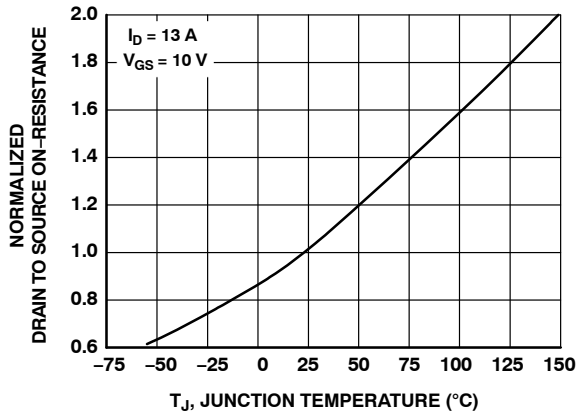


Figure 3. Normalized On Resistance vs. Junction Temperature

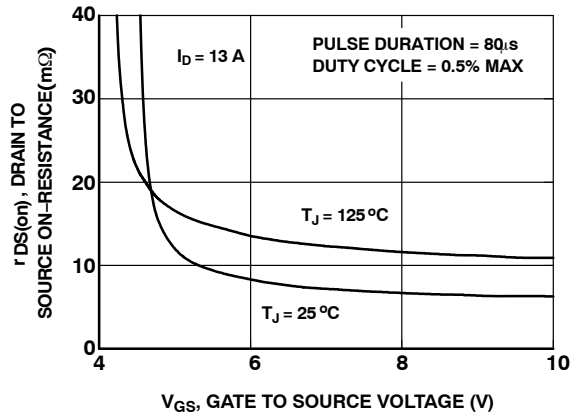


Figure 4. On-Resistance vs. Gate to Source Voltage

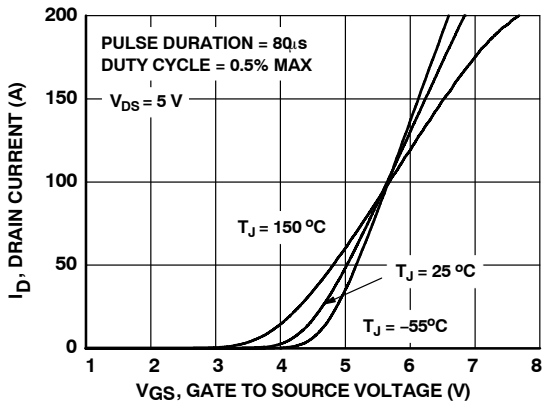


Figure 5. Transfer Characteristics

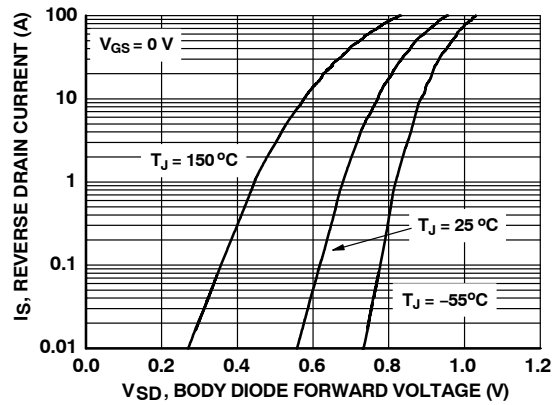


Figure 6. Source to Drain Diode Forward Voltage vs. Source Current

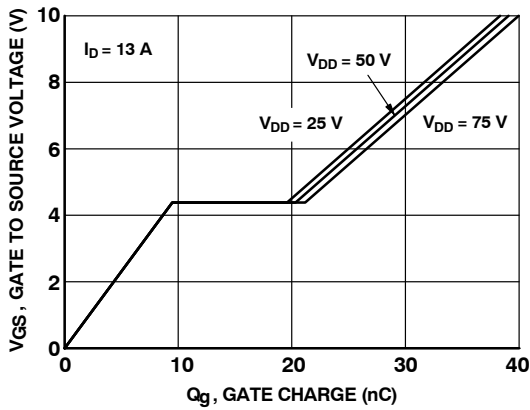


Figure 7. Gate Charge Characteristics

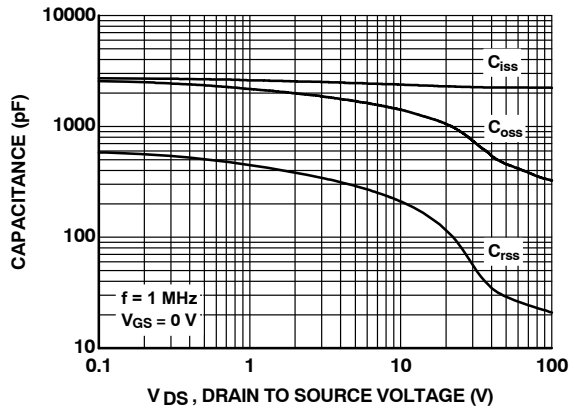


Figure 8. Capacitance vs. Drain to Source Voltage

TYPICAL CHARACTERISTICS (continued)

($T_J = 25^\circ\text{C}$ unless otherwise noted)

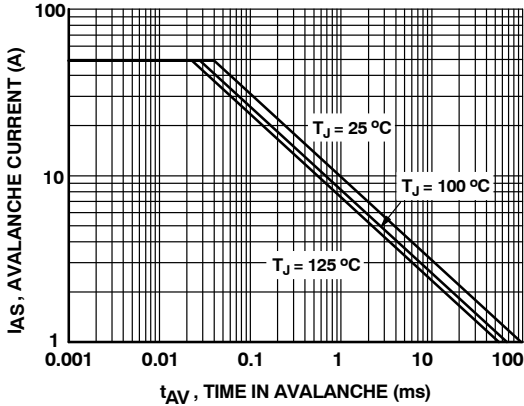


Figure 9. Unclamped Inductive Switching Capability

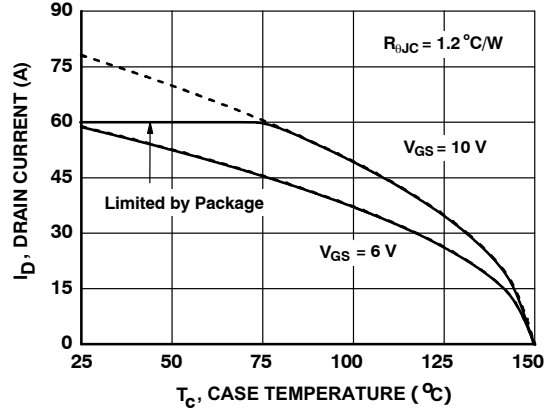


Figure 10. Maximum Continuous Drain Current vs. Case Temperature

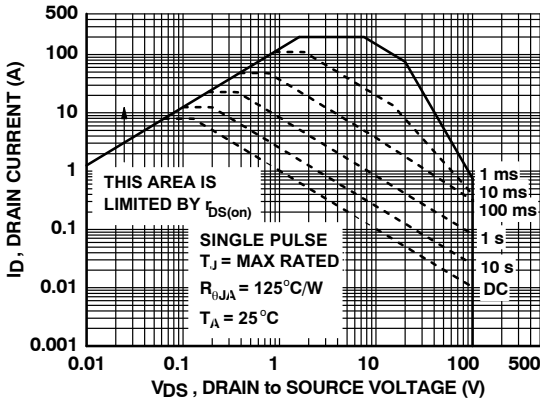


Figure 11. Forward Bias Safe Operating Area

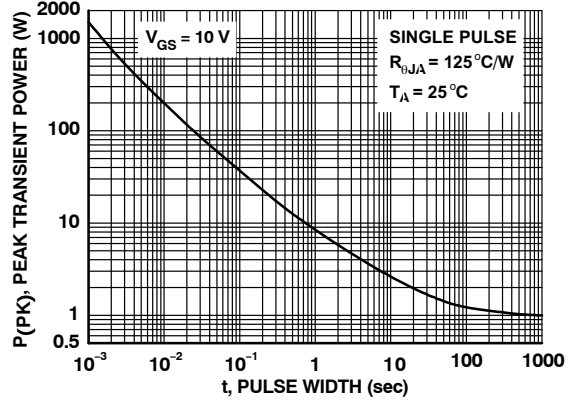


Figure 12. Single Pulse Maximum Power Dissipation

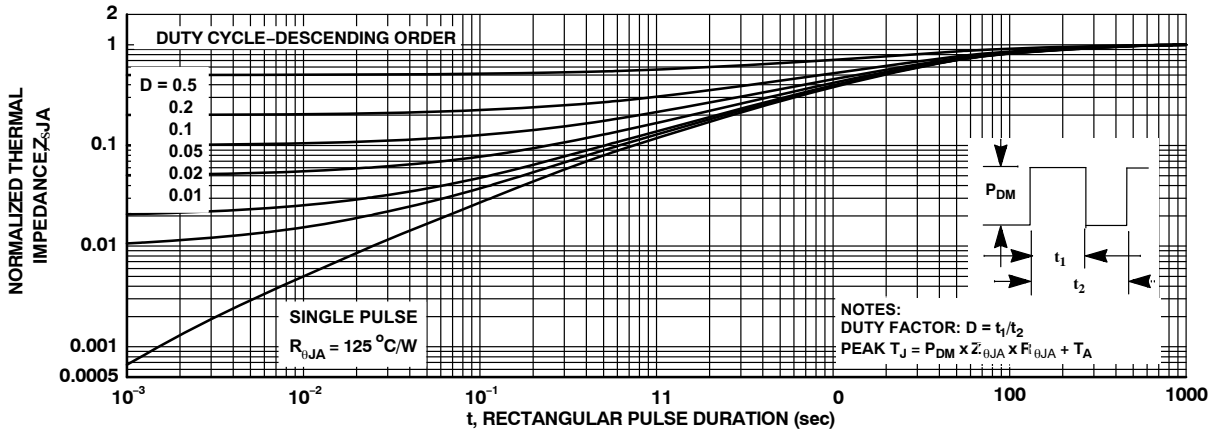


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

POWERTRENCH is registered trademark of Semiconductor Components Industries, LLC (SCILLC) or its subsidiaries in the United States and or other countries.

MECHANICAL CASE OUTLINE PACKAGE DIMENSIONS



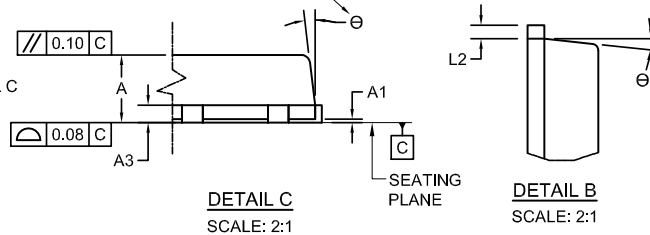
PQFN8 5X6, 1.27P
CASE 483AE
ISSUE C

DATE 21 JAN 2022

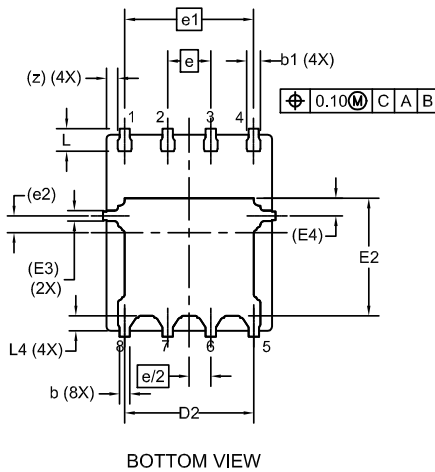


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. COPLANARITY APPLIES TO THE EXPOSED PADS AS WELL AS THE TERMINALS.
4. DIMENSIONS D1 AND E1 DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. SEATING PLANE IS DEFINED BY THE TERMINALS. "A1" IS DEFINED AS THE DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY.
6. IT IS RECOMMENDED TO HAVE NO TRACES OR VIAS WITHIN THE KEEP OUT AREA.



DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	0.90	1.00	1.10
A1	0.00	-	0.05
b	0.21	0.31	0.41
b1	0.31	0.41	0.51
A3	0.15	0.25	0.35
D	4.90	5.00	5.20
D1	4.80	4.90	5.00
D2	3.61	3.82	3.96
E	5.90	6.15	6.25
E1	5.70	5.80	5.90
E2	3.38	3.48	3.78
E3	0.30 REF		
E4	0.52 REF		
e	1.27 BSC		
e/2	0.635 BSC		
e1	3.81 BSC		
e2	0.50 REF		
L	0.51	0.66	0.76
L2	0.05	0.18	0.30
L4	0.34	0.44	0.54
z	0.34 REF		
θ	0°	-	12°



*FOR ADDITIONAL INFORMATION ON OUR PB-FREE STRATEGY AND SOLDERING DETAILS, PLEASE DOWNLOAD THE ON SEMICONDUCTOR SOLDERING AND MOUNTING TECHNIQUES REFERENCE MANUAL, SOLDERRM/D.

DOCUMENT NUMBER:	98AON13655G	Electronic versions are uncontrolled except when accessed directly from the Document Repository. Printed versions are uncontrolled except when stamped "CONTROLLED COPY" in red.
DESCRIPTION:	PQFN8 5X6, 1.27P	PAGE 1 OF 1

onsemi and ONSEMI are trademarks of Semiconductor Components Industries, LLC dba onsemi or its subsidiaries in the United States and/or other countries. onsemi reserves the right to make changes without further notice to any products herein. onsemi makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does onsemi assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. onsemi does not convey any license under its patent rights nor the rights of others.

onsemi, **Onsemi**, and other names, marks, and brands are registered and/or common law trademarks of Semiconductor Components Industries, LLC dba "**onsemi**" or its affiliates and/or subsidiaries in the United States and/or other countries. **onsemi** owns the rights to a number of patents, trademarks, copyrights, trade secrets, and other intellectual property. A listing of **onsemi**'s product/patent coverage may be accessed at www.onsemi.com/site/pdf/Patent-Marking.pdf. **onsemi** reserves the right to make changes at any time to any products or information herein, without notice. The information herein is provided "as-is" and **onsemi** makes no warranty, representation or guarantee regarding the accuracy of the information, product features, availability, functionality, or suitability of its products for any particular purpose, nor does **onsemi** assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. Buyer is responsible for its products and applications using **onsemi** products, including compliance with all laws, regulations and safety requirements or standards, regardless of any support or applications information provided by **onsemi**. "Typical" parameters which may be provided in **onsemi** data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. **onsemi** does not convey any license under any of its intellectual property rights nor the rights of others. **onsemi** products are not designed, intended, or authorized for use as a critical component in life support systems or any FDA Class 3 medical devices or medical devices with a same or similar classification in a foreign jurisdiction or any devices intended for implantation in the human body. Should Buyer purchase or use **onsemi** products for any such unintended or unauthorized application, Buyer shall indemnify and hold **onsemi** and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that **onsemi** was negligent regarding the design or manufacture of the part. **onsemi** is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

ADDITIONAL INFORMATION

TECHNICAL PUBLICATIONS:

Technical Library: www.onsemi.com/design/resources/technical-documentation
onsemi Website: www.onsemi.com

ONLINE SUPPORT: www.onsemi.com/support

For additional information, please contact your local Sales Representative at www.onsemi.com/support/sales