# MOSFET – P-Channel, POWERTRENCH®

## 30 V

# FDS6681Z

| $V_{DSS}$ | $R_{DS(on)}$ MAX | $I_D$ MAX |
|---|---|---|
| –30 V | 4.6 mΩ @ –10 V | –20 A |
| | 6.5 mΩ @ –4.5 V | |

### General Description

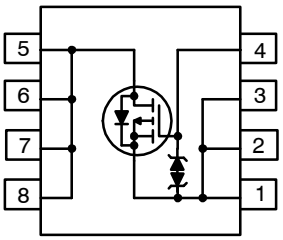
This P–Channel MOSFET is produced using **onsemi**'s advanced PowerTrench process that has been especially tailored to minimize the on–state resistance.

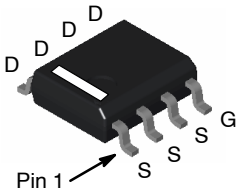
This device is well suited for Power Management and load switching applications common in Notebook Computers and Portable Battery Packs.

### Features

- –20 A, –30 V
  - $R_{DS(ON)}$ = 4.6 mΩ @ $V_{GS}$ = –10 V
  - $R_{DS(ON)}$ = 6.5 mΩ @ $V_{GS}$ = –4.5 V
- Extended $V_{GSS}$ Range (–25 V) for Battery Applications
- HBM ESD Protection Level of 8 kV Typical (Note 3)
- High Performance Trench Technology for Extremely Low $R_{DS(ON)}$
- High Power and Current Handling Capability
- Termination is Lead–free and RoHS Compliant
- This is a Pb–Free and Halide Free Device

P–Channel




**SOIC8**
**CASE 751EB**

### ABSOLUTE MAXIMUM RATINGS ($T_A$ = 25°C unless otherwise noted)

| Symbol | Parameter | | Ratings | Unit |
|---|---|---|---|---|
| $V_{DSS}$ | Drain–Source Voltage | | –30 | V |
| $V_{GSS}$ | Gate–Source Voltage | | ±25 | V |
| $I_D$ | Drain Current | Continuous (Note 1a) | –20 | A |
| | | Pulsed | –105 | |
| $P_D$ | Power Dissipation for Single Operation | (Note 1a) | 2.5 | W |
| | | (Note 1b) | 1.2 | |
| | | (Note 1c) | 1.0 | |
| $T_J$, $T_{STG}$ | Operating and Storage Junction Temperature Range | | –55 to +150 | °C |

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

### THERMAL CHARACTERISTICS

| Symbol | Parameter | Value | Unit |
|---|---|---|---|
| $R_{\theta JA}$ | Thermal Resistance, Junction–to–Ambient (Note 1a) | 50 | °C/W |
| $R_{\theta JC}$ | Thermal Resistance, Junction–to–Case (Note 1) | 25 | °C/W |

### MARKING DIAGRAM

FDS6681Z = Specific Device Code
A = Assembly Site
L = Wafer Lot Number
YW = Assembly Start Week

### ORDERING INFORMATION

| Device | Package | Shipping† |
|---|---|---|
| FDS6681Z | SOIC8 (Pb–Free) | 2500 / Tape & Reel |

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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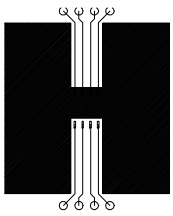
**ELECTRICAL CHARACTERISTICS** ($T_A$ = 25°C unless otherwise noted)

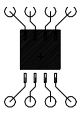
| Symbol | Parameter | Test Condition | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| **OFF CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain–Source Breakdown Voltage | $V_{GS}$ = 0 V, $I_D$ = –250 μA | –30 | – | – | V |
| $\frac{\Delta BV_{DSS}}{\Delta T_J}$ | Breakdown Voltage Temperature Coefficient | $I_D$ = –250 μA, Referenced to 25°C | – | –26 | – | mV/°C |
| $I_{DSS}$ | Zero Gate Voltage Drain Current | $V_{DS}$ = –24 V, $V_{GS}$ = 0 V | – | – | –1 | μA |
| $I_{GSS}$ | Gate–Body Leakage | $V_{GS}$ = ±25 V, $V_{DS}$ = 0 V | – | – | ±10 | μA |
| **ON CHARACTERISTICS** (Note 2) | | | | | | |
| $V_{GS(th)}$ | Gate Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = –250 μA | –1 | –1.8 | –3 | V |
| $\frac{\Delta V_{GS(th)}}{\Delta T_J}$ | Gate Threshold Voltage Temperature Coefficient | $I_D$ = –250 μA, Referenced to 25°C | – | 6 | – | mV/°C |
| $R_{DS(on)}$ | Static Drain–Source On–Resistance | $V_{GS}$ = –10 V, $I_D$ = –20 A | – | 3.8 | 4.6 | mΩ |
| | | $V_{GS}$ = –4.5 V, $I_D$ = –17 A | – | 5.2 | 6.5 | |
| | | $V_{GS}$ = –10 V, $I_D$ = –20 A, $T_J$ = 125°C | – | 5.0 | 6.3 | |
| $g_{FS}$ | Forward Transconductance | $V_{DS}$ = –5 V, $I_D$ = –20 A | – | 79 | – | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{DS}$ = –15 V, $V_{GS}$ = 0 V, f = 1.0 MHz | – | 7540 | – | pF |
| $C_{oss}$ | Output Capacitance | | – | 1400 | – | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | – | 1120 | – | pF |
| **SWITCHING CHARACTERISTICS** (Note 2) | | | | | | |
| $t_{d(on)}$ | Turn–On Delay Time | $V_{DD}$ = –15 V, $I_D$ = –1 A, $V_{GS}$ = –10 V, $R_{GEN}$ = 6 Ω | – | 20 | 35 | ns |
| $t_r$ | Turn–On Rise Time | | – | 9 | 18 | ns |
| $t_{d(off)}$ | Turn–Off Delay Time | | – | 660 | 1060 | ns |
| $t_f$ | Turn–Off Fall Time | | – | 380 | 610 | ns |
| $Q_{g(TOT)}$ | Total Gate Charge at $V_{GS}$= –10 V | $V_{DS}$ = –15 V, $I_D$ = –20 A | – | 185 | 260 | nC |
| $Q_{g(TOT)}$ | Total Gate Charge at $V_{GS}$= –5 V | | – | 105 | 150 | nC |
| $Q_{gs}$ | Gate–Source Charge | | – | 26 | – | nC |
| $Q_{gd}$ | Gate–Drain Charge | | – | 47 | – | nC |
| **DRAIN–SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS** | | | | | | |
| $I_S$ | Maximum Continuous Drain–Source Diode Forward Current | | – | – | –2.1 | A |
| $V_{SD}$ | Drain–Source Diode Forward Voltage | $V_{GS}$ = 0 V, $I_S$ = –2.1 A (Note 2) | – | –0.7 | –1.2 | V |
| $t_{RR}$ | Reverse Recovery Time | $I_F$ = –20 A, $dI_F/dt$ = 100 A/μs (Note 2) | – | 125 | – | ns |
| $Q_{RR}$ | Reverse Recovery Charge | | – | 94 | – | nC |

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

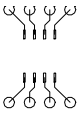
1. $R_{\theta JA}$ is the sum of the junction–to–case and case–to–ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a) 50°C/W (10 s)
62.5°C/W steady state when mounted on a 1in$^2$ pad of 2 oz copper.



b) 105°C/W when mounted on a .04 in$^2$ pad of 2 oz copper.



c) 125°C/W when mounted on a minimum pad.

Scale 1:1 on letter size paper

2. Pulse Test: Pulse Width < 300 μs, Duty Cycle < 2.0%
3. The diode connected between the gate and source serves only as protection against ESD. No gate overvoltage rating is implied.

## TYPICAL CHARACTERISTICS

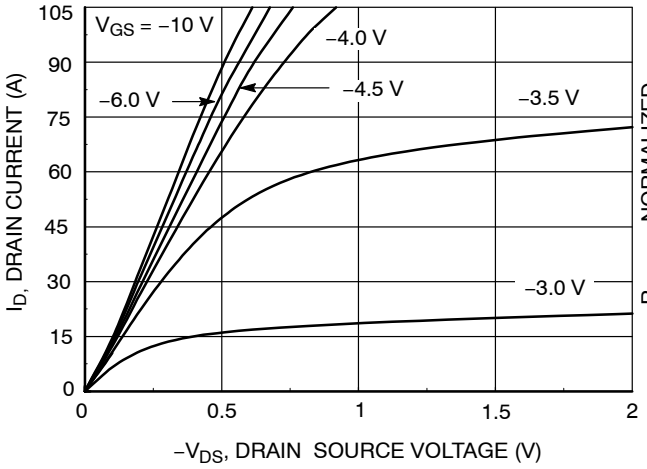



**Figure 1. On−Region Characteristics**

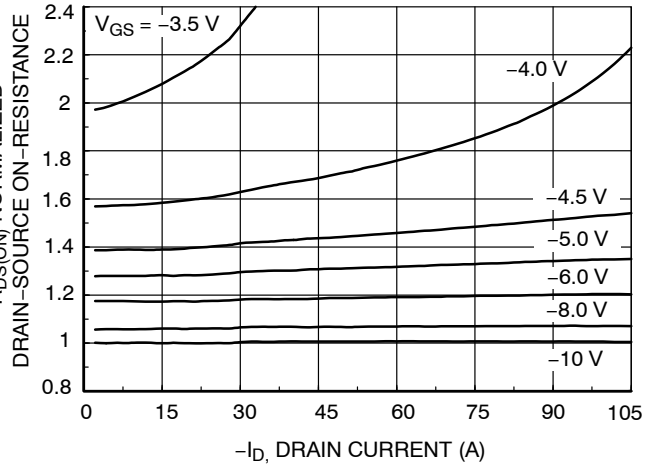



**Figure 2. On−Resistance Variation with Drain Current and Gate Voltage**

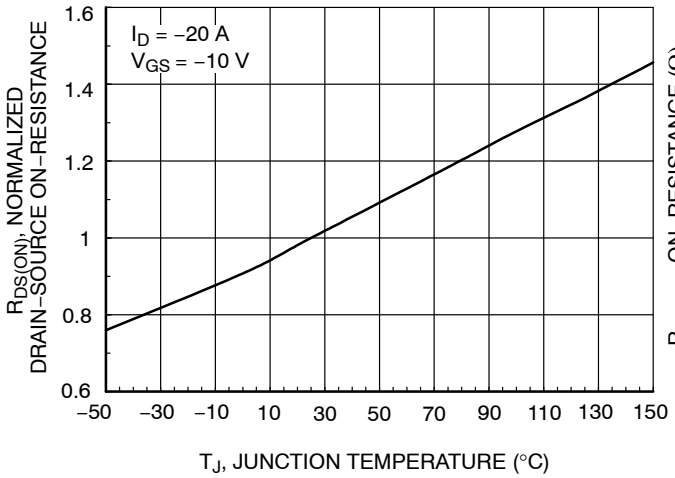



**Figure 3. On−Resistance Variation with Temperature**

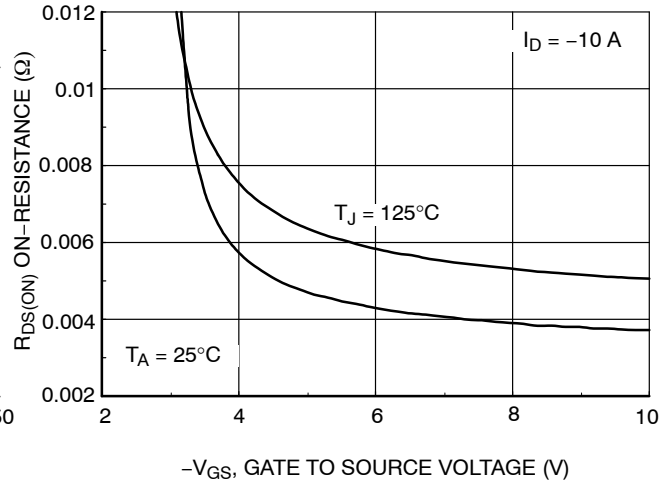



**Figure 4. On−Resistance Variation with Gate−to−Source Voltage**

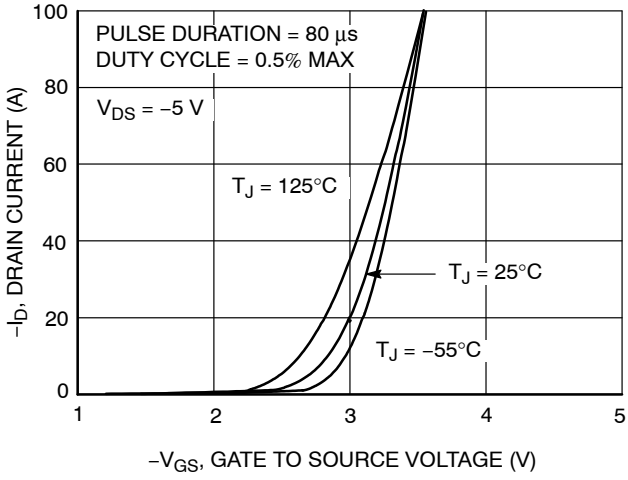



**Figure 5. Transfer Characteristics**

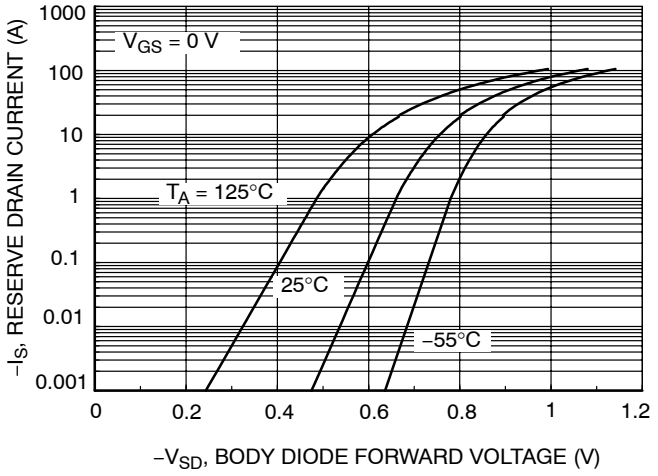



**Figure 6. Body Diode Forward Voltage Variation with Source Current and Temperature**

## TYPICAL CHARACTERISTICS (continued)

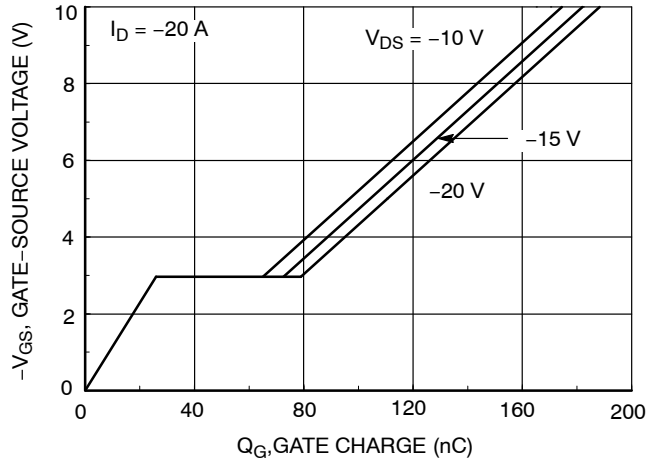



**Figure 7. Gate Charge Characteristics**

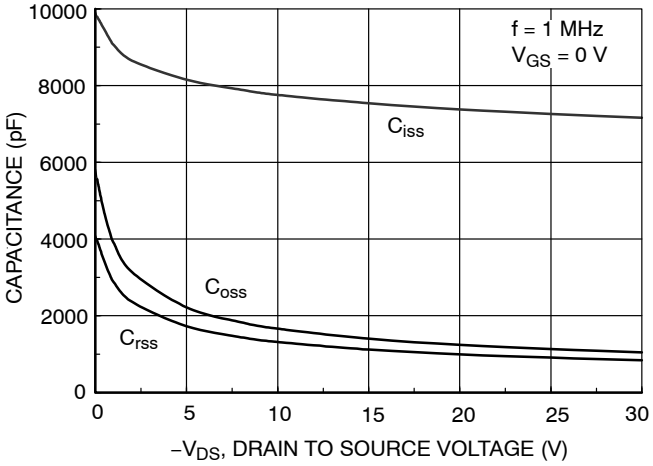



**Figure 8. Capacitance Characteristics**

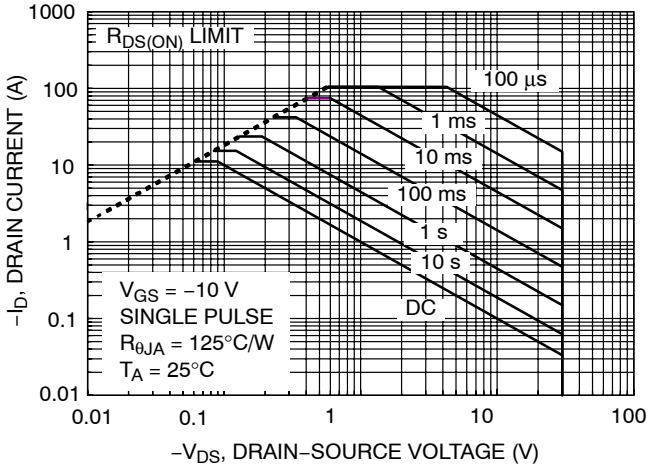



**Figure 9. Maximum Safe Operating Area**

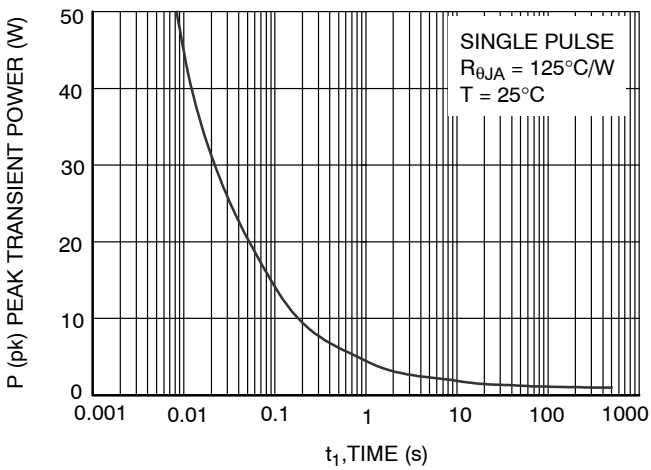



**Figure 10. Single Pulse Maximum Power Dissipation**

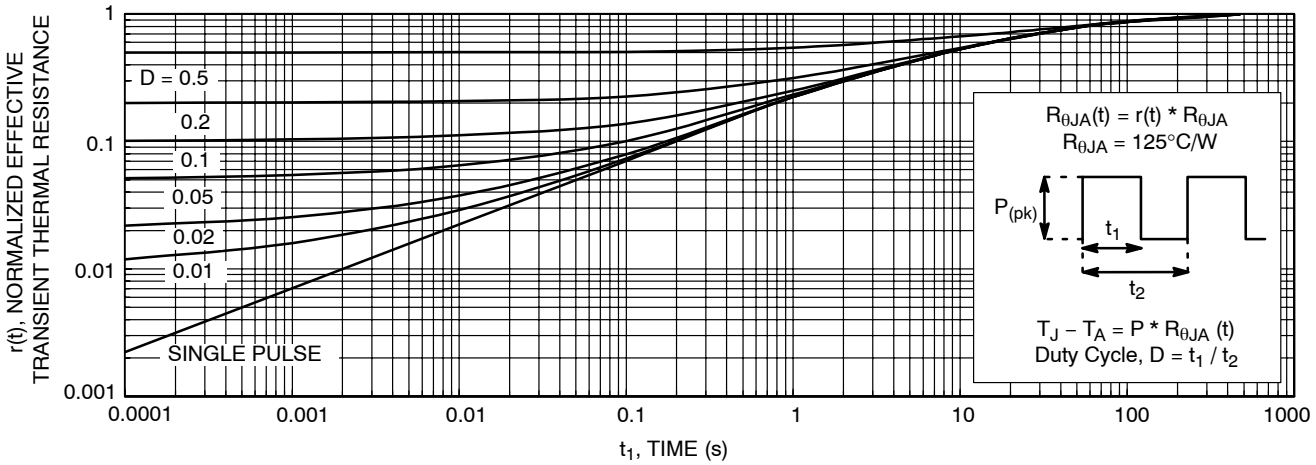



**Figure 11. Transient Thermal Response Curve**

Thermal characterization performed using the conditions described in Note 1c.
Transient thermal response will change depending on the circuit board design.

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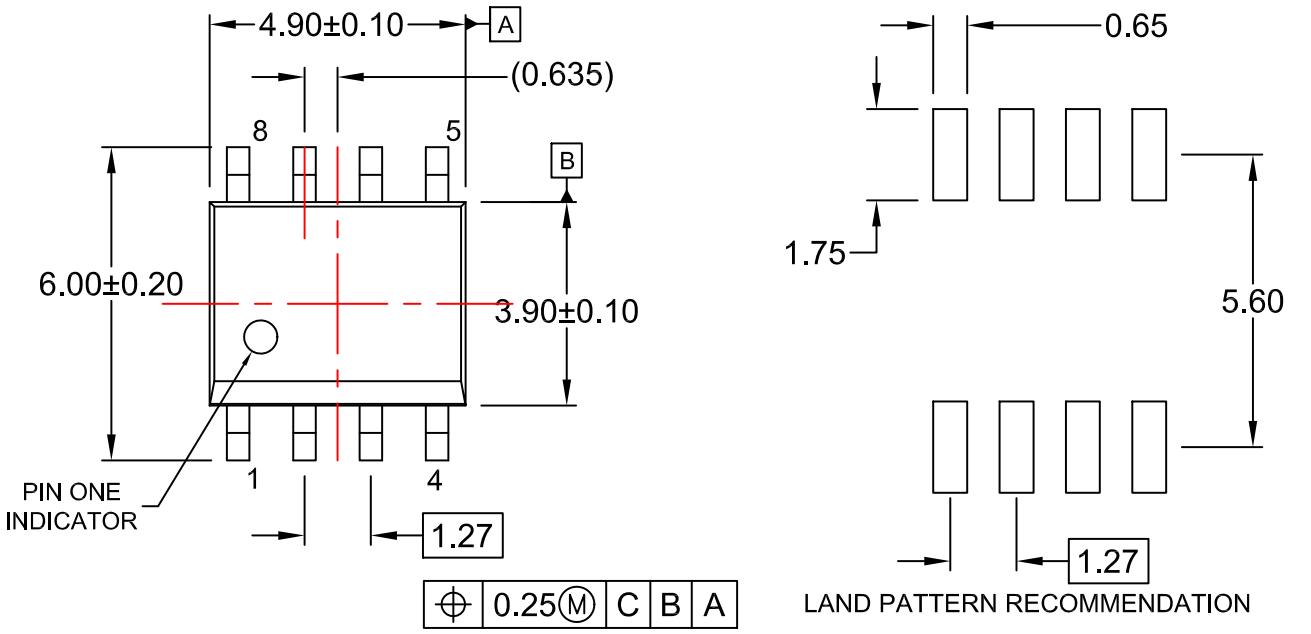
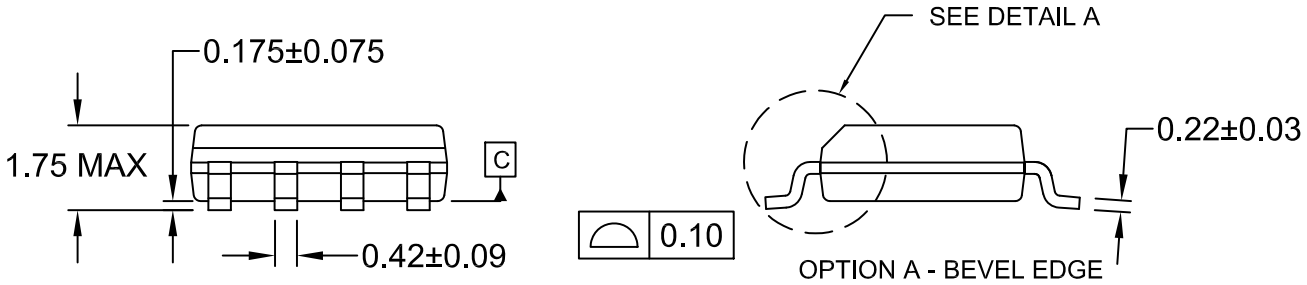
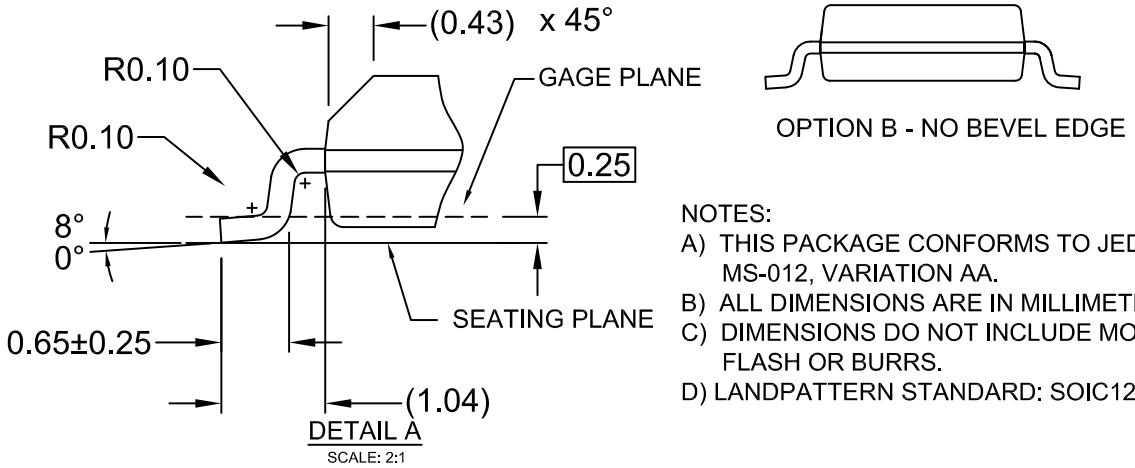
**SOIC8**
CASE 751EB
ISSUE A

DATE 24 AUG 2017




NOTES:
A) THIS PACKAGE CONFORMS TO JEDEC MS-012, VARIATION AA.
B) ALL DIMENSIONS ARE IN MILLIMETERS.
C) DIMENSIONS DO NOT INCLUDE MOLD FLASH OR BURRS.
D) LANDPATTERN STANDARD: SOIC127P600X175-8M

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