

MOSFET – N-Channel, POWERTRENCH®

100 V, 5.6 A, 160 mΩ

FDT1600N10ALZ

General Description

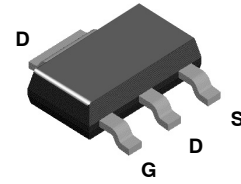
This N-Channel MOSFET is produced using onsemi's advanced POWERTRENCH process that has been tailored to minimize the on-state resistance and maintain superior switching performance.

Features

- $R_{DS(on)} = 121\text{ m}\Omega$ (Typ.) @ $V_{GS} = 10\text{ V}$, $I_D = 2.8\text{ A}$
- $R_{DS(on)} = 156\text{ m}\Omega$ (Typ.) @ $V_{GS} = 5\text{ V}$, $I_D = 1.8\text{ A}$
- Low Gate Charge (Typ. 2.9 nC)
- Low C_{rss} (Typ. 2.04 pF)
- Fast Switching
- 100% Avalanche Tested
- Improved dv/dt Capability
- RoHS Compliant

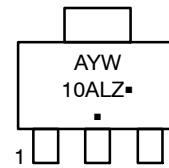
Applications

- Consumer Appliances
- LED TV and Monitor
- Synchronous Rectification
- Uninterruptible Power Supply
- Micro Solar Inverter



SOT-223
 CASE 318H

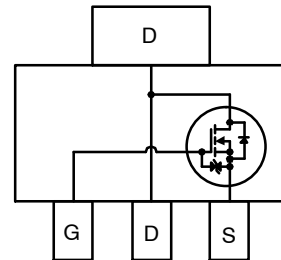
MARKING DIAGRAM



- A = Assembly Location
- Y = Year
- W = Work Week
- 10ALZ = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information on page 3 of this data sheet.

FDT1600N10ALZ

MOSFET MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter		FDT1600N10ALZ	Unit
V_{DSS}	Drain to Source Voltage		100	V
V_{GSS}	Gate to Source Voltage		± 20	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	5.6	A
		- Continuous ($T_C = 100^\circ\text{C}$)	3.5	
I_{DM}	Drain Current	- Pulsed (Note 2)	11.2	A
E_{AS}	Single Pulse Avalanche Energy (Note 3)		9.2	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 4)		6.0	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	10.42	W
		- Derate Above 25°C	0.083	
T_J, T_{STG}	Operating and Storage Junction Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL CHARACTERISTICS

Symbol	Parameter		FDT1600N10ALZ	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case (Note 1)		12	$^\circ\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient (Note 1a)		60	

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain to Source Breakdown Voltage	$I_D = 250 \mu\text{A}, V_{GS} = 0 \text{ V}$	100	-	-	V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	$I_D = 250 \mu\text{A}$, Referenced to 25°C	-	0.1	-	$\text{V}/^\circ\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}$	-	-	1	μA
		$V_{DS} = 80 \text{ V}, V_{GS} = 0 \text{ V}, T_C = 125^\circ\text{C}$	-	-	500	
I_{GSS}	Gate to Source Leakage Current	$V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V}$	-	-	± 10	μA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{GS} = V_{DS}, I_D = 250 \mu\text{A}$	1.4	-	2.8	V
$R_{DS(on)}$	Static Drain to Source On Resistance	$V_{GS} = 10 \text{ V}, I_D = 2.8 \text{ A}$	-	121	160	m Ω
		$V_{GS} = 5 \text{ V}, I_D = 1.8 \text{ A}$	-	156	375	
g_{FS}	Forward Transconductance	$V_{DS} = 10 \text{ V}, I_D = 5.6 \text{ A}$	-	26.1	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}, f = 1 \text{ MHz}$	-	169	225	μF		
C_{oss}	Output Capacitance		-	43	55			
C_{rss}	Reverse Transfer Capacitance		-	2.04	-			
$C_{oss(er)}$	Energy Related Output Capacitance	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	85	-	μF		
$Q_{g(tot)}$	Total Gate Charge at 10 V	$V_{GS} = 10 \text{ V}$	$V_{DD} = 50 \text{ V}, I_D = 5.6 \text{ A}$ (Note 5)	-	2.9	3.77	nC	
$Q_{g(tot)}$	Total Gate Charge at 5 V	$V_{GS} = 5 \text{ V}$		-	1.6	2.08		
Q_{gs}	Gate to Source Gate Charge			-	0.7	-		
Q_{gd}	Gate to Drain "Miller" Charge			-	0.64	-		
$V_{plateau}$	Gate Plateau Voltage			-	3.81	-		V
Q_{sync}	Total Gate Charge Sync.	$V_{DS} = 0 \text{ V}, I_D = 2.8 \text{ A}$		-	2.45	-		
Q_{oss}	Output Charge	$V_{DS} = 50 \text{ V}, V_{GS} = 0 \text{ V}$	-	5.2	-	nC		

FDT1600N10ALZ

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise noted) (continued)

Symbol	Parameter	Test Conditions	Min	Typ	Max	Unit
ESR	Equivalent Series Resistance (G-S)	$f = 1\text{ MHz}$	-	2.1	-	Ω

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 50\text{ V}$, $I_D = 5.6\text{ A}$, $V_{GS} = 10\text{ V}$, $R_G = 4.7\ \Omega$	-	7.4	24.8	ns
t_r	Rise Time		-	2.5	15	ns
$t_{d(off)}$	Turn-Off Delay Time		-	13.5	37	ns
t_f	Turn-Off Fall Time		-	2.4	14.8	ns

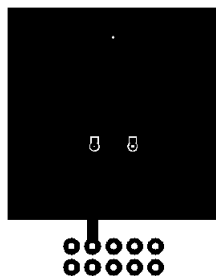
(Note 5)

DRAIN-SOURCE DIODE CHARACTERISTICS

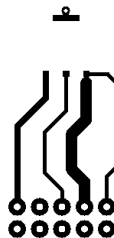
I_S	Maximum Continuous Drain to Source Diode Forward Current	-	-	5.6	A	
I_{SM}	Maximum Pulsed Drain to Source Diode Forward Current	-	-	11.2	A	
V_{SD}	Source to Drain Diode Forward Voltage	$V_{GS} = 0\text{ V}$, $I_S = 5.6\text{ A}$	-	-	1.3	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}$, $I_{SD} = 5.6\text{ A}$, $V_{DD} = 50\text{ V}$ $di_f/dt = 100\text{ A}/\mu\text{s}$	-	34.1	-	ns
Q_{rr}	Reverse Recovery Charge		-	32.7	-	nC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

- $R_{\theta JA}$ is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. $60^\circ\text{C}/\text{W}$ when mounted on a 1 in^2 pad of 2 oz copper



b. $118^\circ\text{C}/\text{W}$ when mounted on a minimum pad of 2 oz copper

- Repetitive rating: pulse-width limited by maximum junction temperature.
- Starting $T_J = 25^\circ\text{C}$, $L = 3\text{ mH}$, $I_{AS} = 2.47\text{ A}$.
- $I_{SD} \leq 5.6\text{ A}$, $di/dt \leq 200\text{ A}/\mu\text{s}$, $V_{DD} \leq BV_{DSS}$, starting $T_J = 25^\circ\text{C}$.
- Essentially independent of operating temperature typical characteristics.

PACKAGE MARKING AND ORDERING INFORMATION

Part Number	Top Mark	Package	Reel Size	Tape Width	Shipping†
FDT1600N10ALZ	10ALZ	SOT-223	13"	12 mm	4000/ Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).

FDT1600N10ALZ

TYPICAL CHARACTERISTICS

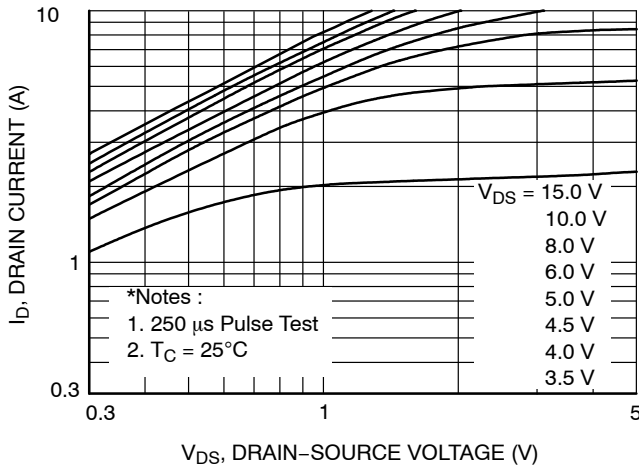


Figure 1. On-Region Characteristics

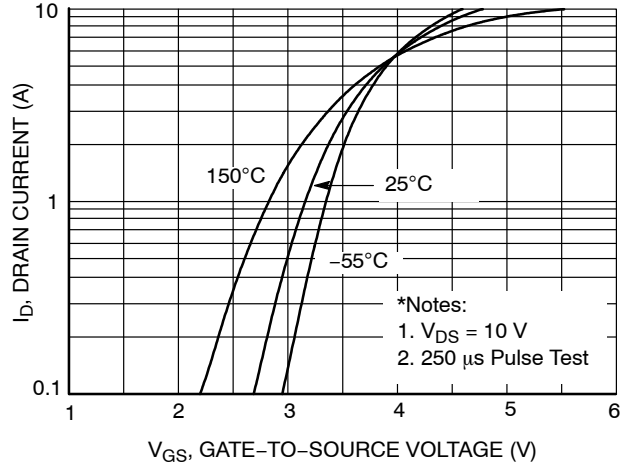


Figure 2. Transfer Characteristics

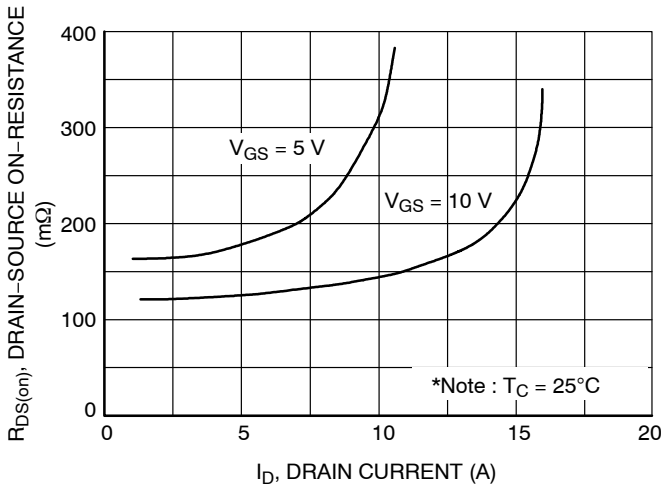


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

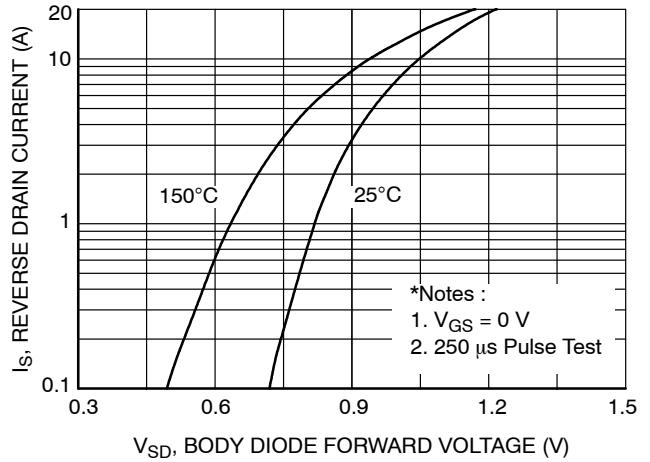


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

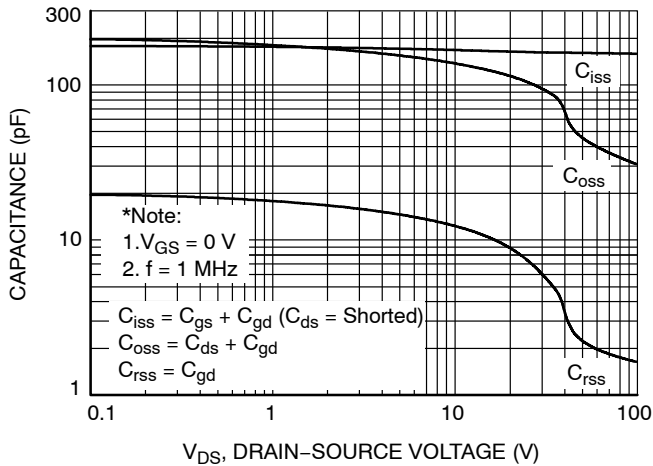


Figure 5. Capacitance Characteristics

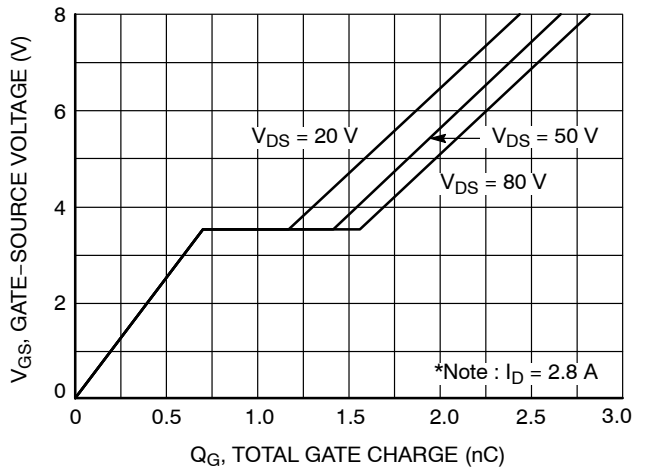


Figure 6. Gate Charge Characteristics

FDT1600N10ALZ

TYPICAL CHARACTERISTICS (continued)

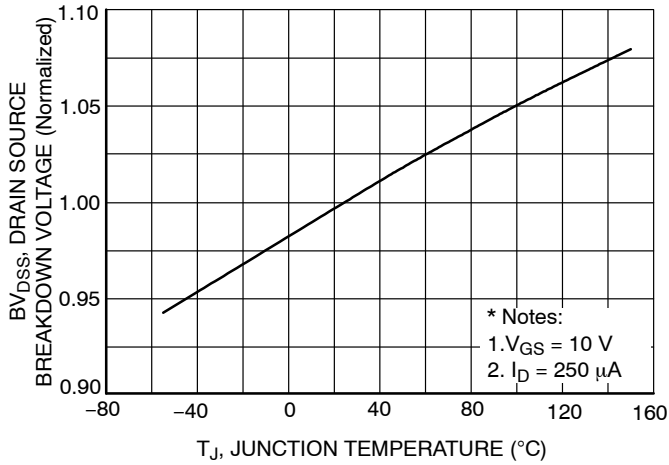


Figure 7. Breakdown Voltage Variation vs. Temperature

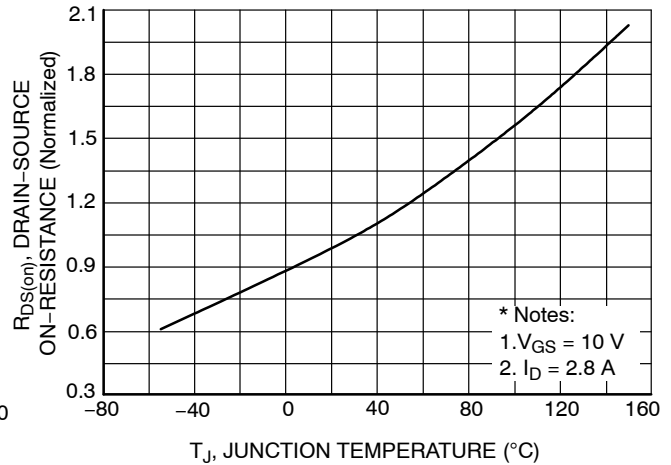


Figure 8. On-Resistance Variation vs. Temperature

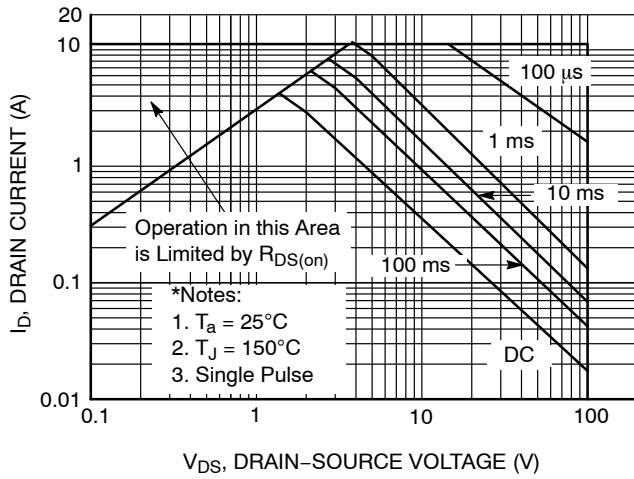


Figure 9. Maximum Safe Operating Area

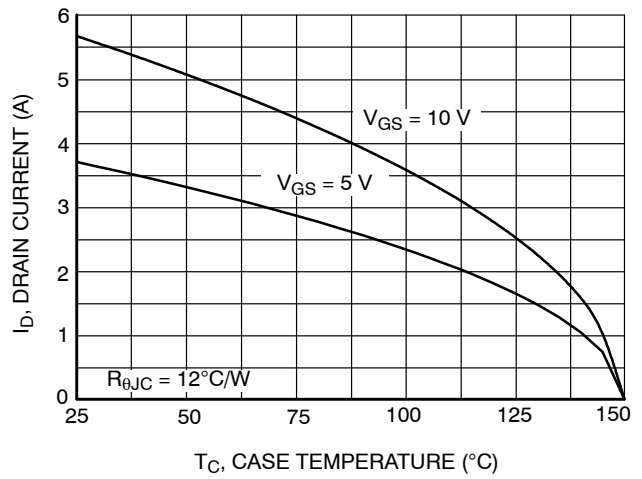


Figure 10. Maximum Drain Current vs. Case Temperature

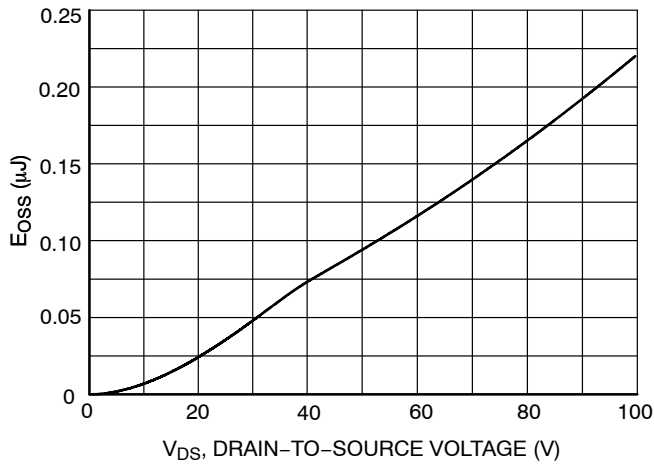


Figure 11. E_{OSS} vs. Drain-to-Source Voltage

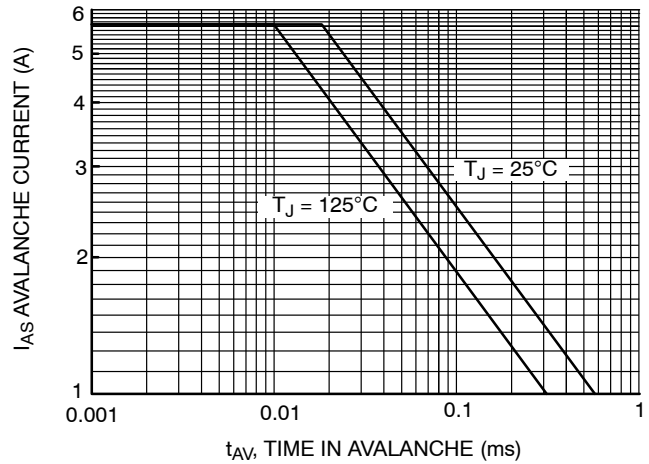


Figure 12. Unclamped Inductive Switching Capability

FDT1600N10ALZ

TYPICAL CHARACTERISTICS (continued)

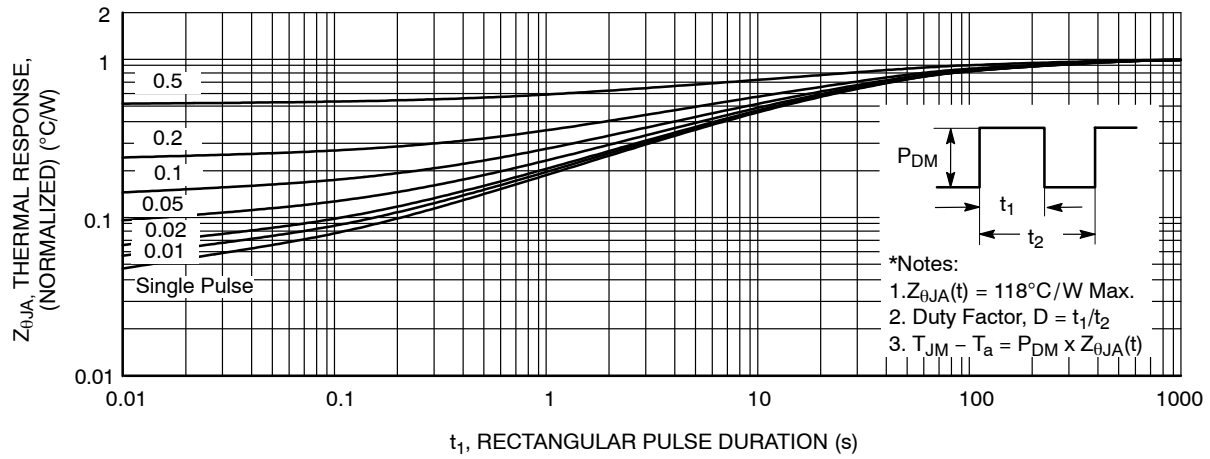


Figure 13. Transient Thermal Response Curve

FDT1600N10ALZ

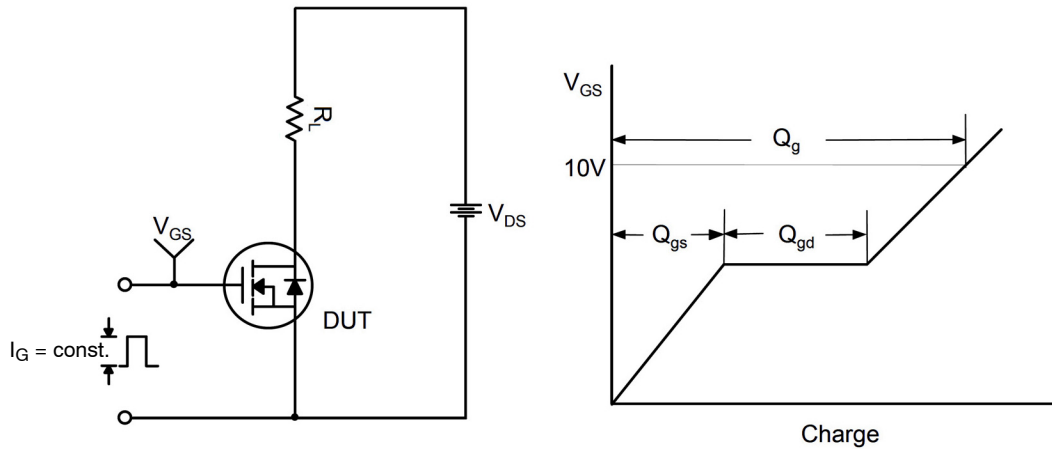


Figure 14. Gate Charge Test Circuit & Waveform

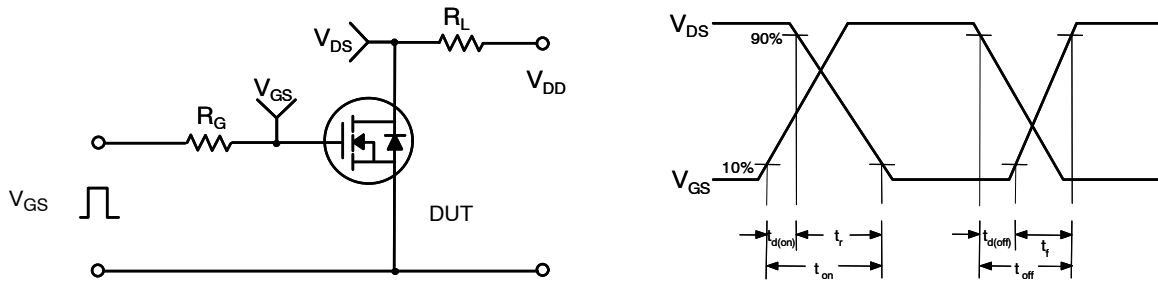


Figure 15. Resistive Switching Test Circuit & Waveforms

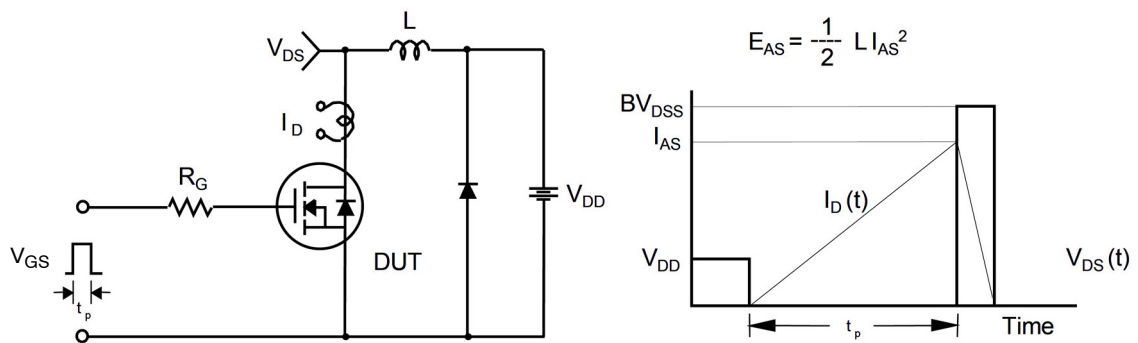


Figure 16. Unclamped Inductive Switching Test Circuit & Waveforms

FDT1600N10ALZ

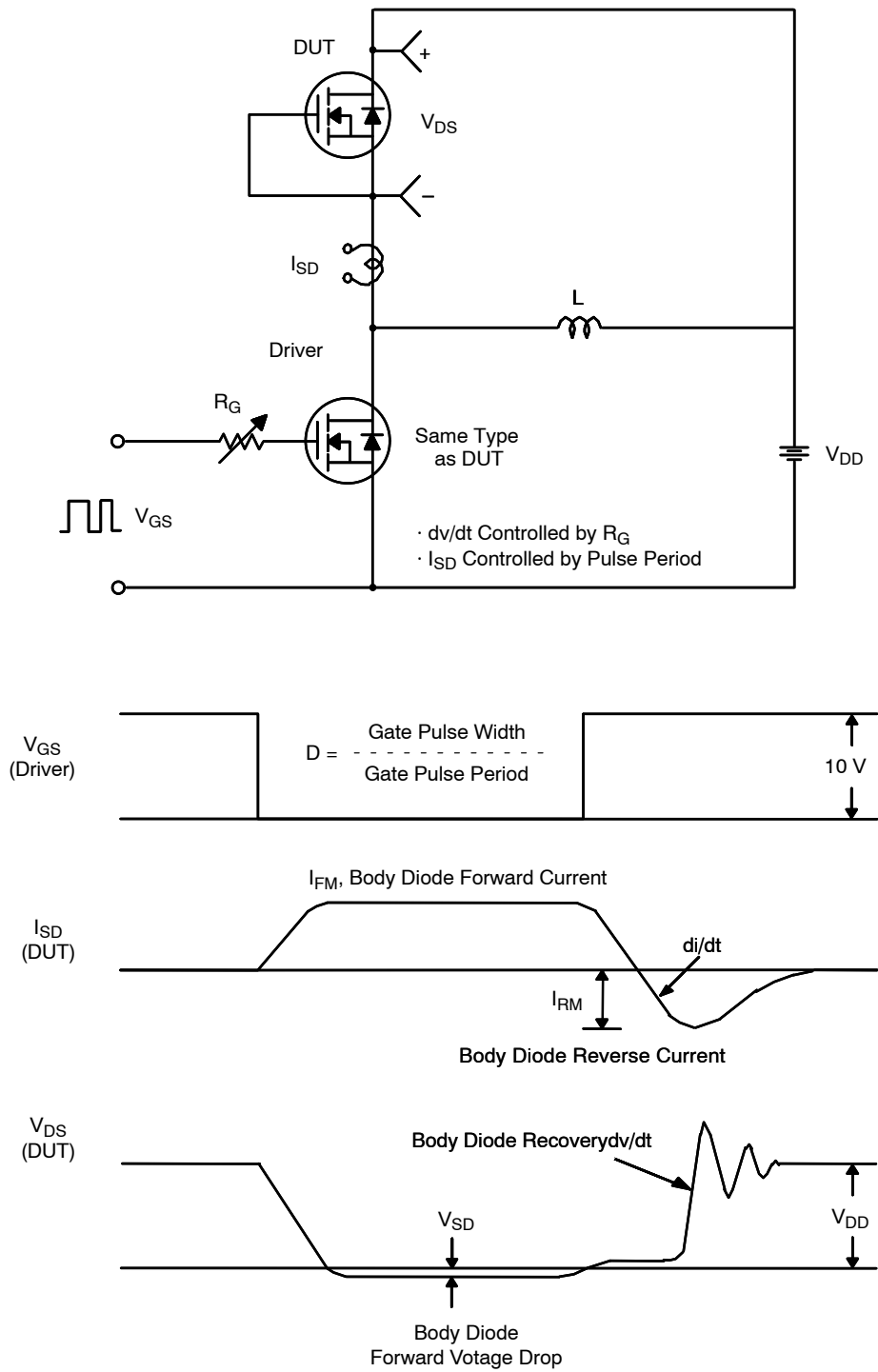


Figure 17. Peak Diode Recovery dv/dt Test Circuit & Waveforms

FDT1600N10ALZ

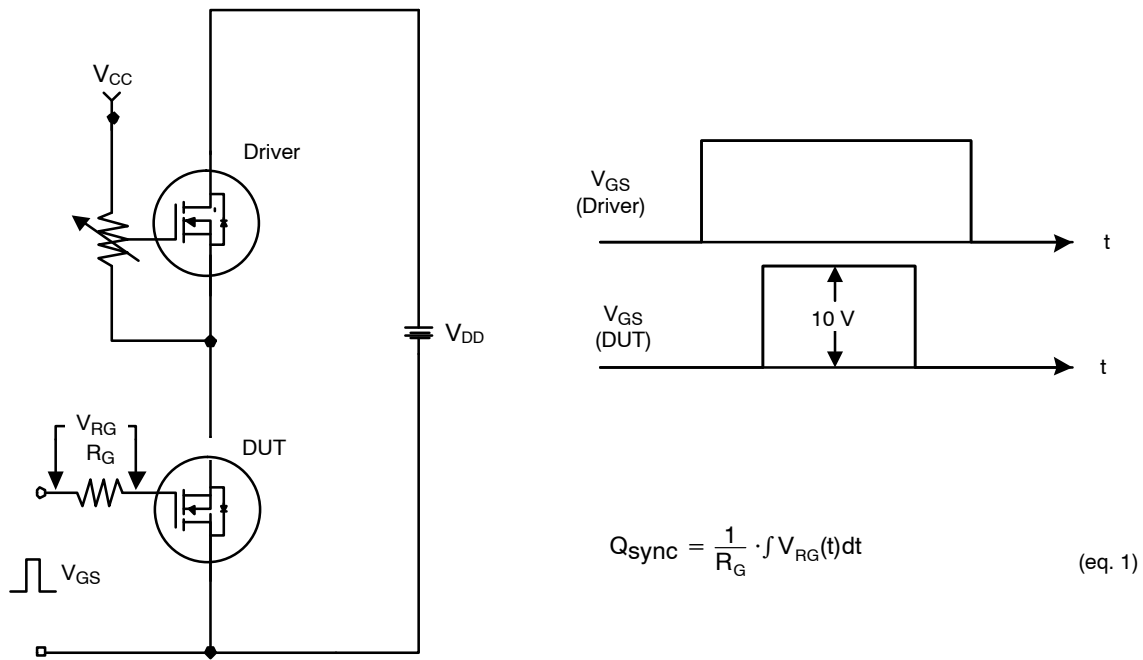
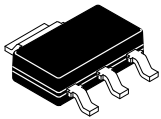


Figure 18. Total Gate Charge Q_{sync} . Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

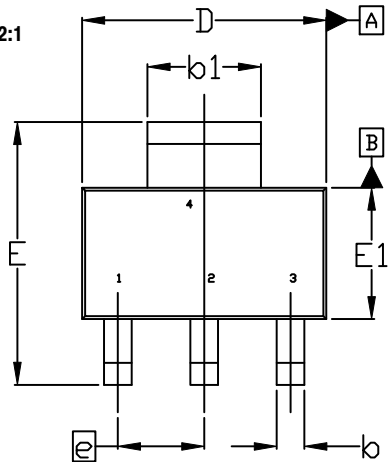
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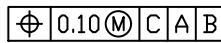
SOT-223
CASE 318H
ISSUE B

DATE 13 MAY 2020

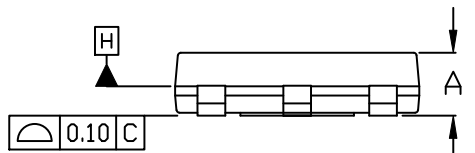
SCALE 2:1



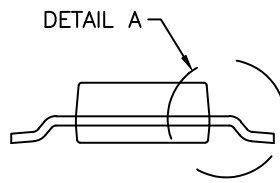
TOP VIEW



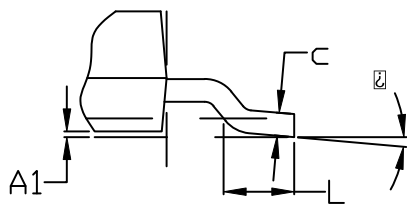
NOTE 7



SIDE VIEW



END VIEW

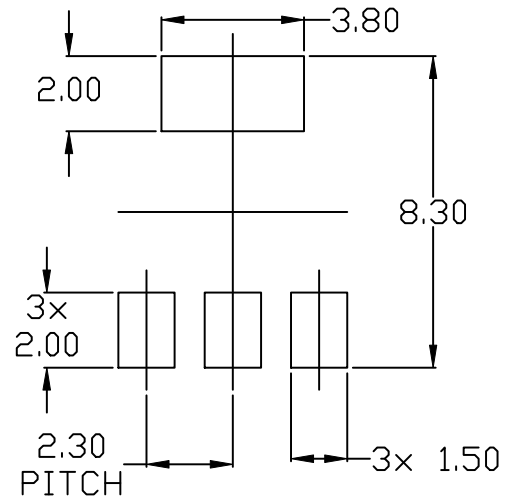


DETAIL A

NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 2009.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSIONS D & E1 ARE DETERMINED AT DATUM H. DIMENSIONS DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. SHALL NOT EXCEED 0.23mm PER SIDE.
4. LEAD DIMENSIONS b AND b1 DO NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION IS 0.08mm PER SIDE.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.
6. A1 IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT OF THE PACKAGE BODY.
7. POSITIONAL TOLERANCE APPLIES TO DIMENSIONS b AND b1.

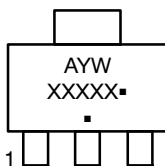
DIM	MILLIMETERS		
	MIN.	NOM.	MAX.
A	---	---	1.80
A1	0.02	0.06	0.11
b	0.60	0.74	0.88
b1	2.90	3.00	3.10
c	0.24	---	0.35
D	6.30	6.50	6.70
E	6.70	7.00	7.30
E1	3.30	3.50	3.70
e	2.30 BSC		
L	0.25	---	---
∠	0°	---	10°



RECOMMENDED MOUNTING FOOTPRINT

* For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERM/D.

GENERIC MARKING DIAGRAM*



- A = Assembly Location
- Y = Year
- W = Work Week
- XXXXX = Specific Device Code
- = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "▪", may or may not be present. Some products may not follow the Generic Marking.

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