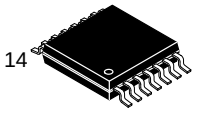
3.3 V LVDS High Speed Differential Driver/Receiver

FIN1019



TSSOP−14 WB
CASE 948G

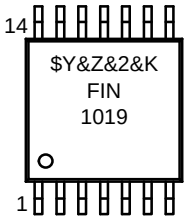
General Description

This driver and receiver pair are designed for high speed interconnects utilizing Low Voltage Differential Signaling (LVDS) technology. The driver translates LVTTL signals to LVDS levels with a typical differential output swing of 350 mV and the receiver translates LVDS signals, with a typical differential input threshold of 100 mV, into LVTTL levels. LVDS technology provides low EMI at ultra low power dissipation even at high frequencies. This device is ideal for high speed clock or data transfer.

Features

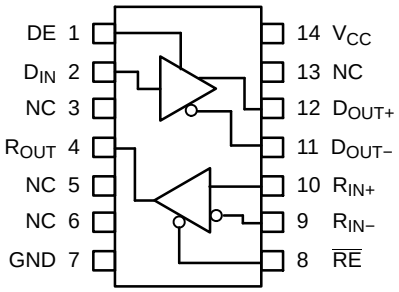
- Greater than 400 Mbs Data Rate
- 3.3 V Power Supply Operation
- 0.5 ns Maximum Differential Pulse Skew
- 2.5 ns Maximum Propagation Delay
- Low Power Dissipation
- Power−Off Protection
- 100 mV Receiver Input Sensitivity
- Fail Safe Protection Open−circuit, Shorted and Terminated Conditions
- Meets or Exceeds the TIA/EIA−644 LVDS Standard
- Flow−through Pinout Simplifies PCB Layout
- 14−Lead TSSOP Package Save Space
- This Device is Pb−Free, Halide Free and is RoHS Compliant

MARKING DIAGRAM



$Y = Logo
&Z = Assembly Plant Code
&2 = 2−Digit Date Code
&K = 2−Digits Lot Run Traceability Code
FIN1019 = Specific Device Code

CONNECTION DIAGRAM



FUNCTION TABLE

R_{IN+}	R_{IN-}	$\overline{RE}$	R_{OUT}
L	H	L	L
H	L	L	H
X	X	H	Z
Fail Safe Condition		L	H

D_{IN}	DE	D_{OUT+}	D_{OUT-}
L	H	L	H
H	H	H	L
X	L	Z	Z
Open−Circuit or Z	H	L	H

H = HIGH Logic Level L = LOW Logic Level X = Don't Care
Z = High Impedance Fail Safe = Open, Shorted, Terminated

ORDERING INFORMATION

Order Number	Package	Shipping†
FIN1019MTCX	TSSOP−14 WB (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PIN DESCRIPTIONS

Pin Name	Description
D_{IN}	LVTTL Data Input
D_{OUT+}	Non−inverting LVDS Output
D_{OUT-}	Inverting LVDS Output
DE	Driver Enable (LVTTL, Active HIGH)
R_{IN+}	Non−Inverting LVDS Input
R_{IN-}	Inverting LVDS Input
R_{OUT}	LVTTL Receiver Output
$\overline{RE}$	Receiver Enable (LVTTL, Active LOW)
V_{CC}	Power Supply
GND	Ground
NC	No Connect

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Rating
V_{CC}	Supply Voltage	−0.5 V to +4.6 V
D_{IN}, DE, $\overline{RE}$	LVTTL DC Input Voltage	−0.5 V to +6 V
R_{IN+}, R_{IN-}	LVDS DC Input Voltage	−0.5 V to 4.7 V
R_{OUT}	LVTTL DC Output Voltage	−0.5 V to +6 V
D_{OUT+}, D_{OUT-}	LVDS DC Output Voltage	−0.5 V to 4.7 V
I_{OSD}	LVDS Driver Short Circuit Current	Continuous
I_O	LVTTL DC Output Current	16 mA
T_{STG}	Storage Temperature Range	−65°C to +150°C
T_J	Max Junction Temperature	150°C
T_L	Lead Temperature (Soldering, 10 Seconds)	260°C
	ESD (Human Body Model)	≥6500 V
	ESD (Machine Model)	≥300 V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value
V_{CC}	Supply Voltage	3.0 V to 3.6 V
V_{IN}	Input Voltage	0 to V_{CC}
$\|V_{ID}\|$	Magnitude of Differential Voltage	100 mV to V_{CC}
V_{IC}	Common−Mode Input Voltage	0.05 V to 2.35 V
T_A	Operating Temperature	−40°C to +85°C

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

DC ELECTRICAL CHARACTERISTICS (Over supply voltage and operating temperature ranges, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 1)	Max	Unit
LVDS DIFFERENTIAL DRIVER CHARACTERISTICS						
V_{OD}	Output Differential Voltage	R_L = 100 Ω, See Figure 1	250	350	450	mV
ΔV_{OD}	V_{OD} Magnitude Change from Differential LOW−to−HIGH		−	−	25	mV
V_{OS}	Offset Voltage		1.125	1.25	1.375	V
ΔV_{OS}	Offset Magnitude Change from Differential LOW−to−HIGH		−	−	25	mV
I_{OZD}	Disabled Output Leakage Current	V_{OUT} = V_{CC} or GND, DE = 0 V	−	−	±20	μA
I_{OFF}	Power Off Output Current	V_{CC} = 0 V, V_{OUT} = 0 V or 3.6 V	−	−	±20	μA
I_{OS}	Short Circuit Output Current	V_{OUT} = 0 V, DE = V_{CC}	−	−	−8	mA
		V_{OD} = 0 V, DE = V_{CC}	−	−	±8	
LVTTL DRIVER CHARACTERISTICS						
V_{OH}	Output HIGH Voltage	I_{OH} = −100 μA, $\overline{RE}$ = 0 V, See Figure 6 and Table 1	V_{CC} − 0.2	−	−	V
		I_{OH} = −8 mA, $\overline{RE}$ = 0 V, V_{ID} = 400 mV V_{ID} = 400 mV, V_{IC} = 1.2 V, see Figure 6	2.4	−	−	
V_{OL}	Output LOW Voltage	I_{OL} = 100 μA, $\overline{RE}$ = 0 V, V_{ID} = −400 mV See Figure 6 and Table 1	−	−	0.2	V
		I_{OL} = −8 mA, $\overline{RE}$ = 0 V, V_{ID} = −400 mV V_{ID} = −400 mV, V_{IC} = 1.2 V, see Figure 6	−	−	0.5	
I_{OZ}	Disabled Output Leakage Current	V_{OUT} = V_{CC} or GND, $\overline{RE}$ = V_{CC}	−	−	±20	μA
LVDS RECEIVER CHARACTERISTICS						
V_{TH}	Differential Input Threshold HIGH	See Figure 6 and Table 1	−	−	100	mV
V_{TL}	Differential Input Threshold LOW	See Figure 6 and Table 1	−100	−	−	mV
I_{IN}	Input Current	V_{IN} = 0 V or V_{CC}	−	−	±20	μA
$I_{I(OFF)}$	Power−OFF Input Current	V_{CC} = 0 V, V_{IN} = 0 V or 3.6 V	−	−	±20	μA
LVTTL DRIVER AND CONTROL SIGNALS CHARACTERISTICS						
V_{IH}	Input HIGH Voltage		2.0	−	V_{CC}	V
V_{IL}	Input LOW Voltage		GND	−	0.8	V
I_{IN}	Input Current	V_{IN} = 0 V or V_{CC}	−	−	±20	μA
$I_{I(OFF)}$	Power−OFF Input Current	V_{CC} = 0 V, V_{IN} = 0 V or 3.6 V	−	−	±20	μA
V_{IK}	Input Clamp Voltage	I_{IK} = −18 mA	−1.5	−	−	V
DEVICE CHARACTERISTICS						
I_{CC}	Power Supply Current	Driver Enabled, Driver Load: R_L = 100 Ω Receiver Disabled, No Receiver Load	−	−	12.5	mA
		Driver Enabled, Driver Load: R_L = 100 Ω, Receiver Enabled, (R_{IN+} = 1 V and R_{IN-} = 1.4 V) or (R_{IN+} = 1.4 V and R_{OUT-} = 1 V)	−	−	12.5	mA
		Driver Disabled, Receiver Enabled, (R_{IN+} = 1 V and R_{IN-} = 1.4 V) or (R_{IN+} = 1.4 V and R_{IN-} = 1 V)	−	−	7.0	mA
		Driver Disabled, Receiver Disabled	−	−	7.0	mA
C_{IN}	Input Capacitance	Any LVTTL or LVDS Input	−	4	−	pF
C_{OUT}	Output Capacitance	Any LVTTL or LVDS Output	−	6	−	pF

1. All typical values are at T_A = 25°C and with V_{CC} = 3.3 V.

AC ELECTRICAL CHARACTERISTICS (Over supply voltage and operating temperature ranges, unless otherwise specified)

Symbol	Parameter	Test Conditions	Min	Typ (Note 2)	Max	Unit
DRIVER TIMING CHARACTERISTICS						
t_{PLHD}	Differential Propagation Delay LOW−to−HIGH	R_L = 100 Ω, C_L = 10 pF, See Figure 2 and Figure 3	0.5	−	1.5	ns
t_{PHLD}	Differential Propagation Delay HIGH−to−LOW		0.5	−	1.5	ns
t_{TLHD}	Differential Output Rise Time (20% to 80%)		0.4	−	1.0	ns
t_{THLD}	Differential Output Fall Time (80% to 20%)		0.4	−	1.0	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$		−	−	0.5	ns
$t_{SK(PP)}$	Part−to−Part Skew (Note 3)	R_L = 100 Ω, C_L = 10 pF, See Figure 4 and Figure 5	−	−	1.0	ns
t_{ZHD}	Differential Output Enable Time from Z to HIGH		−	−	5.0	ns
t_{ZLD}	Differential Output Enable Time from Z to LOW		−	−	5.0	ns
t_{HZD}	Differential Output Disable Time from HIGH to Z		−	−	5.0	ns
t_{LZD}	Differential Output Disable Time from LOW to Z		−	−	5.0	ns
RECEIVER TIMING CHARACTERISTICS						
t_{PLH}	Propagation Delay LOW−to−HIGH	$\|V_{ID}\|$ = 400 mV, C_L = 10 pF, See Figure 6 and Figure 7	0.9	−	2.5	ns
t_{PHL}	Propagation Delay HIGH−to−LOW		0.9	−	2.5	ns
t_{TLH}	Output Rise Time (20% to 80%)		−	0.5	−	ns
t_{THL}	Output Fall Time (80% to 20%)		−	0.5	−	ns
$t_{SK(P)}$	Pulse Skew $\|t_{PLH} - t_{PHL}\|$		−	−	0.5	ns
$t_{SK(PP)}$	Part−to−Part Skew (Note 3)		−	−	1.0	ns
t_{ZH}	LVTTL Output Enable Time from Z to HIGH	R_L = 500 Ω, C_L = 10 pF, See Figure 8	−	−	5.0	ns
t_{ZL}	LVTTL Output Enable Time from Z to LOW		−	−	5.0	ns
t_{HZ}	LVTTL Output Disable Time from HIGH to Z		−	−	5.0	ns
t_{LZ}	LVTTL Output Disable Time from LOW to Z		−	−	5.0	ns

2. All typical values are at T_A = 25°C and with V_{CC} = 5 V.
3. $t_{SK(PP)}$ is the magnitude of the difference in propagation delay times between any specified terminals of two devices switching in the same direction (either LOW−to−HIGH or HIGH−to−LOW) when both devices operate with the same supply voltage, same temperature, and have identical test circuits.

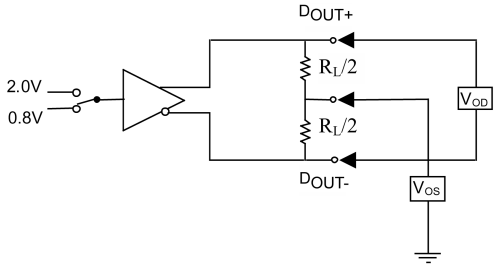
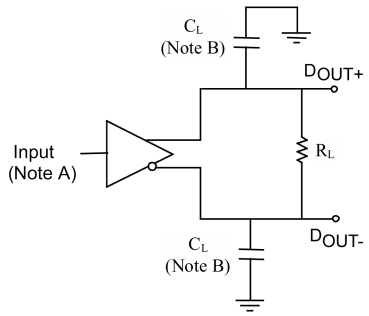


Figure 1. Differential Driver DC Test Circuit



NOTE A: Input pulses have frequency = 10 MHz, t_R or t_F = 2 ns
NOTE B: C_L includes all probe and fixture capacitances

Figure 2. Differential Driver Propagation Delay and Transition Time Test Circuit

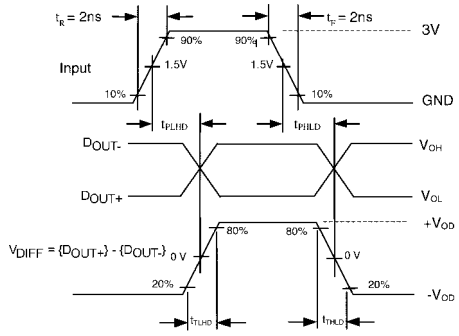
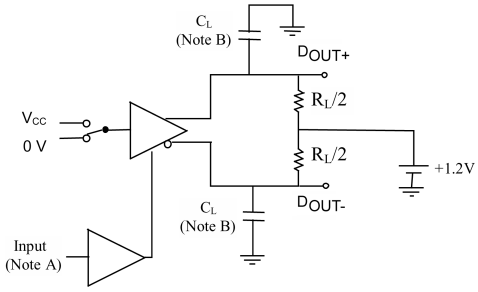


Figure 3. AC Waveforms for Differential Driver



NOTE B: Input pulses have the frequency = 10 MHz, t_R or t_F = 2 ns
NOTE A: C_L includes all probe and fixture capacitances

Figure 4. Differential Driver Enable and Disable Test Circuit

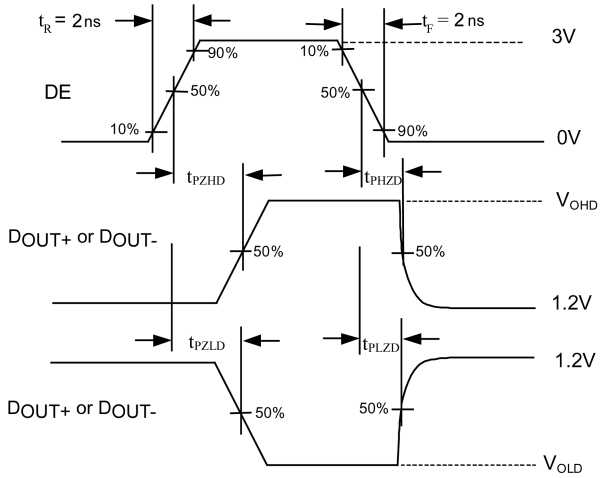
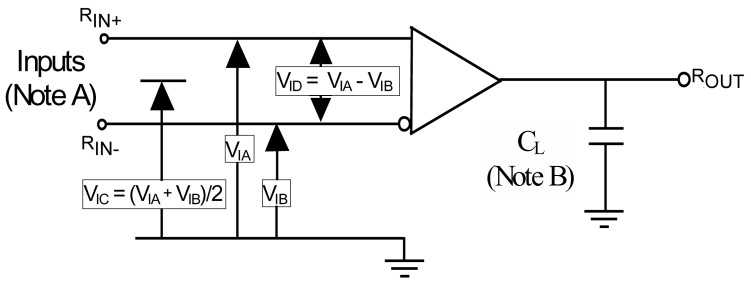


Figure 5. Enable and Disable AC Waveforms



NOTE A: Input pulses have frequency = 10 MHz, tR or tF = 1 ns
NOTE B: CL includes all probe and fixture capacitance

Figure 6. Differential Receiver Voltage Definitions and Propagation Delay and Transition Time Test Circuit

Table 1. RECEIVER MINIMUM AND MAXIMUM INPUT THRESHOLD TEST VOLTAGES

Applied Voltages (V)		Resulting Differential Input Voltage (mV)	Resulting Common Mode Input Voltage (V)
V_{IA}	V_{IB}	V_{ID}	V_{IC}
1.25	1.15	100	1.2
1.15	1.25	−100	1.2
2.4	2.3	100	2.35
2.3	2.4	−100	2.35
0.1	0	100	0.05
0	0.1	−100	0.05
1.5	0.9	600	1.2
0.9	1.5	−600	1.2
2.4	1.8	600	2.1
1.8	2.4	−600	2.1
0.6	0	600	0.3
0	0.6	−600	0.3

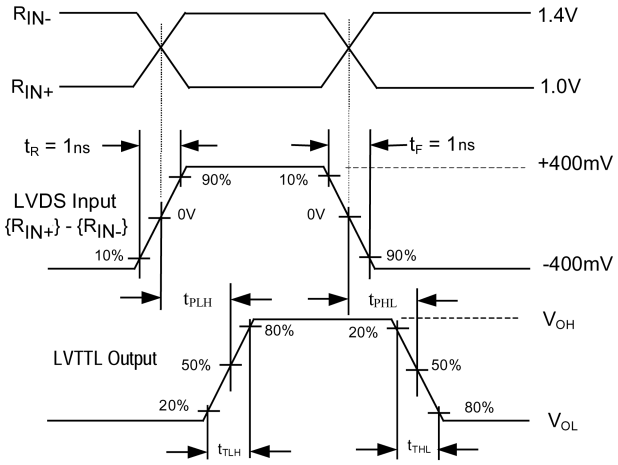
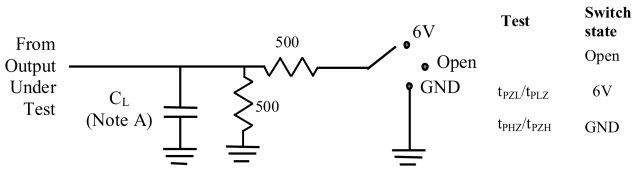
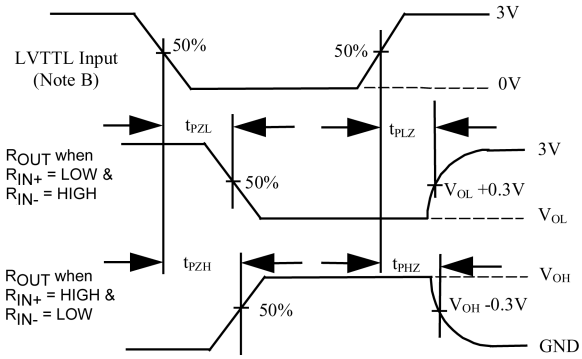


Figure 7. LVDS Input to LVTTL Output AC Waveforms



Test Circuit for LVTTL Outputs



Voltage Waveforms Enable and Disable Times

Figure 8. LVTTL Outputs Test Circuit and AC Waveforms

DC / AC TYPICAL PERFORMANCE CURVES

Drivers

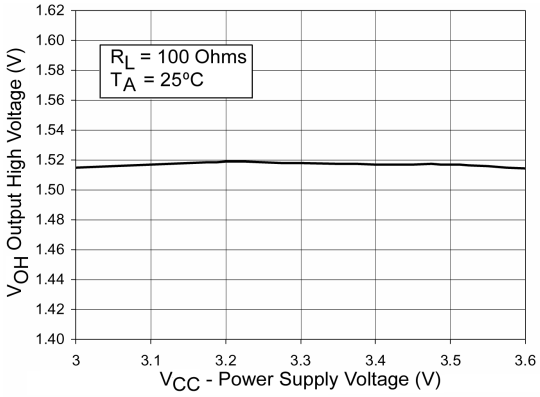


Figure 9. Output High Voltage vs. Power Supply Voltage

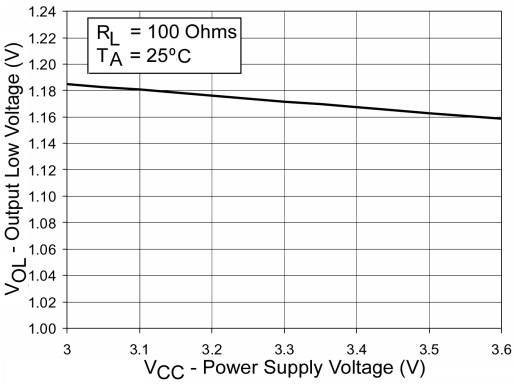


Figure 10. Output Low Voltage vs. Power Supply Voltage

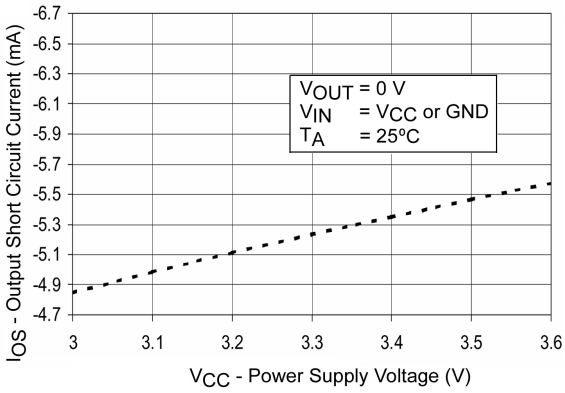


Figure 11. Output Short Circuit Current vs. Power Supply Voltage

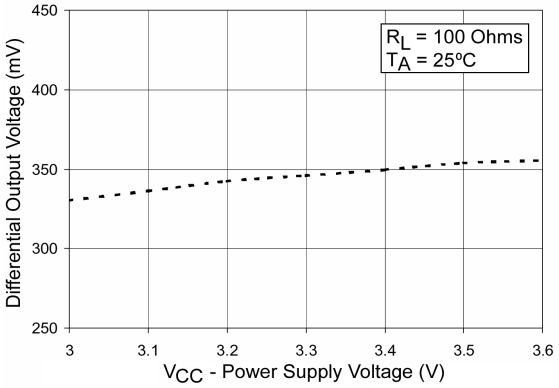


Figure 12. Differential Output Voltage vs. Power Supply Voltage

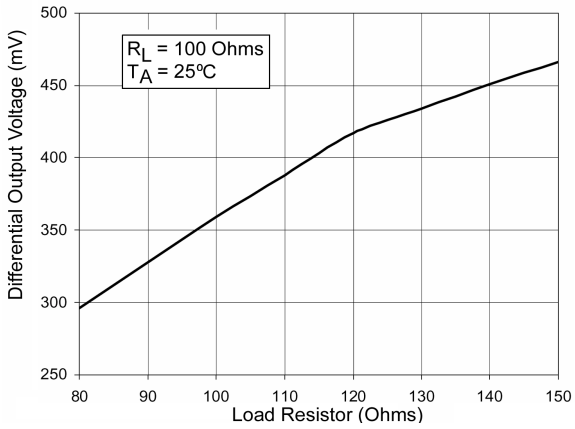


Figure 13. Differential Output Voltage vs. Load Resistor

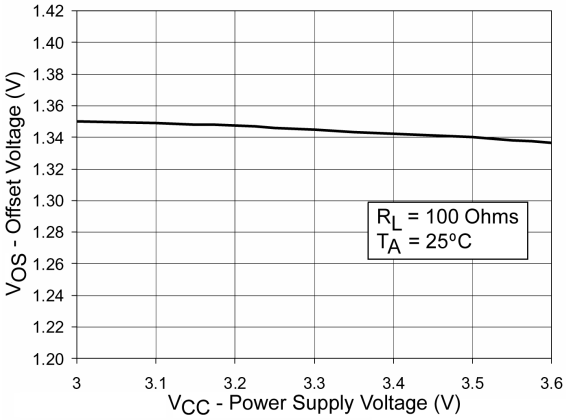


Figure 14. Offset Voltage vs. Power Supply Voltage

DC / AC TYPICAL PERFORMANCE CURVES (continued)

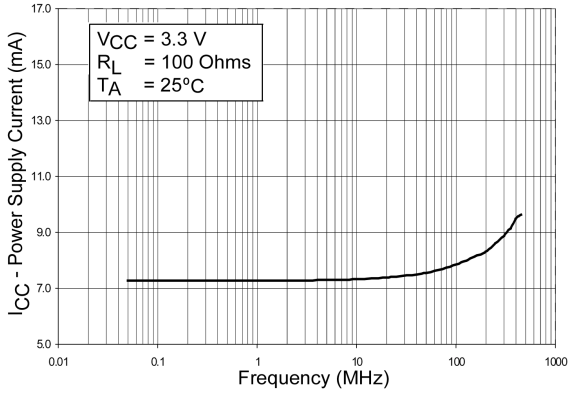


Figure 15. Power Supply Current vs. Frequency

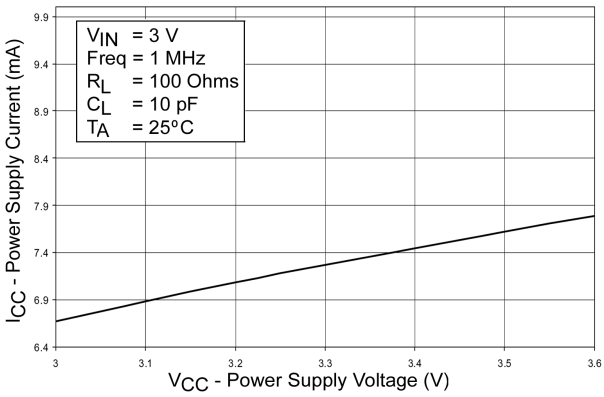


Figure 16. Power Supply Current vs. Power Supply Voltage

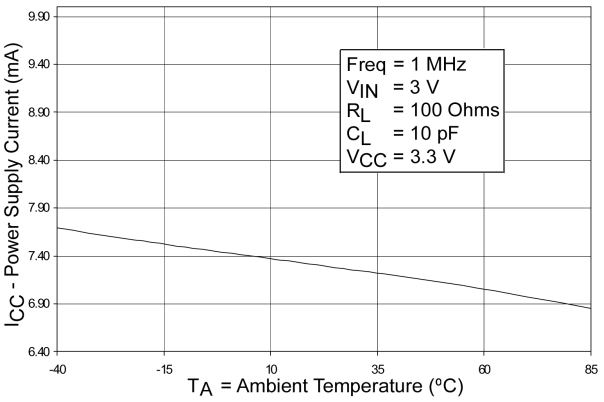


Figure 17. Power Supply Current vs. Ambient Temperature

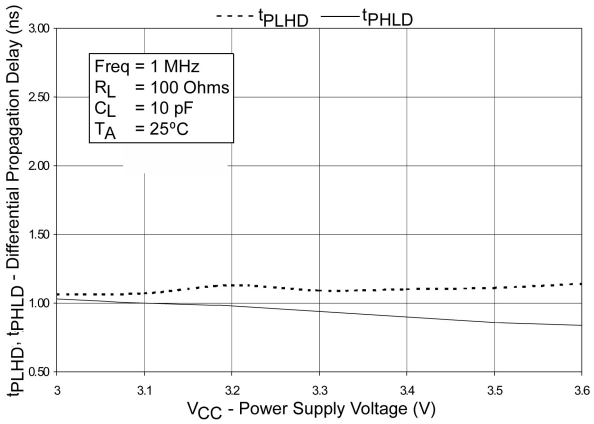


Figure 18. Differential Propagation Delay vs. Power Supply

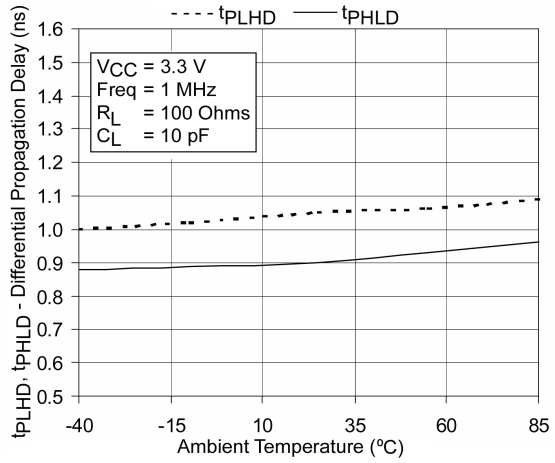


Figure 19. Differential Propagation Delay vs. Ambient Temperature

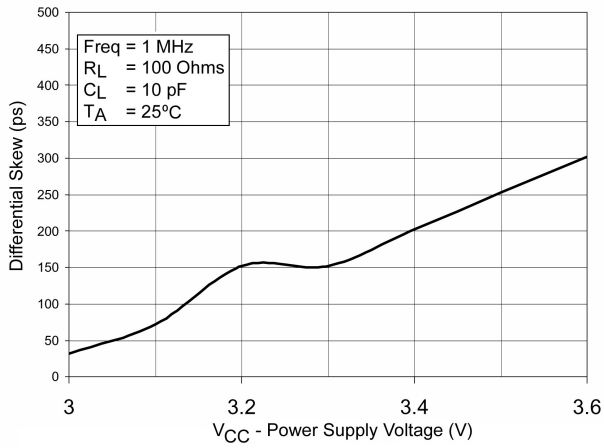


Figure 20. Differential Skew ($t_{PLH} - t_{PHL}$) vs. Power Supply Voltage

DC / AC TYPICAL PERFORMANCE CURVES (continued)

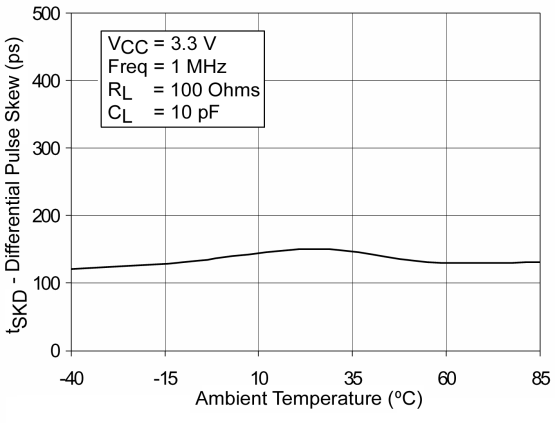


Figure 21. Differential Pulse Skew ($t_{PLH} - t_{PHL}$) vs. Ambient Temperature

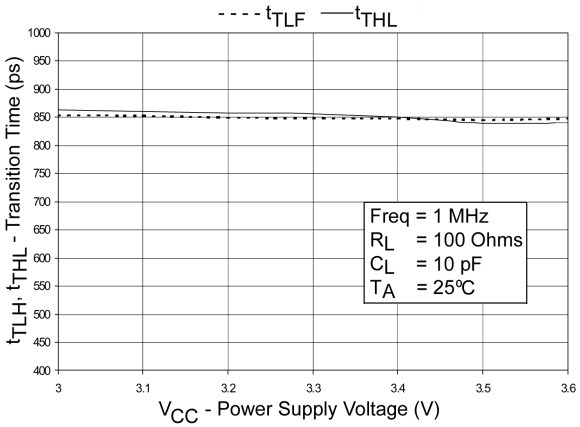


Figure 22. Transition Time vs. Power Supply Voltage

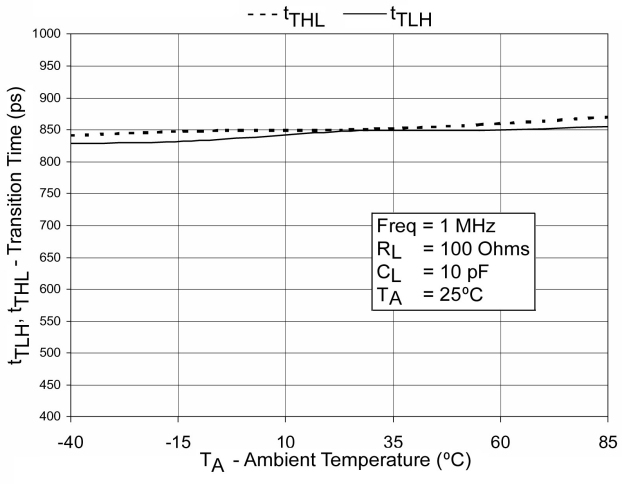


Figure 23. Transition Times vs. Ambient Temperature

DC / AC TYPICAL PERFORMANCE CURVES

Receiver

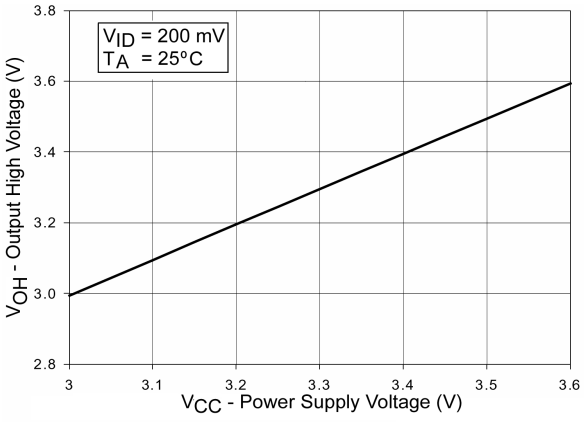


Figure 24. Output High Voltage vs. Power Supply Voltage

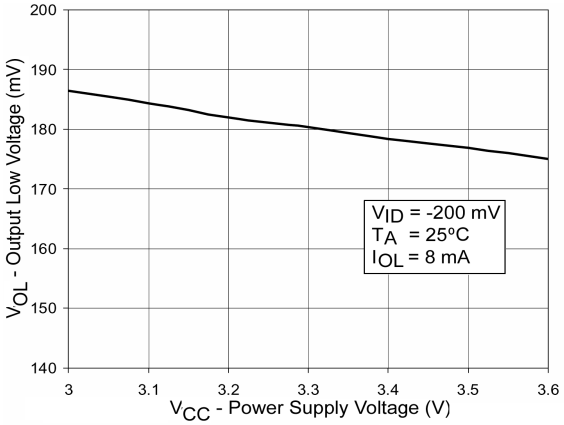


Figure 25. Output Low Voltage vs. Power Supply Voltage

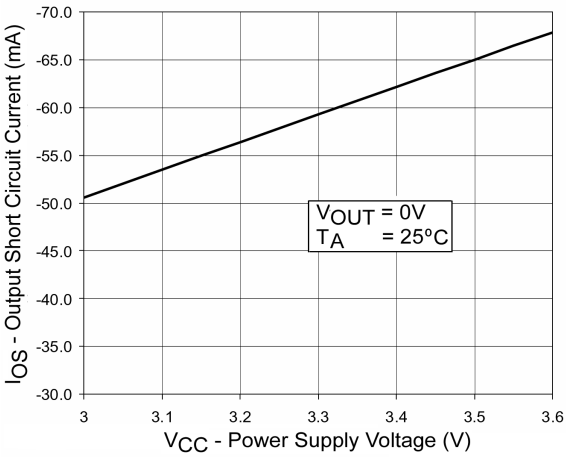


Figure 26. Output Short Circuit Current vs. Power Supply Voltage

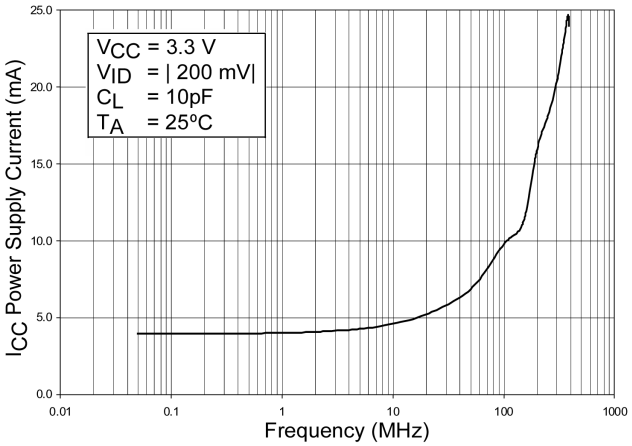


Figure 27. Power Supply Current vs. Frequency

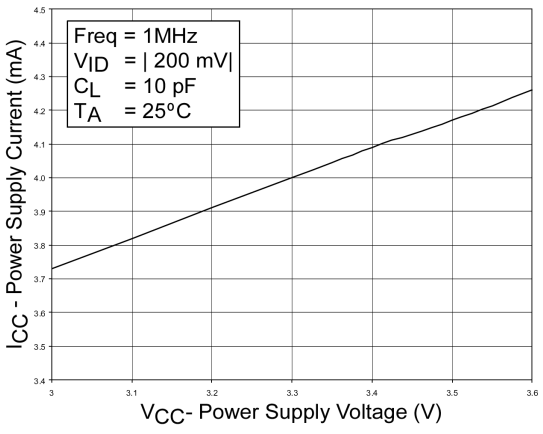


Figure 28. Power Supply Current vs. Power Supply Voltage

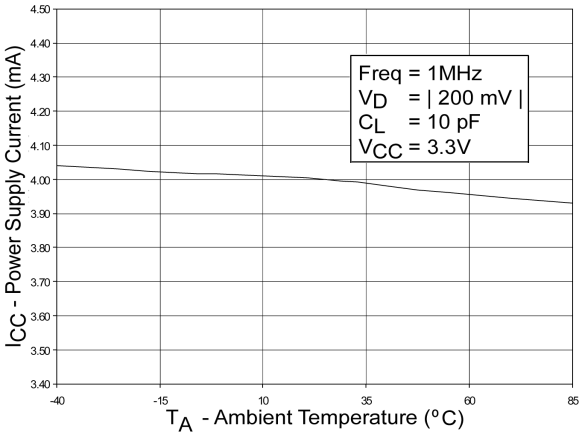


Figure 29. Power Supply Current vs. Ambient Temperature

DC / AC TYPICAL PERFORMANCE CURVES (continued)

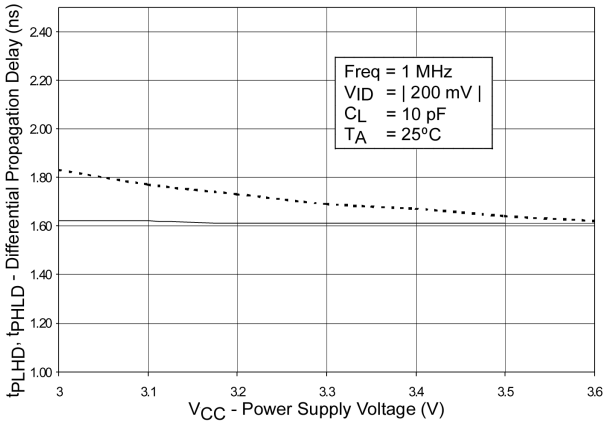


Figure 30. Differential Propagation Delay vs. Power Supply Voltage

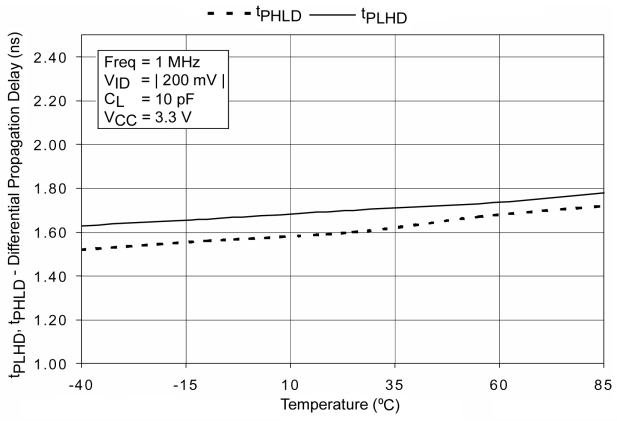


Figure 31. Differential Propagation Delay vs. Ambient Temperature

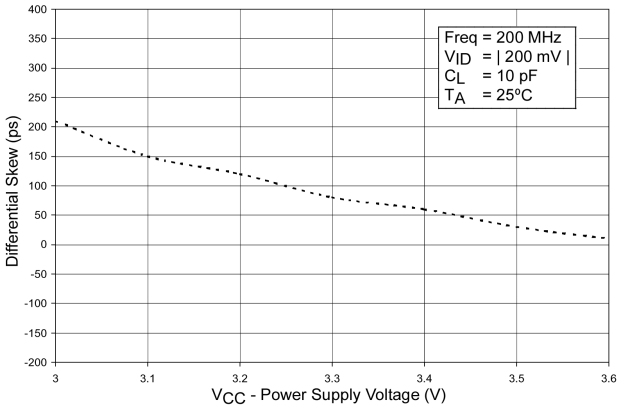


Figure 32. Differential Skew (t_{PHL} − t_{PHL}) vs. Power Supply Voltage

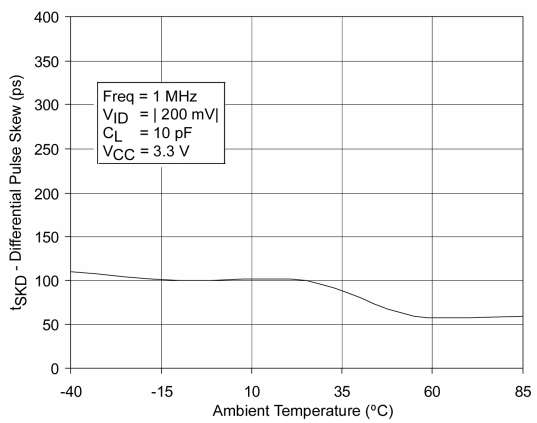


Figure 33. Differential Skew (t_{PLH} − t_{PHL}) vs. Ambient Temperature

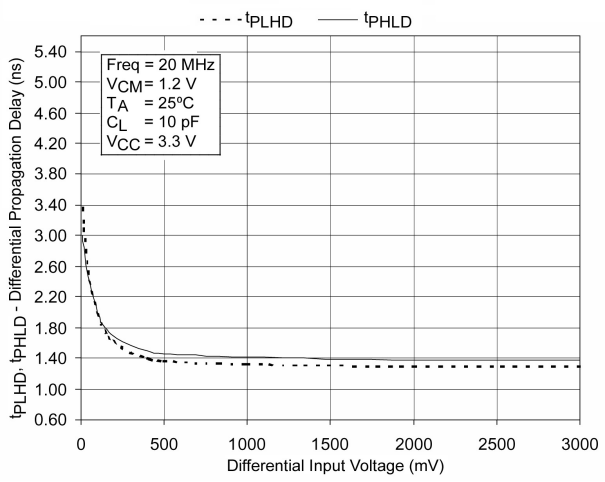


Figure 34. Differential Propagation Delay vs. Differential Input Voltage

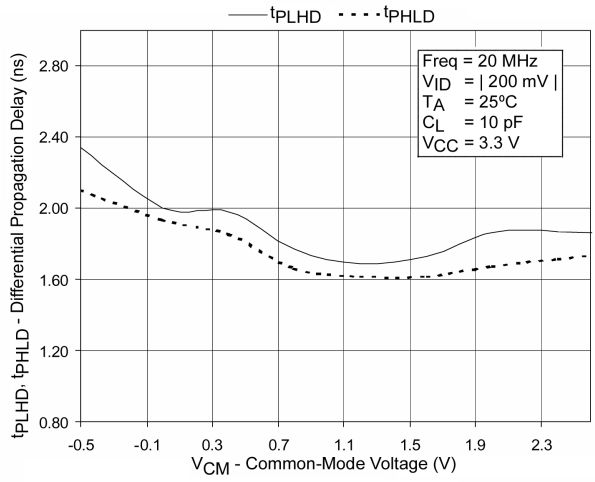


Figure 35. Differential Propagation Delay vs. Common−Mode Voltage

DC / AC TYPICAL PERFORMANCE CURVES (continued)

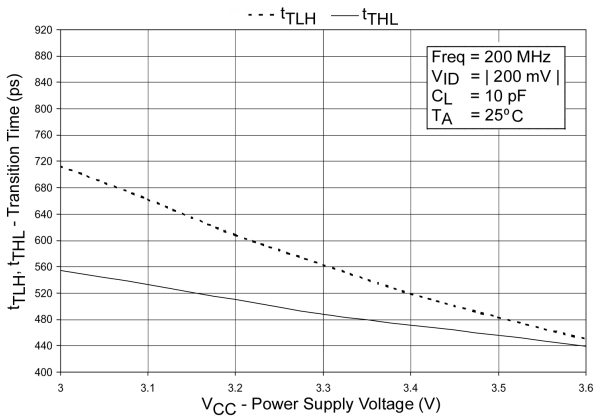


Figure 36. Transition Time vs. Power Supply Voltage

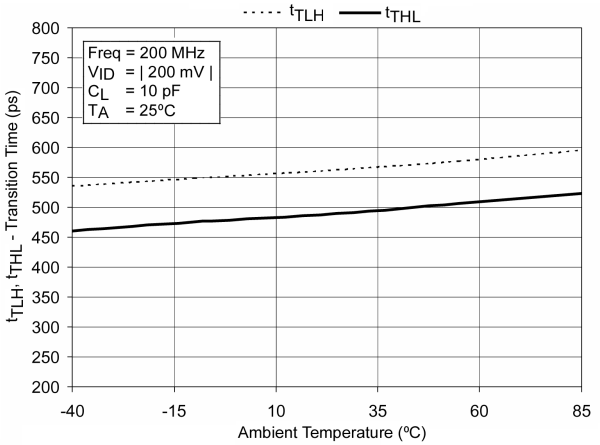


Figure 37. Transition Time vs. Ambient Temperature

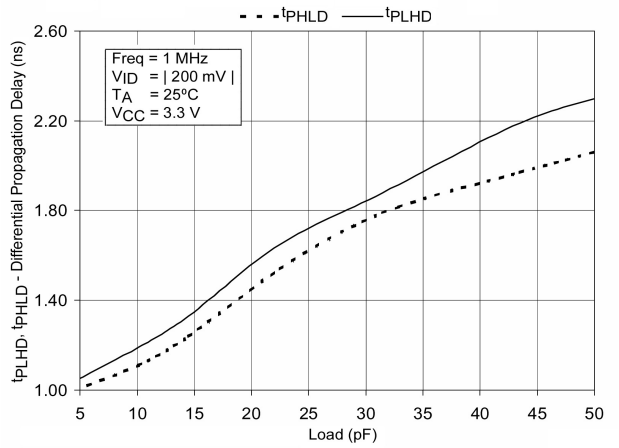


Figure 38. Differential Propagation Delay vs. Load

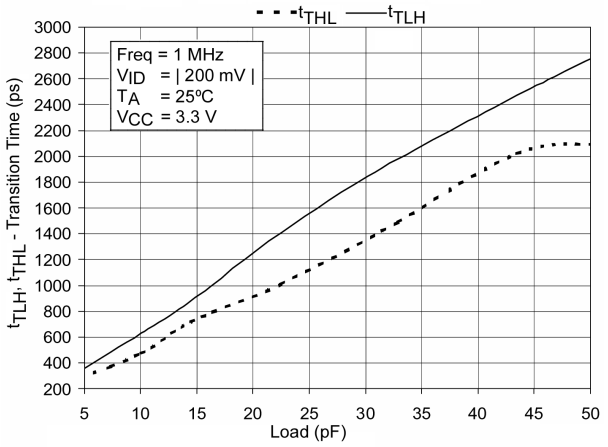
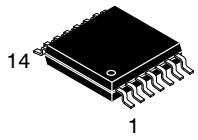


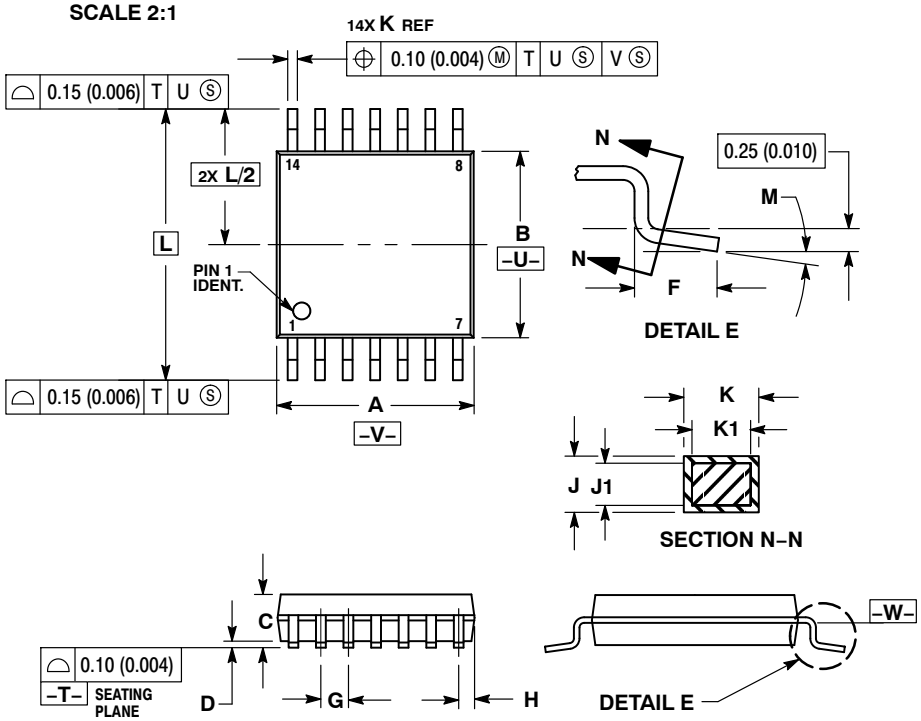
Figure 39. Transition Time vs. Load



SCALE 2:1

TSSOP−14 WB
CASE 948G
ISSUE C

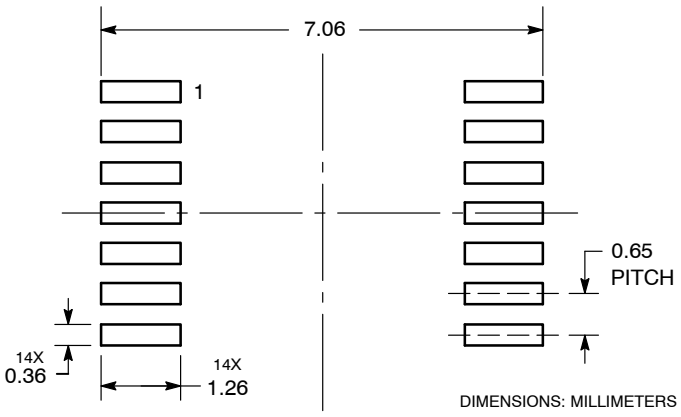
DATE 17 FEB 2016



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS. MOLD FLASH OR GATE BURRS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. DIMENSION B DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.25 (0.010) PER SIDE.
5. DIMENSION K DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE K DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
7. DIMENSION A AND B ARE TO BE DETERMINED AT DATUM PLANE −W−.

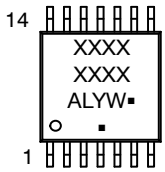
	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	4.90	5.10	0.193	0.200
B	4.30	4.50	0.169	0.177
C	−−−	1.20	−−−	0.047
D	0.05	0.15	0.002	0.006
F	0.50	0.75	0.020	0.030
G	0.65 BSC		0.026 BSC	
H	0.50	0.60	0.020	0.024
J	0.09	0.20	0.004	0.008
J1	0.09	0.16	0.004	0.006
K	0.19	0.30	0.007	0.012
K1	0.19	0.25	0.007	0.010
L	6.40 BSC		0.252 BSC	
M	0 °	8 °	0 °	8 °

RECOMMENDED SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the **onsemi** Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

GENERIC MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb−Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb−Free indicator, “G” or microdot “▪”, may or may not be present. Some products may not follow the Generic Marking.

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